SDLS007 D2635, JANUARY 1981 – REVISED MARCH 1988

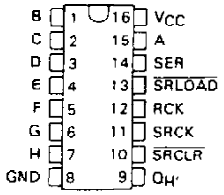
- **8-Bit Parallel Storage Register Inputs ('LS597)**
- **Parallel 3-State I/O, Storage Register Inputs, Shift Register Outputs ('LS598)**
- **Shift Register has Direct Overriding Load and Clear**
- **Accurate Shift-Frequency . . . DC to 20 MHz**

description

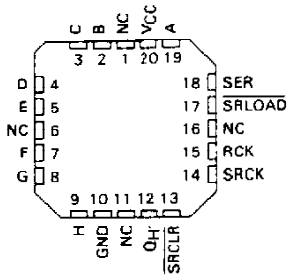
The 'LS597 comes in a 16-pin package and consists of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and shift register have positive-edge triggered clocks. The shift register also has direct load (from storage) and clear inputs.

The 'LS598 comes in a 20-pin package and has all the features of the 'LS597 plus 3-state I/O ports that provide parallel shift register outputs and also has multiplexed serial data inputs.

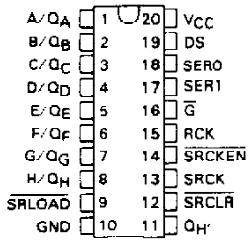
SN54LS597 . . . J OR W PACKAGE
SN74LS597 . . . N PACKAGE
(TOP VIEW)



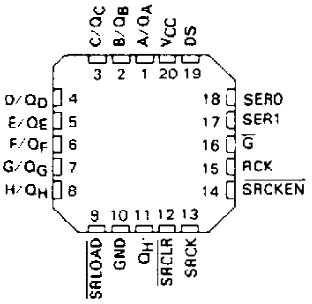
SN54LS597 . . . FK PACKAGE
(TOP VIEW)



SN54LS598 . . . J OR W PACKAGE
LS598 . . . DW OR N PACKAGE
(TOP VIEW)



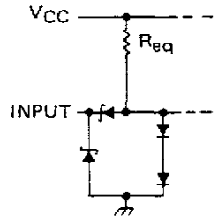
SN54LS598 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

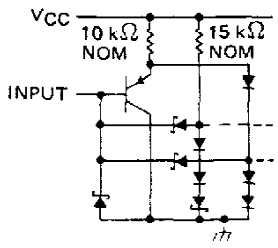
schematics of inputs and outputs

EQUIVALENT OF SERIAL AND A THRU H INPUTS

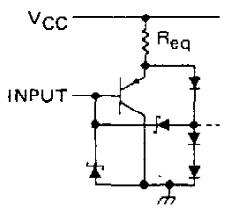


SERIAL: R_{eq} = 20 kΩ NOM
A thru H: R_{eq} = 25 kΩ NOM

EQUIVALENT OF SRCK INPUT ('LS598 ONLY)

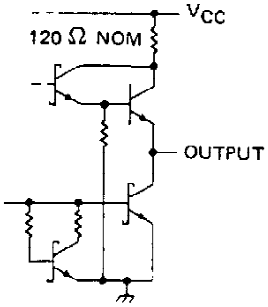


EQUIVALENT OF ALL OTHER INPUTS

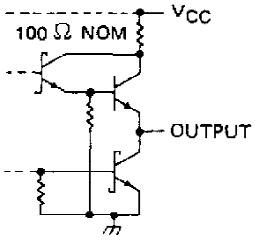


('LS597) RCK, SRCK: R_{eq} = 10 kΩ NOM
('LS598) RCK: R_{eq} = 10 kΩ NOM
ALL OTHER: R_{eq} = 13 kΩ NOM

TYPICAL OF $Q_{H'}$ OUTPUTS

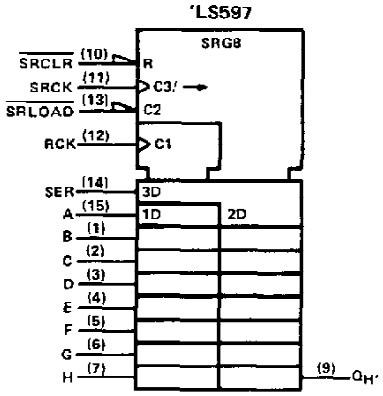


TYPICAL OF Q_A THRU Q_H OUTPUTS ('LS598 ONLY)

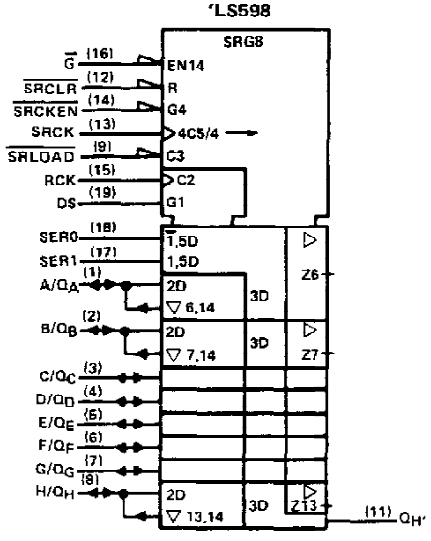


logic symbols†

'LS597

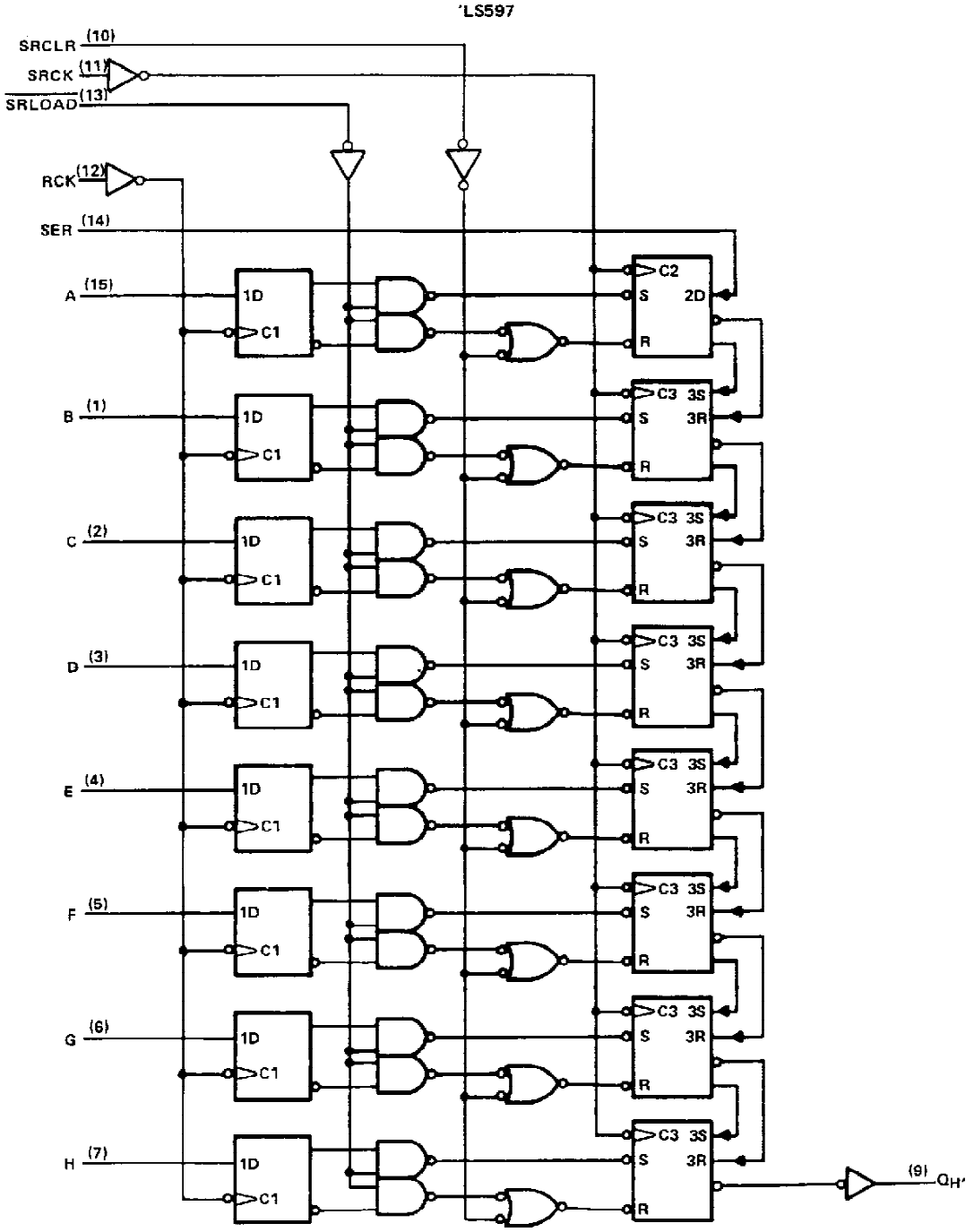


'LS598



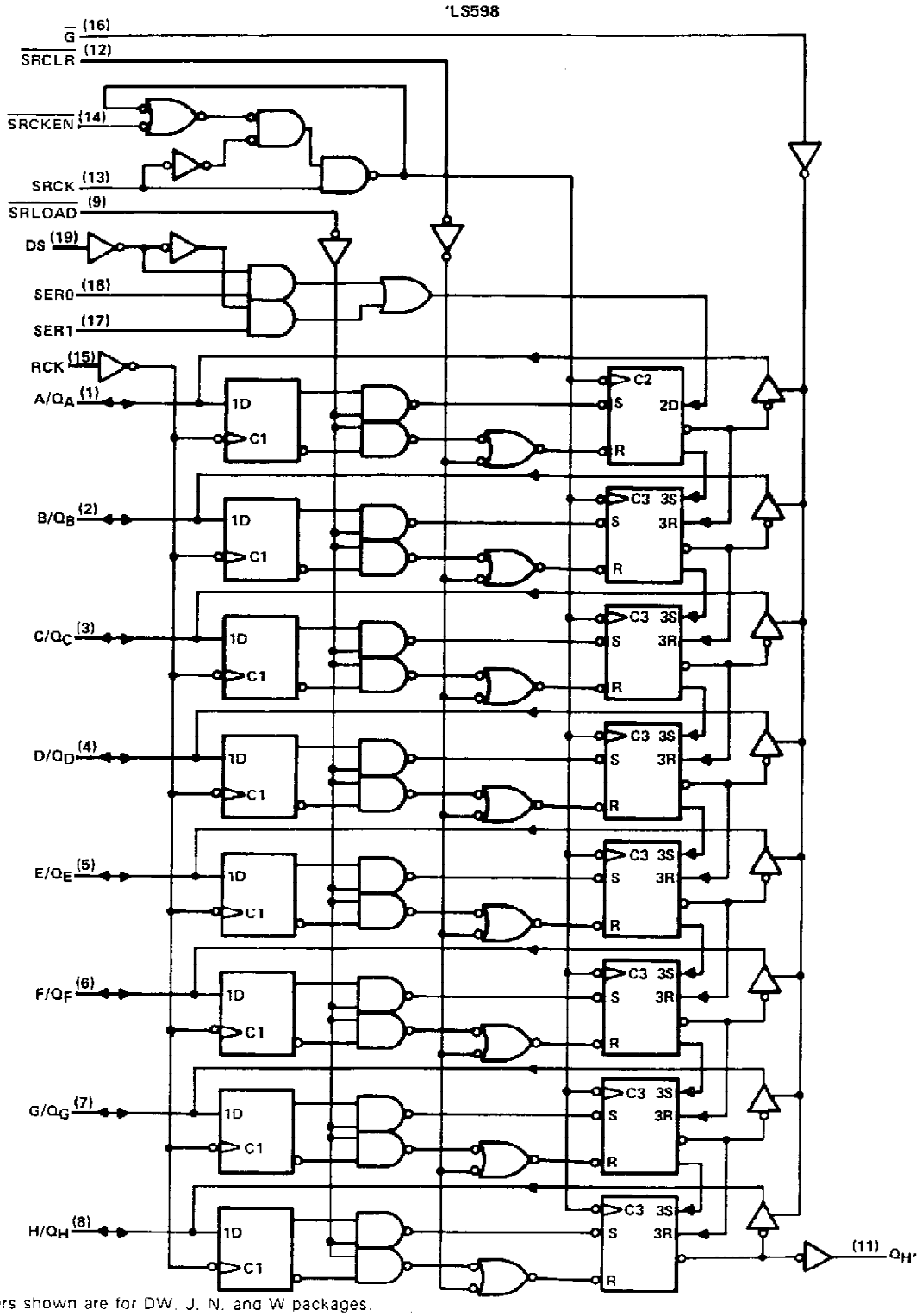
†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, N, and W packages.

logic diagram (positive logic)



Pin numbers shown are for DW, J, N, and W packages.

logic diagram (positive logic)



Pin numbers shown are for DW, J, N, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (excluding I/O ports) . . . . . 7 V
Off-state output voltage (including I/O ports) . . . . . 5.5 V
Operating free-air temperature range: SN54LS597, SN54LS598 . . . . . −55°C to 125°C
SN74LS597, SN74LS598 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

				SN54LS'			SN74LS'			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
I_{OH}	High-level output current	Q_H'				−1			−1	mA
		Q_A thru Q_H, 'LS598 only				−1			−2.6	
I_{OL}	Low-level output current	Q_H'				8			16	mA
		Q_A thru Q_H, 'LS598 only				12			24	
f_{SCK}	Shift clock frequency			0		20	0		20	MHz
t_w	Pulse duration	SRCK	high	15			15			ns
			low	35			35			
		RCK		20			20			
		$\overline{\text{SRCLR}}$		20			20			
		$\overline{\text{SRLOAD}}$		40			40			
t_{su}	Setup time	Data before RCK ↑		20			20			ns
		DS before SRCK ↑ ('LS598 only)		30			30			
		$\overline{\text{SRCKEN}}$ low before SRCK ↑ ('LS598 only)		20			20			
		$\overline{\text{SRCLR}}$ inactive before SRCK ↑		25			25			
		$\overline{\text{SRLOAD}}$ inactive before SRCK ↑		30			30			
		RCK ↑ before $\overline{\text{SRLOAD}}$ ↑ (see Note 2)		40			40			
		SER before SRCK ↑		20			20			
t_h	Hold time			0			0			ns
T_A	Operating free-air temperature			−55		125	0		70	°C

NOTE 2: The RCK ↑ before $\overline{\text{SRLOAD}}$ ↑ setup time ensures the data saved by RCK ↑ will also be loaded into the shift register.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†			SN54LS' MIN	SN54LS' TYP‡	SN54LS' MAX	SN74LS' MIN	SN74LS' TYP‡	SN74LS' MAX	UNIT
V_{IK}			V_{CC} = MIN, I_I = −18 mA					−1.5			−1.5	V
V_{OH}	'LS598 Q		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX	I_{OH} = −1 mA		2.4	3.2					V
				I_{OH} = −2.6 mA					2.4	3.1		
	Q_H'			I_{OH} = −1 mA		2.4	3.2		2.4	3.2		
V_{OL}	'LS598 Q		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX	I_{OL} = 12 mA			0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA						0.35	0.5	
	Q_H'			I_{OL} = 8 mA			0.25	0.4		0.25	0.4	
				I_{OL} = 16 mA						0.35	0.5	
I_{OZH}	'LS598 Q		V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = MAX, V_O = 2.7 V					20			20	μA
I_{OZL}	'LS598 Q		V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = MAX, V_O = 0.4 V					−0.4			−0.4	mA
I_I	'LS598 Q		V_{CC} = MAX	V_I = 5.5 V				0.1			0.1	mA
	Others			V_I = 7 V				0.1			0.1	
I_{IH}			V_{CC} = MAX, V_I = 2.7 V					20			20	μA
I_{IL}	'LS598 SRCK		V_{CC} = MAX, V_I = 0.4 V					−0.8			−0.8	mA
	SER, A Thru H							−0.4			−0.4	
	Others							−0.2			−0.2	
I_{OS}§	'LS598 Q		V_{CC} = MAX, V_O = 0 V			−30		−130	−30		−130	mA
	Q_H'					−20		−100	−20		−100	
I_{CC}	'LS597	I_{CCH}	V_{CC} = MAX, All possible inputs grounded, All outputs open				35	53		35	53	mA
		I_{CCL}					35	53		35	53	
	'LS598	I_{CCH}					45	68		45	68	
		I_{CCL}					54	80		54	80	
		I_{CCZ}					56	85		56	85	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C
§ Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

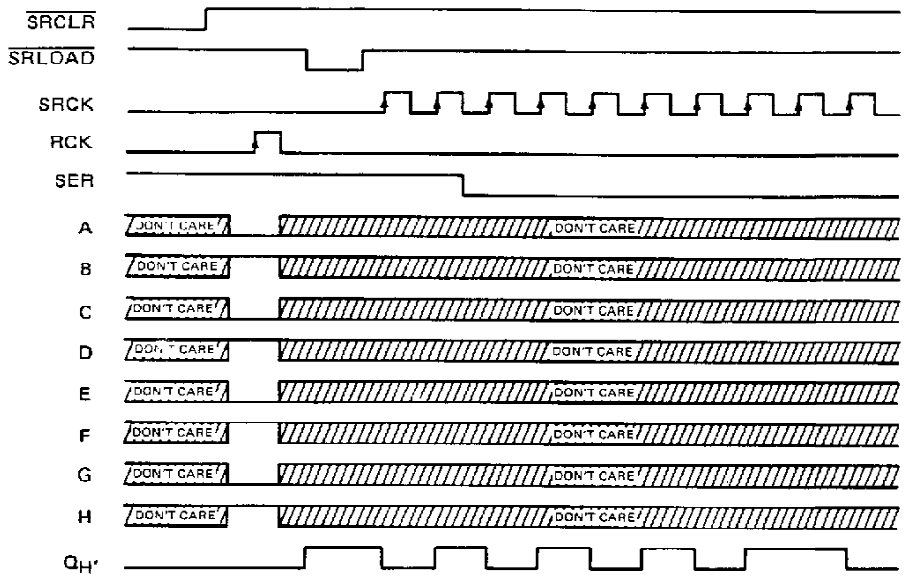
switching characteristics, V_{CC} = 5 V, T_A = 25°C, (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS597			'LS598			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	SRCK	Q	R_L = 667 Ω, C_L = 45 pF	20	35		20	35		MHz
f_{max}	SRCK	Q_H'	R_L = 1 kΩ, C_L = 30 pF	20	35					MHz
t_{PLH}	SRCK↑	Q_H'	R_L = 1 kΩ, C_L = 30 pF		15	23		11	17	ns
t_{PHL}	SPCK↑	Q_H'			20	30		15	23	ns
t_{PLH}	$\overline{\text{SRLOAD}}$↓	Q_H'			38	57		28	42	ns
t_{PHL}	$\overline{\text{SRLOAD}}$↓	Q_H'			29	44		20	30	ns
t_{PHL}	$\overline{\text{SRCLR}}$↓	Q_H'			24	36		18	27	ns
t_{PLH}	RCK↑	Q_H'	R_L = 1 kΩ, C_L = 30 pF		41	60		32	48	ns
t_{PHL}	RCK↑	Q_H'	SRLOAD = L		32	48		24	36	ns
t_{PLH}	SRCK↑	Q	R_L = 667 Ω, C_L = 45 pF					12	18	ns
t_{PHL}	SRCK↑	Q						19	28	ns
t_{PLH}	$\overline{\text{SRLOAD}}$↓	Q						32	48	ns
t_{PHL}	$\overline{\text{SRLOAD}}$↓	Q						27	40	ns
t_{PHL}	$\overline{\text{SRCLR}}$↓	Q						25	38	ns
t_{PZH}	G↓	Q						26	31	ns
t_{PZL}	G↓	Q						29	43	ns
t_{PHZ}	G↑	Q	R_L = 667 Ω, C_L = 5 pF					25	38	ns
t_{PLZ}	G↑	Q						20	30	ns

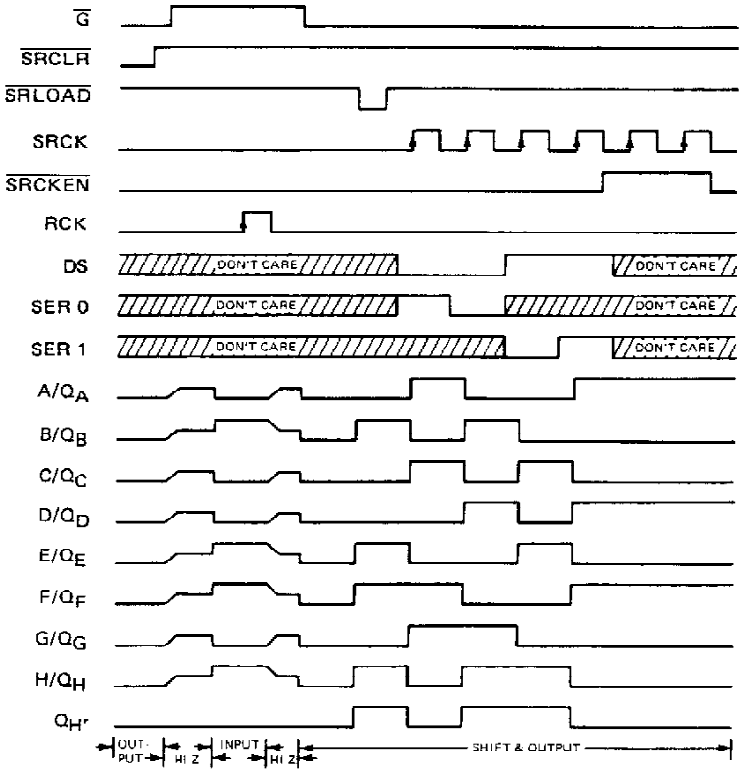
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

typical operating sequences

'LS597



'LS598



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