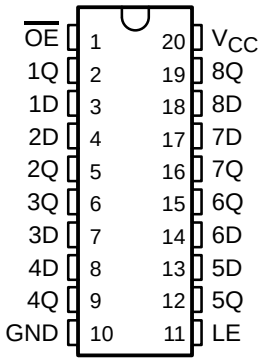
- **Eight Latches in a Single Package**
- **3-State True Outputs With 25-Ω Sink Resistors**
- **Full Parallel Access for Loading**
- **Buffered Control Inputs**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB) Packages, and Plastic (N) DIPs**

DB, DW, OR N PACKAGE
(TOP VIEW)



description

This 8-bit latch features 3-state outputs designed to sink up to 12 mA, and include 25-Ω sink resitors to reduce overshoot and undershoot.

The eight latches of the SN74F2373 are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When the LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$ input does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

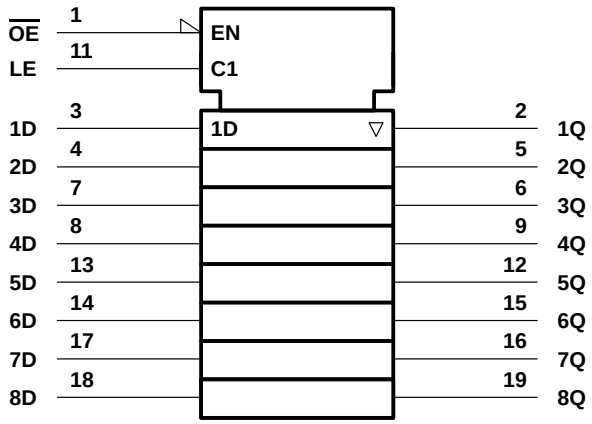
The SN74F373 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74F373 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each latch)

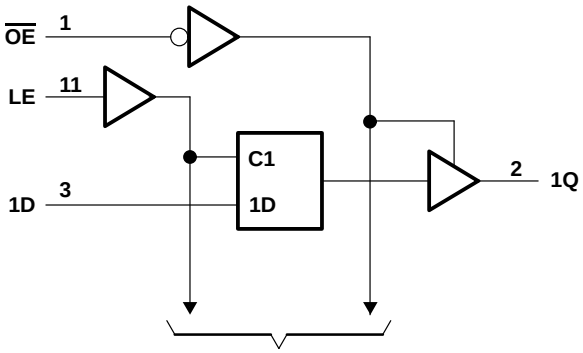
INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



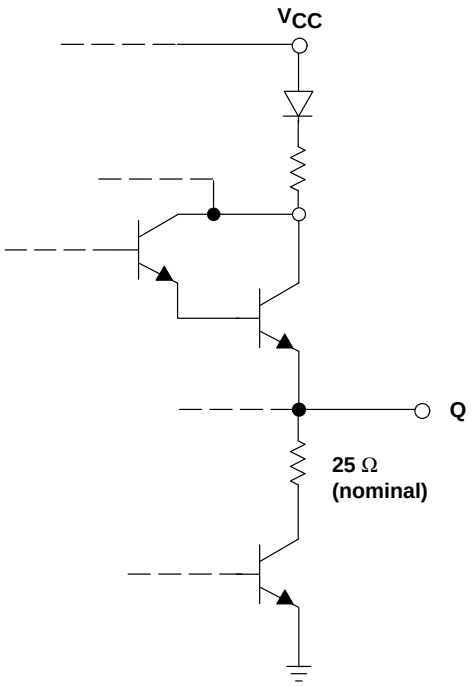
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Seven Other Channels

schematic diagram



Typical Output Configuration

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –1.2 V to 7 V
Input current range, I_I . . . . . –30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state, V_O . . . . . –0.5 V to 5.5 V
Voltage range applied to any output in the high state, V_O . . . . . –0.5 V to V_{CC}
Current into any output in the low state, I_O . . . . . 30 mA
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded if the input current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			– 3	mA
I_{OL}	Low-level output current			12	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA			–1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = – 1 mA	2.5	3.4		V
		I_{OH} = – 3 mA	2.4	3.3		
	V_{CC} = 4.75 V,	I_{OH} = -1 mA to – 3 mA	2.7			
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 1 mA		0.2	0.5	V
		I_{OL} = 12 mA		0.5	0.75	
$I_{OZ(H)}$	V_{CC} = 5.5 V,	V_O = 2.7 V			50	µA
$I_{OZ(L)}$	V_{CC} = 5.5 V,	V_O = 0.5 V			–50	µA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			– 0.6	mA
I_{OS}§	V_{CC} = 5.5 V,	V_O = 0	–60		–150	mA
$I_{CC(H)}$	V_{CC} = 5.5 V,	See Note 2, Condition A		38	55	mA
$I_{CC(L)}$	V_{CC} = 5.5 V,	See Note 2, Condition B		46	66	mA
$I_{CC(Z)}$	V_{CC} = 5.5 V,	See Note 2, Condition C		43	62	mA

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: I_{CC} is measured with the outputs open under the following conditions:
A. $\overline{OE}$ at ground (0) and all other inputs at 4.5 V.
B. LE at 4.5 V and all other inputs grounded.
C. $\overline{OE}$ at 4.5 V and all other inputs grounded.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

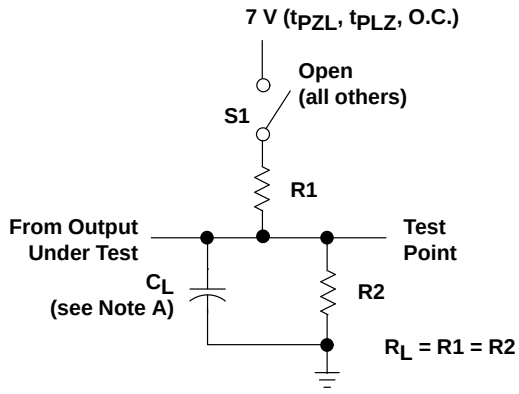
		V_{CC} = 5 V, T_A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t_w	Pulse duration, LE high	6		6		ns
t_{su}	Setup time, data before LE↓	2		2		ns
t_h	Hold time, data after LE↓	5		6		ns

switching characteristics (see Figure 1)

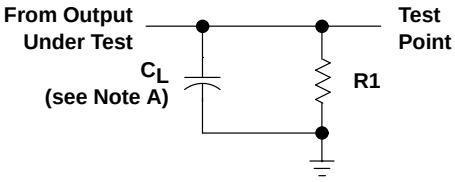
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 PF, R_1 = 500 Ω, R_2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V TO 5.5 V, C_L = 50 PF, R_1 = 500 Ω, R_2 = 500 Ω, T_A = MIN TO MAX†		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	D	Q	2.2	4.4	7	2.1	9	ns
t_{PHL}			1.2	4.1	5.5	1.2	7	
t_{PLH}	LE	Q	4.2	7.3	11.5	4.2	13	ns
t_{PHL}			2.2	4.2	7	2.2	8	
t_{PZH}	$\overline{OE}$	Q	1.2	4.1	11	1.2	12	ns
t_{PZL}			1.2	6	8.3	1.2	9.5	
t_{PHZ}	$\overline{OE}$	Q	1.2	4.2	6.5	1.2	7.5	ns
t_{PLZ}			1.2	3.5	6	1.2	6	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

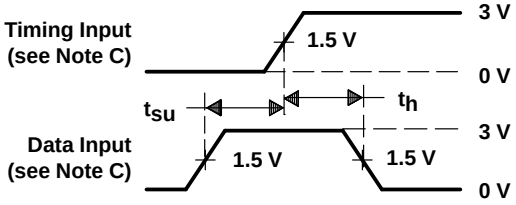
PARAMETER MEASUREMENT INFORMATION



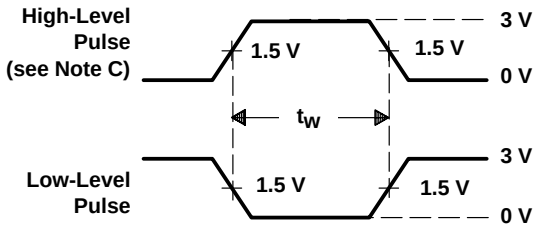
LOAD CIRCUIT FOR
3-STATE AND OPEN-COLLECTOR OUTPUTS



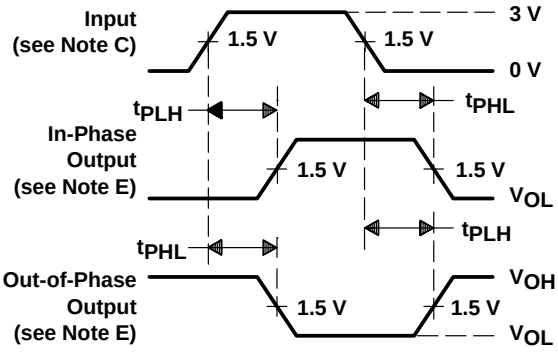
LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS



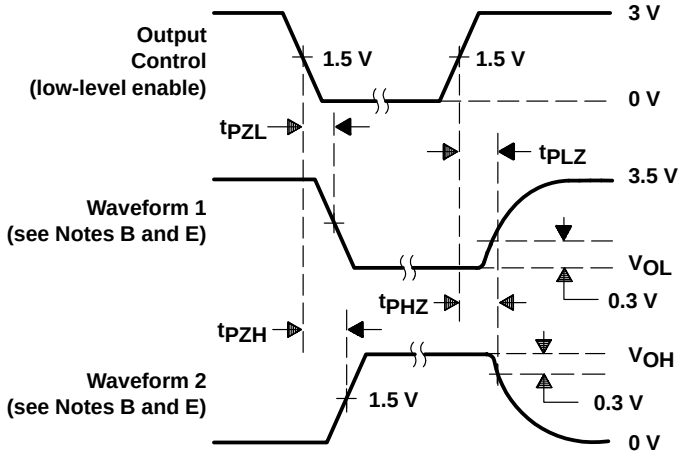
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (see Note D)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $t_r = t_f \leq 2.5$ ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is open.
E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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