

# SN54F299, SN74F299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS

SDFS071A – MARCH 1987 – REVISED OCTOBER 1993

- **Four Modes of Operation:**  
Hold (Store)  
Shift Right  
Shift Left  
Load Data
- Operates With Outputs Enabled or at High Impedance
- 3-State Outputs Drive Bus Lines Directly
- Can Be Cascaded for N-Bit Word Lengths
- Direct Overriding Clear
- **Applications:**  
Stacked or Push-Down Registers  
Buffer Storage  
Accumulator Registers
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

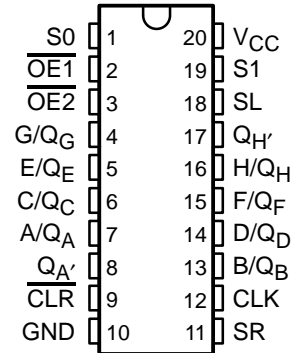
## description

These 8-bit universal shift/storage registers feature multiplexed I/O ports to achieve full 8-bit data handling in a single 20-pin package. Two function-select ( $S_0$ ,  $S_1$ ) inputs and two output-enable ( $\overline{OE1}$ ,  $\overline{OE2}$ ) inputs can be used to choose the modes of operation listed in the function table.

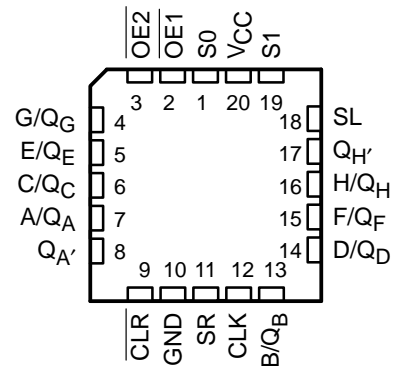
Synchronous parallel loading is accomplished by taking both  $S_0$  and  $S_1$  high. This places the 3-state outputs in a high-impedance state and permits data that is applied on the I/O ports to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. Clearing occurs when the clear ( $\overline{CLR}$ ) input is low. Taking either  $\overline{OE1}$  or  $\overline{OE2}$  high disables the outputs but has no effect on clearing, shifting, or storage of data.

The SN54F299 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74F299 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54F299 . . . J PACKAGE  
SN74F299 . . . DW OR N PACKAGE  
(TOP VIEW)



SN54F299 . . . FK PACKAGE  
(TOP VIEW)



# SN54F299, SN74F299

## 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

### WITH 3-STATE OUTPUTS

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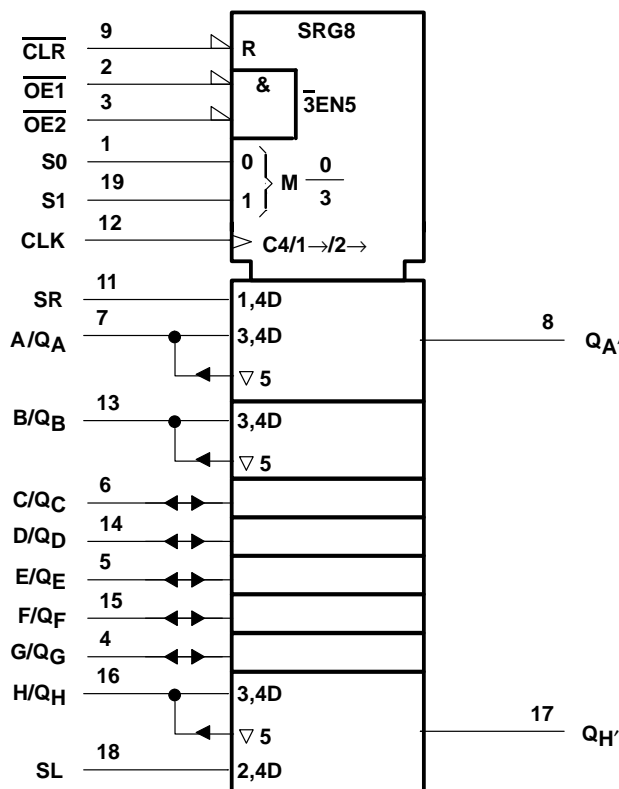
FUNCTION TABLE

MODE	INPUTS								I/O PORTS								OUTPUTS	
	CLR	S1	S0	$\overline{OE1}^\dagger$	$\overline{OE2}^\dagger$	CLK	SL	SR	A/Q <sub>A</sub>	B/Q <sub>B</sub>	C/Q <sub>C</sub>	D/Q <sub>D</sub>	E/Q <sub>E</sub>	F/Q <sub>F</sub>	G/Q <sub>G</sub>	H/Q <sub>H</sub>	Q <sub>A</sub> '	Q <sub>H</sub> '
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	L	L
Hold	H	L	L	L	L	X	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>	Q <sub>E0</sub>	Q <sub>F0</sub>	Q <sub>G0</sub>	Q <sub>H0</sub>	Q <sub>A0</sub>	Q <sub>H0</sub>
	H	X	X	L	L	L	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>	Q <sub>E0</sub>	Q <sub>F0</sub>	Q <sub>G0</sub>	Q <sub>H0</sub>	Q <sub>A0</sub>	Q <sub>H0</sub>
Shift Right	H	L	H	L	L	↑	X	H	H	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	Q <sub>En</sub>	Q <sub>Fn</sub>	Q <sub>Gn</sub>	H	Q <sub>Gn</sub>
	H	L	H	L	L	↑	X	L	L	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	Q <sub>En</sub>	Q <sub>Fn</sub>	Q <sub>Gn</sub>	L	Q <sub>Gn</sub>
Shift Left	H	H	L	L	L	↑	H	X	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	Q <sub>En</sub>	Q <sub>Fn</sub>	Q <sub>Gn</sub>	Q <sub>Hn</sub>	H	Q <sub>Bn</sub>	H
	H	H	L	L	L	↑	L	X	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	Q <sub>En</sub>	Q <sub>Fn</sub>	Q <sub>Gn</sub>	Q <sub>Hn</sub>	L	Q <sub>Bn</sub>	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

NOTE: a . . . h = the level of the steady-state input at inputs A through H, respectively. This data is loaded into the flip-flops while the flip-flop outputs are isolated from the I/O terminals.

† When one or both output-enable inputs are high the eight I/O terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

### logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

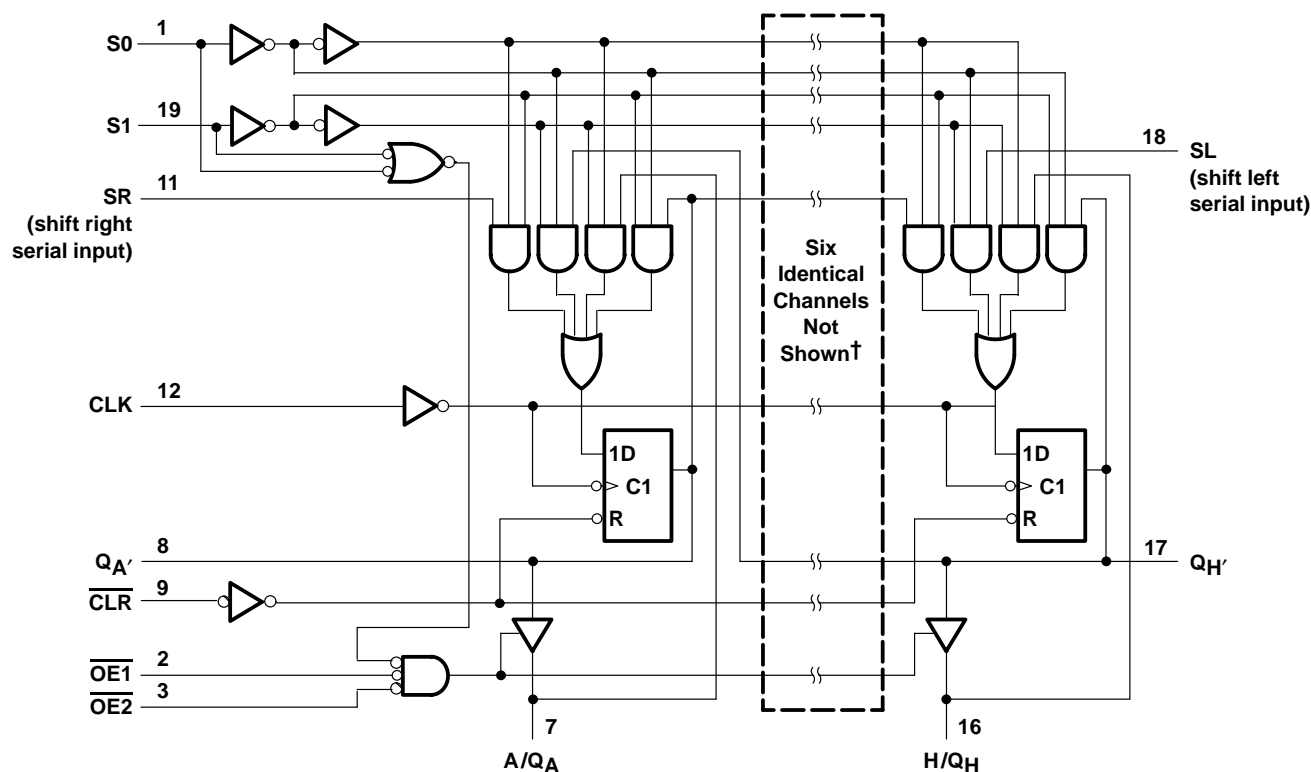
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## 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

### WITH 3-STATE OUTPUTS

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#### logic diagram (positive logic)



† I/O ports not shown: B/Q<sub>B</sub> (13), C/Q<sub>C</sub> (6), D/Q<sub>D</sub> (14), E/Q<sub>E</sub> (5), F/Q<sub>F</sub> (15), and G/Q<sub>G</sub> (4).

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–1.2 V to 7 V
Input current range	–30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state	–0.5 V to 5.5 V
Voltage range applied to any output in the high state	–0.5 V to $V_{CC}$
Current into any output in the low state: $Q_A'$ or $Q_H'$	40 mA
SN54F299 ( $Q_A$ thru $Q_H$ )	40 mA
SN74F299 ( $Q_A$ thru $Q_H$ )	48 mA
Operating free-air temperature range: SN54F299	–55°C to 125°C
SN74F299	0°C to 70°C
Storage temperature range	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

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## 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

### WITH 3-STATE OUTPUTS

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#### recommended operating conditions

			SN54F299			SN74F299			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage		2			2			V
V <sub>IL</sub>	Low-level input voltage		0.8			0.8			V
I <sub>IK</sub>	Input clamp current		−18			−18			mA
I <sub>OH</sub>	High-level output current	Q <sub>A</sub> ' or Q <sub>H</sub> '	−1			−1			mA
		Q <sub>A</sub> thru Q <sub>H</sub>	−3			−3			
I <sub>OL</sub>	Low-level output current	Q <sub>A</sub> ' or Q <sub>H</sub> '	20			20			mA
		Q <sub>A</sub> thru Q <sub>H</sub>	20			24			
T <sub>A</sub>	Operating free-air temperature		−55	125		0	70		°C

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54F299			SN74F299			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{IK}$		$V_{CC} = 4.5\text{ V}$ ,	$I_I = -18\text{ mA}$			–1.2			–1.2	V
$V_{OH}$	$Q_A'$ or $Q_H'$	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -1\text{ mA}$	2.5	3.4		2.5	3.4		V
	$Q_A$ thru $Q_H$		$I_{OH} = -1\text{ mA}$	2.5	3.4		2.5	3.4		
	$Q_A$ thru $Q_H$		$I_{OH} = -3\text{ mA}$	2.4	3.3		2.4	3.3		
	Any output	$V_{CC} = 4.75\text{ V}$ ,	$I_{OH} = -1\text{ mA to } -3\text{ mA}$				2.7			
$V_{OL}$	$Q_A'$ or $Q_H'$	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 20\text{ mA}$	0.3	0.5		0.3	0.5		V
	$Q_A$ thru $Q_H$		$I_{OL} = 20\text{ mA}$	0.3	0.5					
	$Q_A$ thru $Q_H$		$I_{OL} = 24\text{ mA}$				0.35	0.5		
	Any output	$V_{CC} = 4.75\text{ V}$ ,	$I_{OL} = 1\text{ mA to } 3\text{ mA}$				2.7			
$I_I$	A thru H	$V_{CC} = 5.5\text{ V}$	$V_I = 5.5\text{ V}$			1			1	mA
	Any other		$V_I = 7\text{ V}$			0.1			0.1	
$I_{IH}^\ddagger$	A thru H	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 2.7\text{ V}$			70			70	$\mu\text{A}$
	Any other					20			20	
$I_{IL}^\ddagger$	A thru H	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 0.5\text{ V}$			–0.65			–0.65	mA
	S0 or S1					–1.2			–1.2	
	Any other					–0.6			–0.6	
	Any other	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 0.5\text{ V}$			–0.6			–0.6	
$I_{OS}^\S$		$V_{CC} = 5.5\text{ V}$ ,	$V_O = 0$	–60		–150	–60		–150	mA
$I_{CC}$		$V_{CC} = 5.5\text{ V}$ ,	See Note 2	68		95	68		95	mA

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ For I/O ports ( $Q_A$  thru  $Q_H$ ), the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2:  $I_{CC}$  is measured with  $\text{OE1}$ ,  $\text{OE2}$ , and  $\text{CLK}$  at 4.5 V.



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## 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

### WITH 3-STATE OUTPUTS

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		SN54F299		SN74F299		UNIT	
				'F299							
				MIN	MAX	MIN	MAX	MIN	MAX		
f <sub>clock</sub>	Clock frequency			0	70	0	65	0	70	MHz	
t <sub>w</sub>	Pulse duration		CLK high or low	7		8		7		ns	
			$\overline{\text{CLR}}$ low	7		8		7			
t <sub>su</sub>	Setup time before CLK↑	S0 or S1	High or low	8.5		9.5		8.5		ns	
		A/Q <sub>A</sub> thru H/Q <sub>H</sub> , SR, or SL	High or low	5.5		6.5		5.5			
		Inactive-state setup time before CLK↑↑	$\overline{\text{CLR}}$	High	7		13		7		
t <sub>h</sub>	Hold time after CLK↑		S0 or S1	High or low	0		0		0		ns
			A/Q <sub>A</sub> thru H/Q <sub>H</sub> , SR, or SL	High or low	2		2		2		

† Inactive-state setup time is also referred to as recovery time.

### switching characteristics (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = 25°C			V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX‡			UNIT	
			'F299			SN54F299		SN74F299		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
f <sub>max</sub>			70	100		65		70	MHz	
t <sub>PLH</sub>	CLK	Q <sub>A</sub> ' or Q <sub>H</sub> '	3.2	6.6	9	2.7	10.5	3.2	10	ns
t <sub>PHL</sub>			2.7	6.1	8.5	2.2	10	2.7	9.5	
t <sub>PLH</sub>	CLK	Q <sub>A</sub> thru Q <sub>H</sub>	3.2	6.6	9	2.7	11	3.2	10	ns
t <sub>PHL</sub>			4.2	8.1	11	3.7	12.5	4.2	12	
t <sub>PHL</sub>	$\overline{\text{CLR}}$	Q <sub>A</sub> ' or Q <sub>H</sub> '	3.7	7.1	9.5	3.2	11.5	3.7	10.5	ns
		Q <sub>A</sub> thru Q <sub>H</sub>	5.7	10.6	14	5	15.5	5.7	15	
t <sub>PZH</sub>	$\overline{\text{OE1}}$ or $\overline{\text{OE2}}$	Q <sub>A</sub> thru Q <sub>H</sub>	2.7	5.6	8	2.2	10.5	2.7	9	ns
t <sub>PZL</sub>			3.2	6.6	10	2.7	12	3.2	11	
t <sub>PHZ</sub>	$\overline{\text{OE1}}$ or $\overline{\text{OE2}}$	Q <sub>A</sub> thru Q <sub>H</sub>	1.7	4.1	6	1.7	9	1.7	7	ns
t <sub>PLZ</sub>			1.2	3.6	5.5	1.2	7.5	1.2	6.5	

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 3: Load circuits and waveforms are shown in Section 1.

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