- **Synchronous Load**
- **Direct Overriding Clear**
- **Parallel-to-Serial Conversion**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

SN54F166A . . . J PACKAGE
SN74F166A . . . D OR N PACKAGE
(TOP VIEW)

SER	1	16	V_{CC}
A	2	15	SH/$\overline{LD}$
B	3	14	H
C	4	13	Q_H
D	5	12	G
CLK INH	6	11	F
CLK	7	10	E
GND	8	9	$\overline{CLR}$

SN54F166A . . . FK PACKAGE
(TOP VIEW)

Pins (top): A, SER, NC, V_{CC}, SH/$\overline{LD}$ — 3 2 1 20 19
Left side: B 4, C 5, NC 6, D 7, CLK INH 8
Right side: 18 H, 17 Q_H, 16 NC, 15 G, 14 F
Bottom pins: CLK 9, GND 10, NC 11, $\overline{CLR}$ 12, E 13
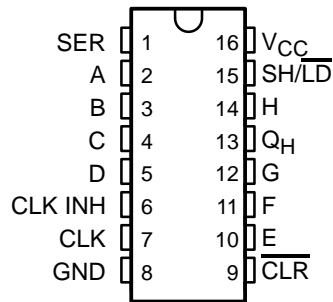
NC – No internal connection

description

The 'F166A parallel-in or serial-in, serial-out registers feature gated clock (CLK INH and CLK) inputs and an overriding clear ($\overline{CLR}$) input. The parallel-in or serial-in modes are established by the shift/load (SH/$\overline{LD}$) input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled, and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited.
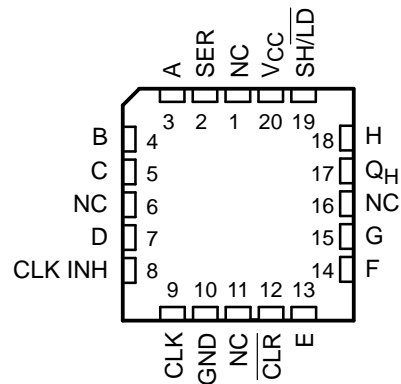
Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input positive OR gate, permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free-running, and the register can be stopped on command with the other clock input. The clock inhibit input should be changed to the high level only when the clock input is high. The direct clear ($\overline{CLR}$) overrides all other inputs, including the clock, and resets all flip-flops to zero.

The SN54F166A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F166A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS						INTERNAL OUTPUTS		OUTPUT
$\overline{CLR}$	SH/$\overline{LD}$	CLK INH	$\overline{CLR}$	SER	PARALLEL A . . . H	Q_A	Q_B	Q_H
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a . . . h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H†	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

† The CLK INH input was taken to the high level in a prior configuration when CLK was high.

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logic symbol†

Pin	Signal		
9	$\overline{\text{CLR}}$	R	SRG8
15	SH/$\overline{\text{LD}}$	M1 [SHIFT]	
		M2 [LOAD]	
6	CLK INH	≥1	
7	CLK		C3/1 →
1	SER	1, 3D	
2	A	2, 3D	
3	B	2, 3D	
4	C		
5	D		
10	E		
11	F		
12	G		
14	H		
13	Q_H		
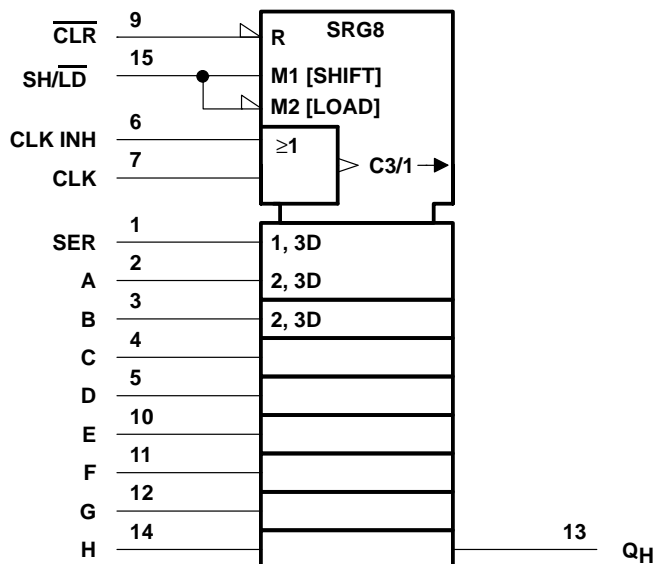
† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

logic symbol (positive logic)
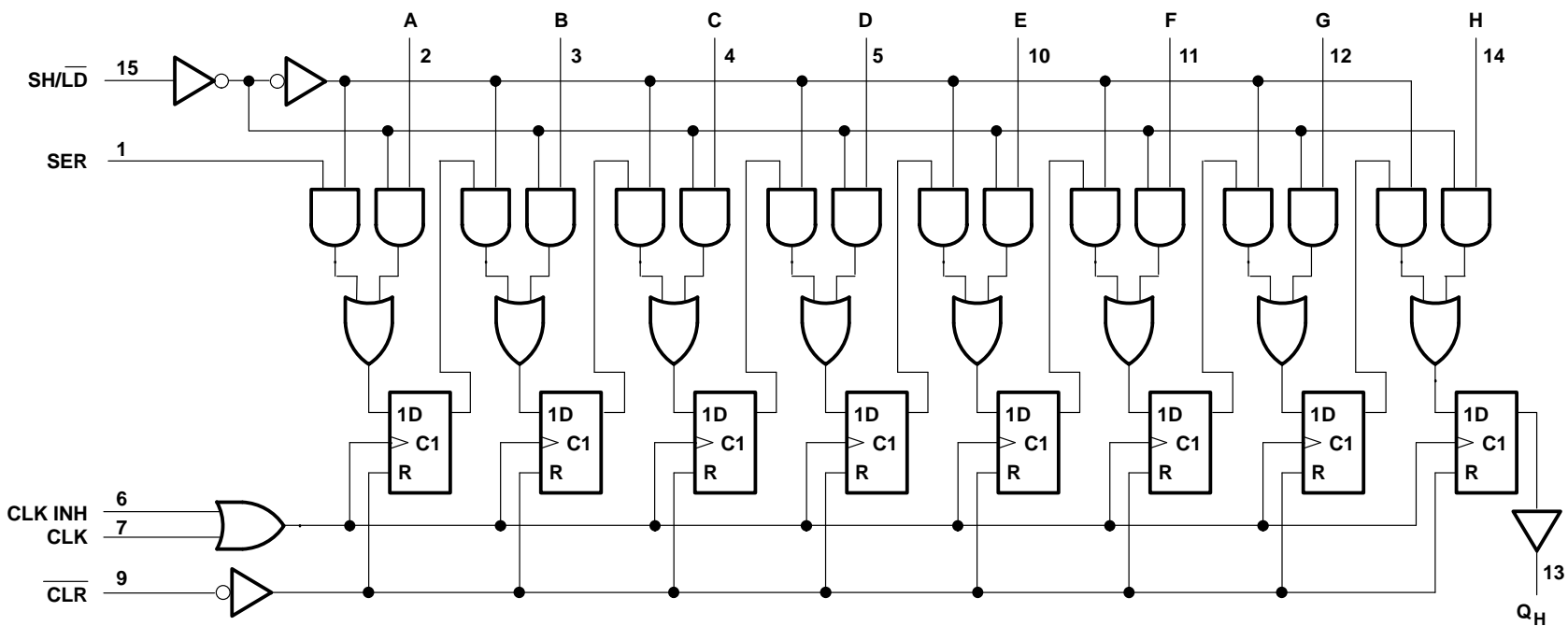
Pin numbers shown are for the D, J, and N packages.

typical clear, shift, load, inhibit, and shift operations
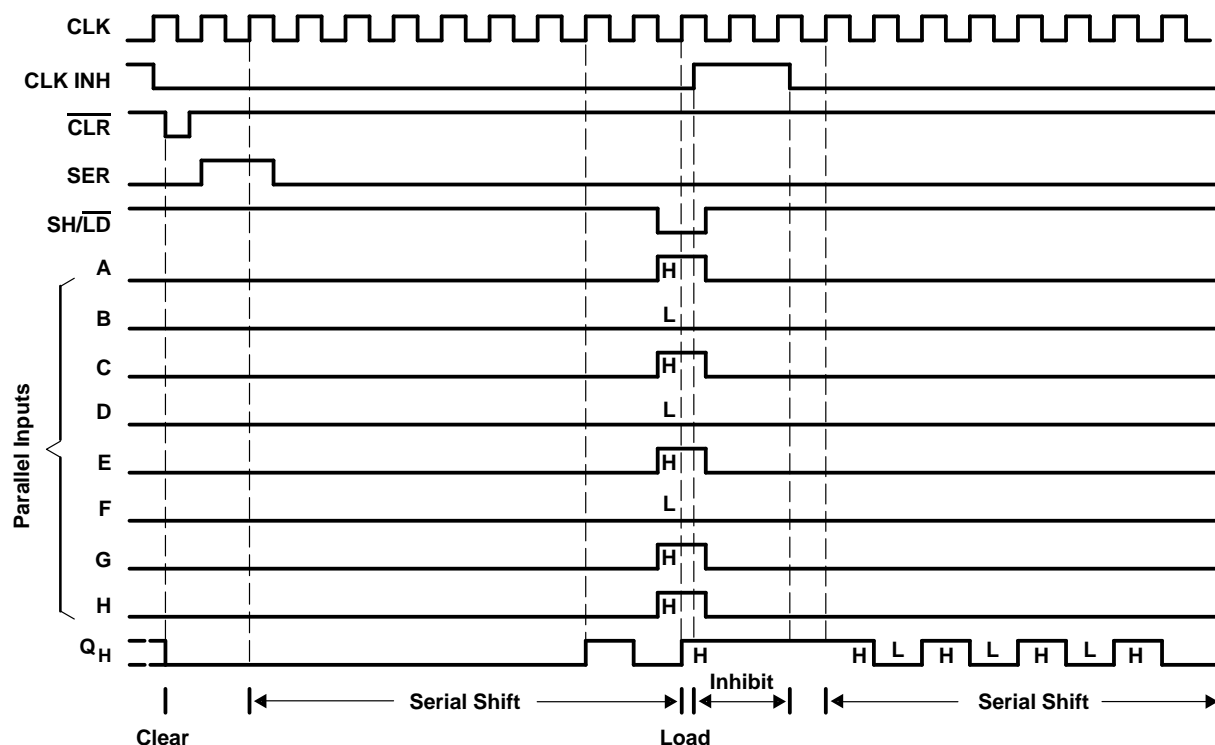
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... − 0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... − 1.2 V to 7 V
Input current range .... −30 mA to 5 mA
Voltage applied to any output in the high state, V_O .... − 0.5 V to V_{CC}
Current into any output in the low state, I_O .... 40 mA
Operating free-air temperature range: SN54F166A .... − 55°C to 125°C
                                       SN74F166A .... 0°C to 70°C
Storage temperature range .... − 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

		SN54F166A			SN74F166A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			− 18			− 18	mA
I_{OH}	High-level output current			− 1			− 1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	− 55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F166A			SN74F166A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = – 18 mA				– 1.2			– 1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = – 1 mA		2.5	3.4		2.5	3.4		V
	V_{CC} = 4.75 V, I_{OH} = – 1 mA					2.7			
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 20 mA			0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 0, V_I = 7 V				0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V, V_I = 2.7 V	Control inputs			40			40	μA
		Others			20			20	
I_{IL}	V_{CC} = 5.5 V, V_I = 0.5 V	Control inputs			– 40			– 40	μA
		Others			– 20			– 20	
I_{OS}‡	V_{CC} = 5.5 V, V_O = 0		– 60		– 150	– 60		– 150	mA
I_{CC}	V_{CC} = 5.5 V			43	70		43	70	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

timing characteristics

			V_{CC} = 5 V, T_A = 25°C		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX§				UNIT
			′F166A		SN54F166A		SN74F166A		
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	135			0	110	MHz
t_w	Pulse duration	$\overline{CLR}$ low	4		4		4		ns
		CLK high	4		4		4		
		CLK low	4		4		4		
t_{su}	Setup time before CLK↑	SH/$\overline{LD}$ high	2.5		2.5		2.5		ns
		SER	3.5		3.5		3.5		
		CLK INH low	2.5		2.5		2.5		
		A . . . H	4		4		4		
		$\overline{CLR}$ high	2.5		2.5		2.5		
t_h	Hold time after CLK↑	SH/$\overline{LD}$ high	1		1		1		ns
		SER	1.5		1.5		1.5		
		CLK INH low	1.5		1.5		1.5		
		A . . . H	1		1		1		

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX†				UNIT
			'F166A			SN54F166A		SN74F166A		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			135	175				110		MHz
t_{PHL}	$\overline{CLR}$	Q_H	4.8	6	7.1	4.2	13.4	4.4	8.3	ns
t_{PLH}	CLK	Q_H	4.6	5.9	7.1	4	9.4	4.2	8.2	ns
t_{PHL}			4.6	5.8	6.9	3.9	9.4	4.1	8	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ Load circuits and waveforms are shown in Section 1.

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