SDFS031A – D3693, JANUARY 1991 – REVISED OCTOBER 1993

D OR N PACKAGE High-Speed f_{max} of 100 MHz Typical (TOP VIEW) Parallel Asynchronous Load for Modulo-N Count Lengths 16 🛛 V_{CC} В Look-Ahead Circuitry Enhances Speed of 15 A QB 2 **Cascaded Counters** Q_A 14 CLR 3 Fully Synchronous in Count Modes DOWN 4 13 BO Package Options Include Plastic UP [12 CO 5 Small-Outline Packages and Standard QCL 11 LOAD 6 Plastic 300-mil DIPs Q_D 7 10 C 9 🛛 D GND [8 description

The SN74F193A is a synchronous, 4-bit binary up/down counter. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of either count/clock (UP or DOWN) input. The direction of the count is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the \overline{LOAD} input and entering the desired data at the data (D) inputs. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A high level applied to the clear (CLR) input forces all outputs to the low level. The clear function is independent of the count and load inputs.

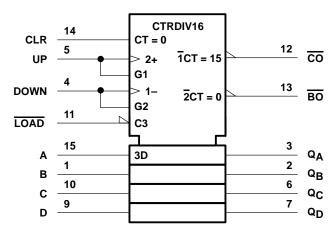
These counters were designed to be cascaded without the need for external circuitry. The borrow (\overline{BO}) output produces a low-level pulse while the count is zero (all Q outputs low) and the DOWN input is low. Similarly, the carry (\overline{CO}) output produces a low-level pulse while the count is 15 (all Q outputs high) and the UP input is low. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs, respectively, of the succeeding counter.

The SN74F193A is characterized for operation from 0°C to 70°C.



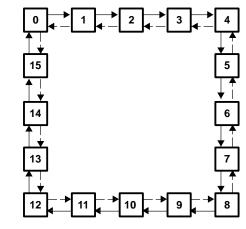
SDFS031A - D3693, JANUARY 1991 - REVISED OCTOBER 1993

logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

state diagram

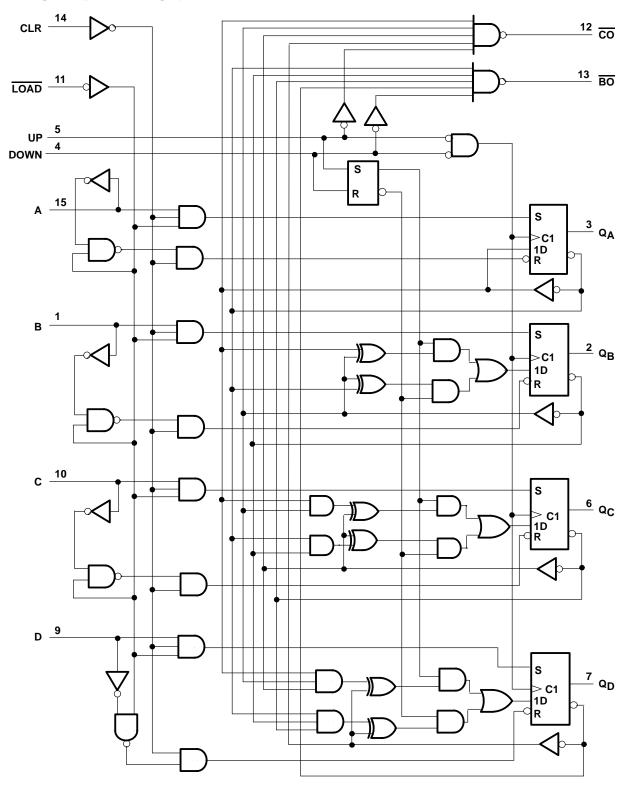


Count up \longrightarrow Count down $- \rightarrow$



SN74F193A SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTER WITH DUAL CLOCK AND CLEAR SDFS031A – D3693, JANUARY 1991 – REVISED OCTOBER 1993

logic diagram (positive logic)



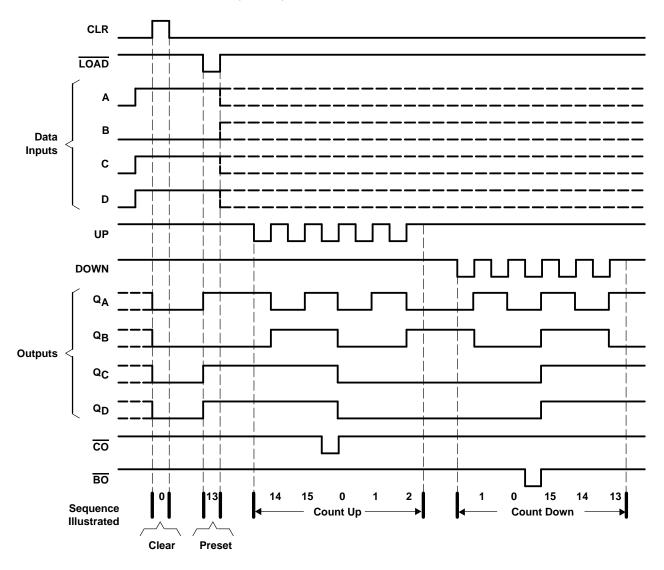


SDFS031A - D3693, JANUARY 1991 - REVISED OCTOBER 1993

typical clear, load, and count sequence

Illustrated below is the following sequence:

- 1. Clear outputs to zero
- 2. Load (preset) to binary thirteen
- 3. Count up to fourteen, fifteen (carry), zero, one, and two
- 4. Count down to one, zero (borrow), fifteen, fourteen, and thirteen





SDFS031A - D3693, JANUARY 1991 - REVISED OCTOBER 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	–1.2 V to 7 V
Input current range	– 30 mA to 5 mA
Voltage applied to any output in the high state	$\dots - 0.5$ V to V _{CC}
Current into any output in the low state	40 mA
Operating free-air temperature range	0 °C to 70 °C
Storage temperature range	– 55°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input-voltage ratings may be exceeded if the input-current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	V
VIH	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
Iк	Input clamp current			18	mA
ЮН	High-level output current			- 1	mA
IOL	Low-level output current			20	mA
TA	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	Т	TEST CONDITIONS			TYP‡	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	l _l = – 18 mA				- 1.2	V
VoH	$V_{CC} = 4.5 V,$	I _{OH} = – 1 mA		2.5	5 3.4		V
VOH	$V_{CC} = 4.75 \text{ V},$ $I_{OH} = -1 \text{ mA to } 3 \text{ mA}$	2.7			v		
VOL	$V_{CC} = 4.5 V,$	I _{OL} = 20 mA	I _{OL} = 20 mA		0.3	0.5	V
lı	V _{CC} = 5.5 V,	V _I = 7 V	V ₁ = 7 V			0.1	mA
Чн	$V_{CC} = 5.5 V,$	V _I = 2.7 V	V ₁ = 2.7 V			20	μΑ
l.,			UP			– 1.8	mA
lιL	V _{CC} = 5.5 V,	VI =0.5, v	Others			- 0.6	ША
IOS [§]	V _{CC} = 5.5 V,	$V_{O} = 0$		- 60		- 150	mA
lcc	V _{CC} = 5.5 V,	Outputs open			34	54	mA

[‡] All typical values are at V_{CC} = 5 V, $T_A = 25^{\circ}C$.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.



SDFS031A - D3693, JANUARY 1991 - REVISED OCTOBER 1993

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V _{CC} = 5 V, T _A = 25°C		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $T_A = \text{MIN to MAX}^{\dagger}$		UNIT			
			MIN	MAX	MIN	MAX				
fclock	Clock frequency		0	85	0	85	MHz			
t _w	Pulse duration	CLR high	4		4		ns			
		LOAD low	5.5		5.5					
		UP or DOWN high	4		4					
		UP or DOWN low	6		6					
t _{su}		Data before LOAD inactive	3.5		3.5					
	Setup time	CLR inactive before UP↑ or DOWN↑	5		5		ns			
		LOAD inactive before UP↑ or DOWN↑	7.5		7.5					
t _h	Hold time	Data after LOAD inactive	2.5		2.5		ns			

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CL RL	c = 5 V, = 50 pF, = 500 Ω, = 25°C	C _L = 50 p R _L = 500	5 V to 5.5 V, DF, Ω, to MAX [†]	UNIT
			MIN	TYP MAX	MIN	MAX	
fmax			85	100	85		MHz
^t PLH	UP or DOWN	CO or BO	2.5	8.5	2.5	9	ns
^t PHL	UP OF DOWN		3	8	3	9	115
^t PLH	UP or DOWN	Any Q	2.5	8.5	2.5	9	ns
^t PHL		Ally Q	5	12	5	13	115
^t PLH	A, B, C, or D	Any	2	7	1.5	8	ns
^t PHL	A, B, C, 01 D	Any Q	6	13.5	5	15	115
^t PLH	LOAD	AmirO	4.5	10	4	11	
^t PHL	LOAD	Any Q	5.5	12	5	13	ns
^t PHL		Any Q	5	11	5	12	
^t PLH	CLR	CO	6	12	5.5	13	ns
^t PHL	CLR	BO	5	11	5	12	ns
^t PLH		00 100	6	13.5	6	15	
^t PHL	LOAD	CO or BO	6	12.6	6	13.8	ns
^t PLH		CO or BO	5.5	13	5	14	
^t PHL	A, B, C, or D		4.5	12.5	4.5	13.5	ns

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. NOTE 2: Load circuits and waveforms are shown in Section 1.



IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1996, Texas Instruments Incorporated