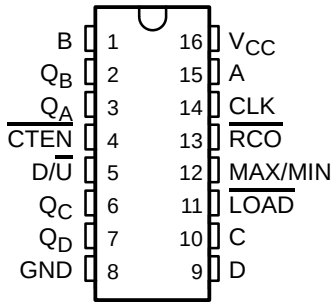
- **High-Speed f_{max} of 125 MHz Typical**
- **Single Down/Up Count Control Line**
- **Look-Ahead Circuitry Enhances Speed of Cascaded Counters**
- **Fully Synchronous in Count Modes**
- **Asynchronously Presettable With Load Control**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

D OR N PACKAGE
(TOP VIEW)



description

The SN74F190A is a synchronous, 4-bit decade reversible up/down counter. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

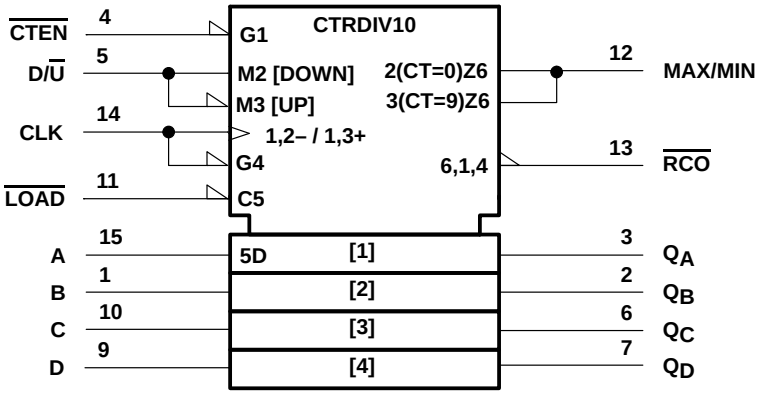
The outputs of the four flip-flops are triggered on a low-to-high-level transition of the clock (CLK) input if the enable ($\overline{CTEN}$) input is low. A high at $\overline{CTEN}$ inhibits counting. The direction of the count is determined by the level of the down/up (D/$\overline{U}$) input. When D/$\overline{U}$ is low, the counter counts up, and when D/$\overline{U}$ is high, it counts down.

This counter features a fully independent clock circuit. Changes at the control ($\overline{CTEN}$ and D/$\overline{U}$) inputs that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter is dictated solely by the condition meeting the stable setup and hold times. This counter is fully programmable; that is, it may be preset to any number between 0 and 9 by placing a low on the load input and entering the desired data at the data inputs. The output changes to agree with the data inputs independent of the level of the clock input. This feature allows the counter to be used as a modulo-N divider by simply modifying the count length with the preset inputs.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is minimum (0) counting down or maximum (9) counting up. The ripple-clock ($\overline{RCO}$) output produces a low-level output pulse under those same conditions, but only while the clock input is low. The counter can easily be cascaded by feeding the ripple-clock output to the enable input of the succeeding counter if parallel clocking is used or to the clock input if parallel enabling is used. The maximum/minimum count (MAX/MIN) output can be used to accomplish look-ahead for high speed operation.

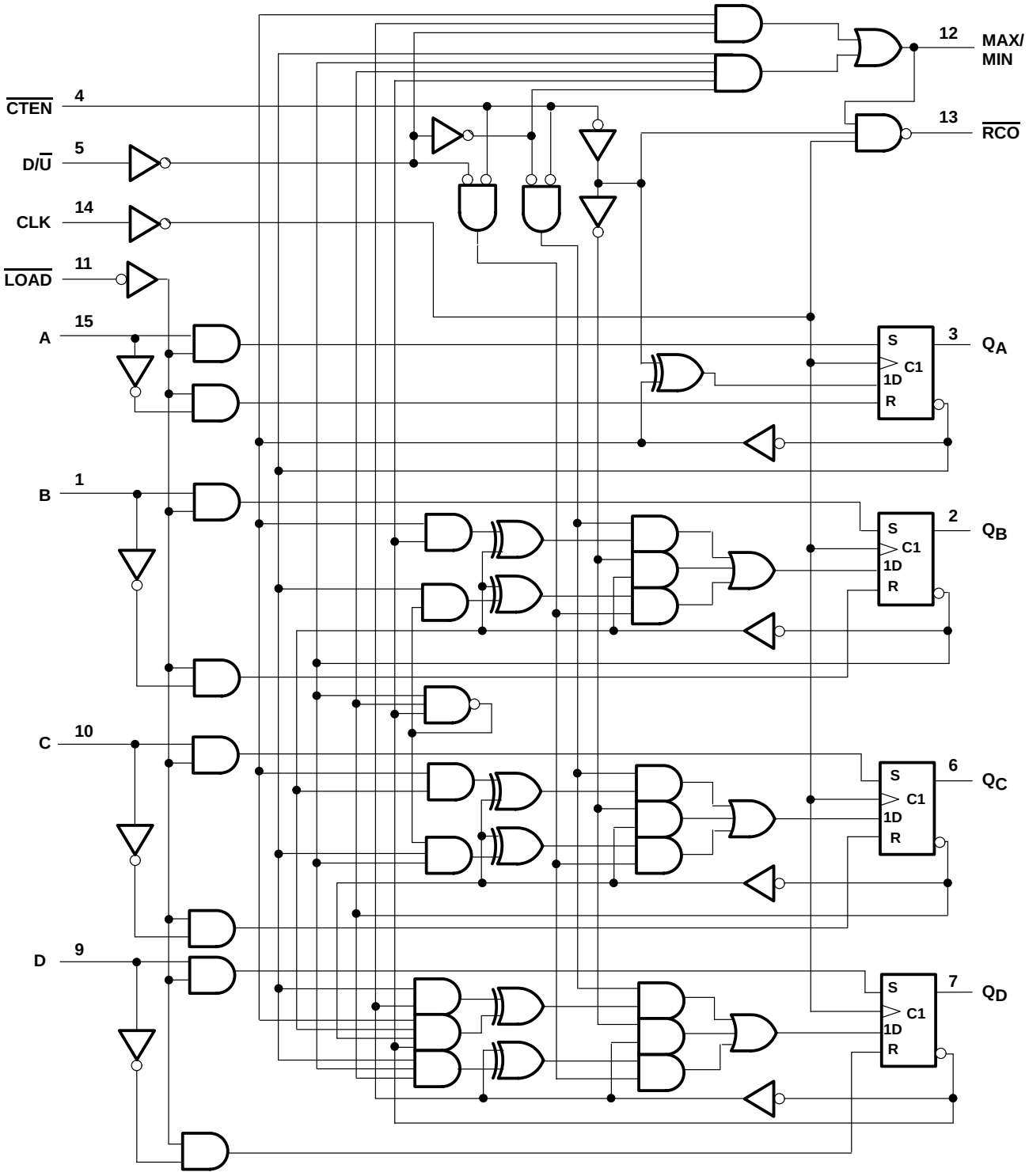
The SN74F190A is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

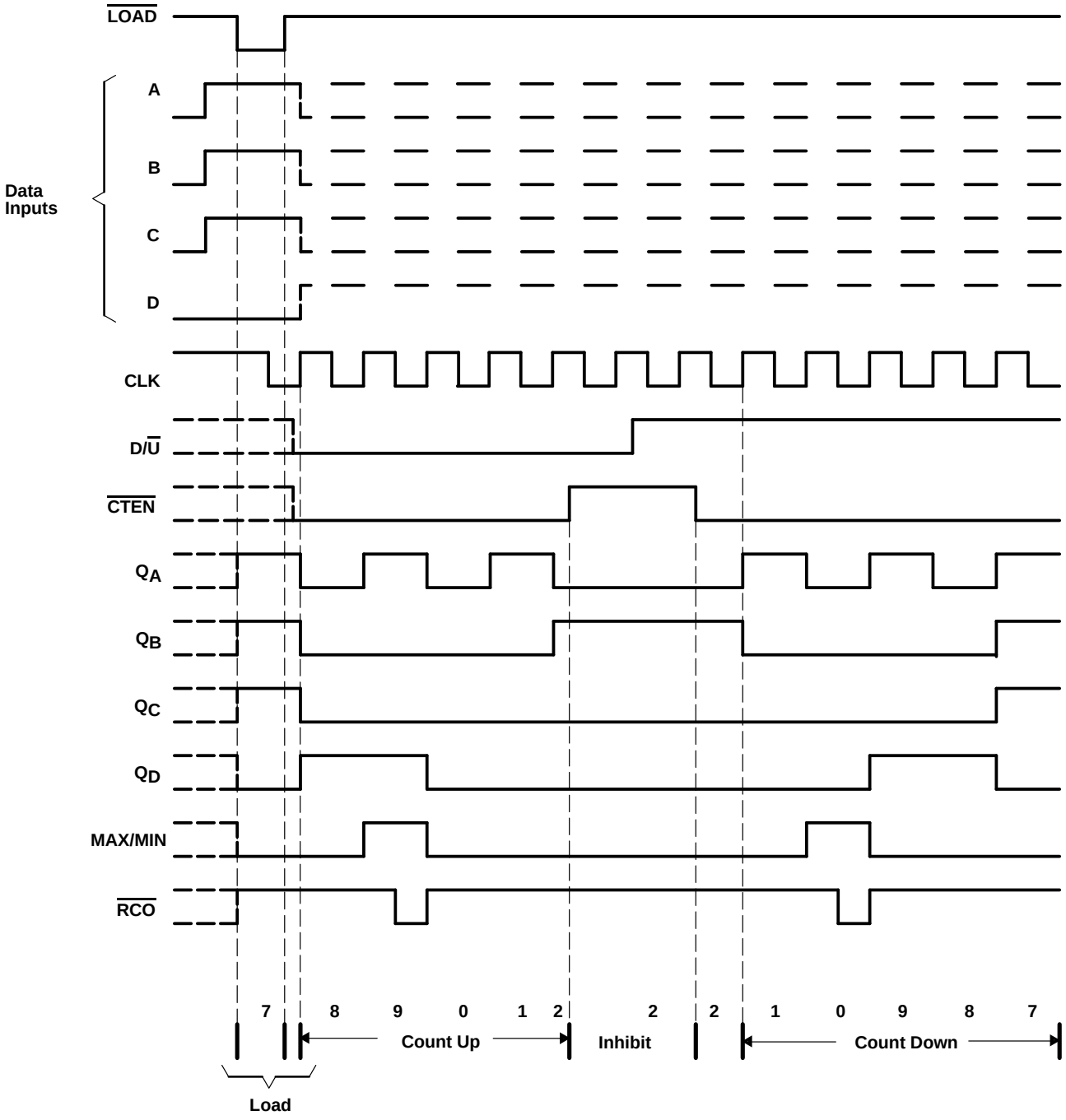
logic diagram (positive logic)



typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to BCD seven
2. Count up to eight, nine (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . – 0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –1.2 V to 7 V
Input current range . . . . . – 30 mA to 5 mA
Voltage applied to any output in the high state . . . . . – 0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range . . . . . 0 °C to 70 °C
Storage temperature range . . . . . – 55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input-voltage ratings may be exceeded if the input-current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			18	mA
I_{OH}	High-level output current			– 1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = – 18 mA				– 1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = – 1 mA		2.5	3.4		V
	V_{CC} = 4.75 V,	I_{OH} = – 1 mA		2.7			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA			0.3	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V				0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V				20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V	$\overline{CTEN}$			– 1.8	mA
			Others			– 0.6	
I_{OS}§	V_{CC} = 5.5 V,	V_O = 0		– 60		– 150	mA
I_{CC}	V_{CC} = 5.5 V,	Outputs open			40	55	mA

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

timing requirements

			V_{CC} = 5 V, T_A = 25°C		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX†		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	90	0	90	MHz
t_w	Pulse duration	$\overline{LOAD}$ low	6		6		ns
		CLK high	4		4		
		CLK low	7		7		
t_{su}	Setup time	Data before $\overline{LOAD}$↑	4		4		ns
		$\overline{CTEN}$ before CLK↑	6.5		6.5		
		D/$\overline{U}$ before CLK↑	15		15		
		$\overline{LOAD}$ inactive before CLK↑	10		10		
t_h	Hold time	Data after $\overline{LOAD}$↑	2		2		ns
		$\overline{CTEN}$ after CLK↑	1		1		
		D/$\overline{U}$ after CLK↑	0		0		

switching characteristics (see Note)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX †		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}			90			90		MHz
t_{PLH}	CLK	Any Q	2.5	4.8	8	2	8.5	ns
t_{PHL}			5	7	11.5	5	12	
t_{PLH}	CLK	MAX/MIN	6.5	9.4	12.5	6	13	ns
t_{PHL}			6	8.9	11	6	12	
t_{PLH}	CLK	$\overline{RCO}$	2.5	5.2	7.5	2	8	ns
t_{PHL}			3	4.8	7.5	2.5	8	
t_{PLH}	$\overline{CTEN}$	$\overline{RCO}$	2	5.7	7	2	7.8	ns
t_{PHL}			3	5	7.5	3	8	
t_{PLH}	D/$\overline{U}$	$\overline{RCO}$	8	13	16	8	17.8	ns
t_{PHL}			4.5	8.1	10.5	4	11	
t_{PLH}	D/$\overline{U}$	MAX/MIN	4	7.9	9.8	3	11.3	ns
t_{PHL}			3	7.5	9.5	3	10	
t_{PLH}	A, B, C, or D	Any Q	2	4.7	7	1.5	7.5	ns
t_{PHL}			6.5	8.9	12	6.5	13	
t_{PLH}	A, B, C, or D	MAX/MIN	5.5	10.5	13.6	5	15.4	ns
t_{PHL}			6.5	10	13	6	14	
t_{PLH}	A, B, C, or D	$\overline{RCO}$	6	15	18.6	6	21.1	ns
t_{PHL}			6	9.5	13.5	6	15	
t_{PLH}	$\overline{LOAD}$	Any Q	4.5	7.7	9.8	4	11.4	ns
t_{PHL}			5.5	9.9	12.1	5	13.1	
t_{PLH}	$\overline{LOAD}$	MAX/MIN	5.5	12.3	15.2	5.5	17	ns
t_{PHL}			6	11.7	14	6	15.6	
t_{PLH}	$\overline{LOAD}$	$\overline{RCO}$	8.5	16.8	19.9	8.5	23.2	ns
t_{PHL}			7.5	11.6	14	7	15.2	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 2: Load circuits and waveforms are shown in Section 1.

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