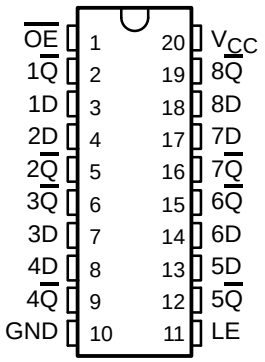
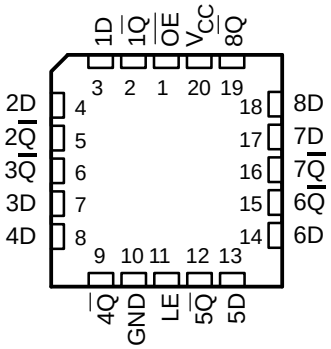
- **8 Latches in a Single Package**
- **3-State Bus-Driving Inverting Outputs**
- **Full Parallel Access for Loading**
- **Buffered Output-Enable Inputs**
- **P-N-P Inputs Reduce DC Loading on Data Lines**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

SN54AS533 . . . J PACKAGE
SN74AS533A . . . DW OR N PACKAGE
(TOP VIEW)



SN54AS533 . . . FK PACKAGE
(TOP VIEW)



description

These 8-bit D-type transparent latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

While the latch-enable (LE) input is high, the $\overline{Q}$ outputs follow the complements of the data (D) inputs. When LE is taken low, the $\overline{Q}$ outputs are latched at the inverse level set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

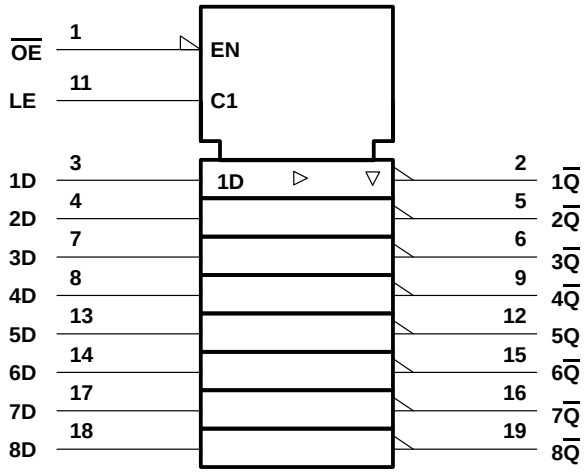
The output-enable ($\overline{OE}$) input does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54AS533 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AS533A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each latch)

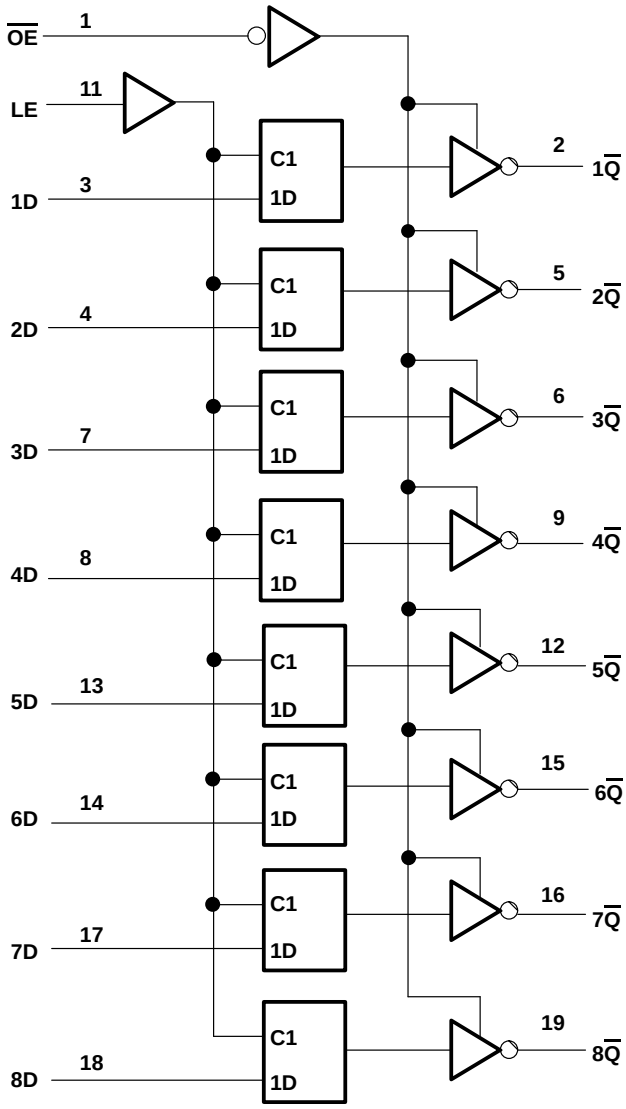
INPUTS			OUTPUT
$\overline{OE}$	LE	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I . . . . . –1.2 V to 7 V
Voltage applied to disabled 3-state output, V_O . . . . . –0.5 V to 5.5 V
Operating free-air temperature range: SN54AS533 . . . . . –55°C to 125°C
SN74AS533A . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54AS533			SN74AS533A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			–12			–15	mA
I_{OL}	Low-level output current			32			48	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS533			SN74AS533A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = –18 mA				–1.5			–1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V, I_{OH} = – 2 mA		V_{CC}–2			V_{CC}–2			V
	V_{CC} = 4.5 V, I_{OH} = –12 mA		2.4	3.2					
	V_{CC} = 4.5 V, I_{OH} = – 15 mA					2.4	3.3		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 32 mA			0.29	0.5				V
	V_{CC} = 4.5 V, I_{OL} = 48 mA						0.34	0.5	
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V				50			50	µA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.4 V				–50			–50	µA
I_I	V_{CC} = 5.5 V, V_I = 7 V				0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V, V_I = 2.7 V				20			20	µA
I_{IL}	V_{CC} = 5.5 V, V_I = 0.5 V			–0.02	–0.5		–0.02	–0.5	mA
I_O‡	V_{CC} = 5.5 V, V_O = 2.25 V		–30		–112	–30		–112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		62	100		62	100	mA
		Outputs low		64	100		64	100	
		Outputs disabled		71	110		71	110	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

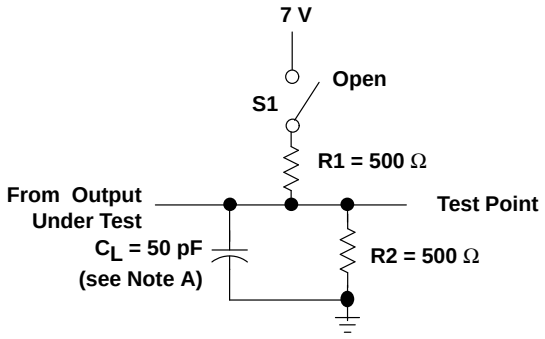
timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		SN54AS533		SN74AS533A		UNIT
		MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	3		2		ns
t_{su}	Setup time, data before LE↓	2		2		ns
t_h	Hold time, data after LE↓	3		3		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54AS533		SN74AS533A		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	4	10	4	7.5	ns
t_{PHL}			4	8	4	7	
t_{PLH}	LE	Q	5	11	5	9	ns
t_{PHL}			4	8.5	4	8	
t_{PZH}	OE	Q	2	7.5	4	6.5	ns
t_{PZL}			4	10.5	4	9.5	
t_{PHZ}	OE	Q	2	7.5	2	6.5	ns
t_{PLZ}			3	8	3	7	

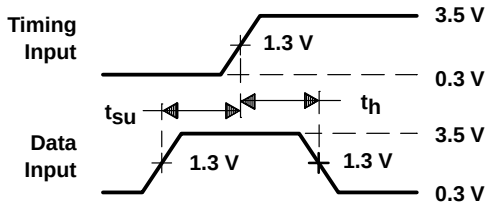
PARAMETER MEASUREMENT INFORMATION



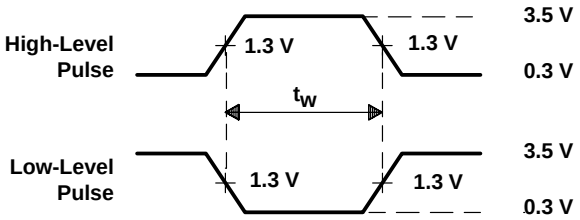
LOAD CIRCUIT FOR 3-STATE OUTPUTS

SWITCH POSITION TABLE

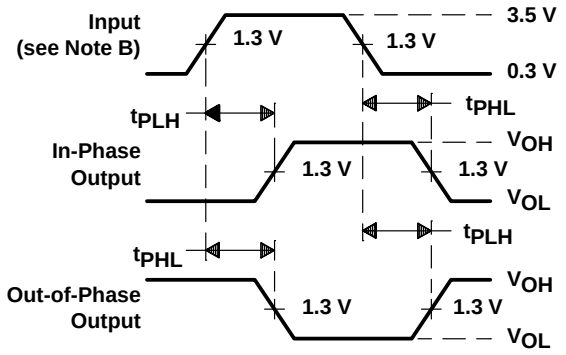
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



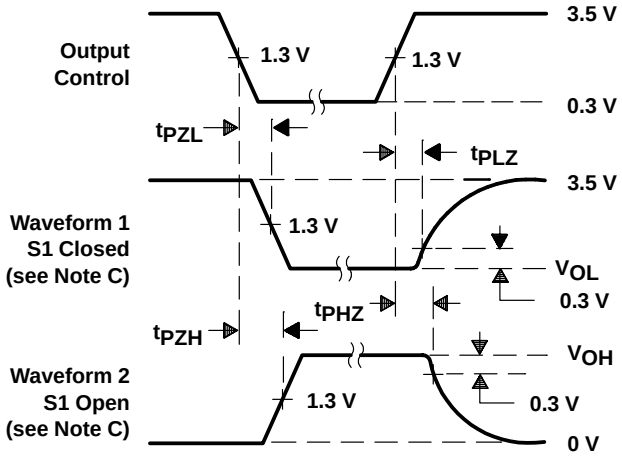
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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