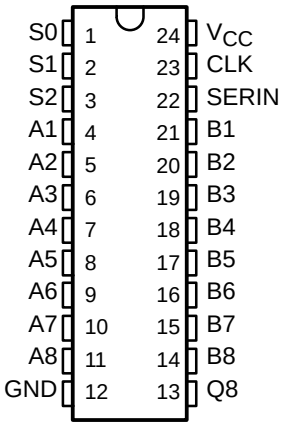
- **Package Options Include Plastic Small Outline Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Buffered 3-State Outputs Drive Bus Lines Directly**
- **Cascaded to n-Bits**
- **Eight Selectable Transceiver/Port Functions:**
  - **A to B or B to A**
  - **Register to A or Register to B**
  - **Shifted to A or Shifted to B**
  - **Off-Line Shifts (A and B Ports in High-Impedance State)**
  - **Register Clear**
- **Particularly Suitable for Use in Signature Analysis Circuitry**
- **Serial Register Provides:**
  - **Parallel Storage of Either A or B Input Data**
  - **Serial Transmission of Data from Either A or B Port**
- **Dependable Texas Instruments Quality and Reliability**

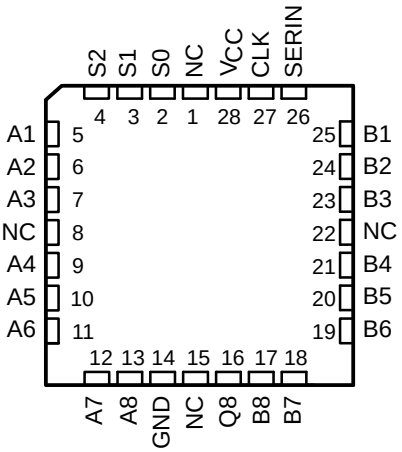
SN54AS877 . . . JT PACKAGE
SN74AS877 . . . DW OR NT PACKAGE

(TOP VIEW)



SN54AS877 . . . JT PACKAGE
SN74AS877 . . . DW OR NT PACKAGE

(TOP VIEW)



NC – No internal connection

description

The ’AS877 features two 8-bit I/O ports (A1-A8 and B1-B8), an 8-bit parallel-load, serial-in, parallel-out shift register, and control logic. With these features, this device is capable of performing eight selectable transceiver or port functions, depending on the state of the three select lines S0, S1, and S2. These functions include: transferring data from port A to port B or vice versa (i.e., the transceiver function), transferring data from the register to either port, serial shifting data to either port, performing off-line shifts (with A and B ports in high-impedance state), and clearing the register. Synchronous parallel loading of the internal register can be accomplished from either port on the positive transition of the clock while serially shifting data in via the SERIN input. The ’AS877 is ideally suited for applications needing signature-analysis circuitry to enhance system verification and/or fault analysis. All serial data is shifted right. All outputs are buffer-type outputs designed specifically to drive bus lines directly and all are 3-state except for Q8, which is a totem-pole output.

The SN54AS877 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AS877 is characterized for operation from 0°C to 70°C.

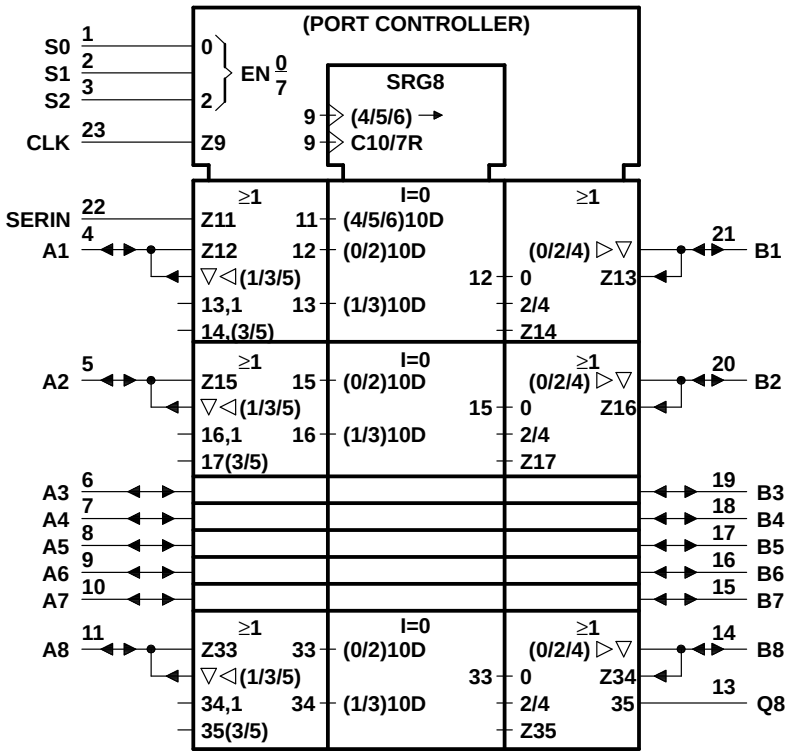
FUNCTION TABLE

MODE			CLOCK	SERIN	A1	Q1	B1	A2	Q2	B2	A3	Q3	B3	A4	Q4	B4	A5	Q5	B5	A6	Q6	B6	A7	Q7	B7	A8	Q8	B8	PORT FUNCTION
S2	S1	S0																											
L	L	L	H or L	X	Z	Q_n	A1	Z	Q_n	A2	Z	Q_n	A3	Z	Q_n	Q4	Z	Q_n	A5	Z	Q_n	Q6	Z	Q_n	Q7	Z	Q_n	A8	A To B
L	L	L	↑	X	Z	A1	A1	Z	A2	A2	Z	A3	A3	Z	A4	Q4	Z	Q5	A5	Z	A6	Q6	Z	A7	Q7	Z	A8	A8	
L	L	H	H or L	X	B1	Q_n	Z	B2	Q_n	Z	B3	Q_n	Z	B4	Q_n	Z	B5	Q_n	Z	B6	Q_n	Z	B7	Q_n	Z	B8	Q_n	Z	B To A
L	L	H	↑	X	B1	B1	Z	B2	B2	Z	B3	B3	Z	B4	B4	Z	B5	B5	Z	B6	B6	Z	B7	B7	Z	B8	B8	Z	
L	H	L	H or L	X	X	Q_n	Q1	X	Q_n	Q2	X	Q_n	Q3	X	Q_n	Q4	X	Q_n	Q5	X	Q_n	Q6	X	Q_n	Q7	X	Q_n	Q8	Q_N To B_N
L	H	L	↑	X	Z	A1	A1	Z	A2	A2	Z	A3	A3	Z	A4	A4	Z	A5	A5	Z	A6	A6	Z	A7	A7	Z	A8	A8	
L	H	H	H or L	X	Q1	Q_n	X	Q2	Q_n	X	Q3	Q_n	Z	Q4	Q_n	Z	Q5	Q_n	X	Q6	Q_n	Z	Q7	Q_n	Z	Q8	Q_n	X	Q_N To A_N
L	H	H	↑	X	B1	B1	Z	B2	B2	Z	B3	B3	Z	B4	B4	Z	B5	B5	Z	B6	B6	Z	B7	B7	Z	B8	B8	Z	
H	L	L	H or L	X	Z	Q_n	Q1	Z	Q_n	Q2	Q3	Q_n	Q3	Z	Q_n	Q4	Z	Q_n	Q5	Z	Q_n	Q6	Z	Q_n	Q7	Z	Q_n	Q8	Shift
H	L	L	↑	H	Z	H	H	Z	Q1	Q1	Q2	Q2	Q2	Z	Q3	Q3	Z	Q4	Q4	Z	Q5	Q5	Z	Q6	Q6	Z	Q7	Q7	To
H	L	L	↑	L	Z	L	L	Z	Q1	Q1	Q2	Q2	Q2	Z	Q3	Q3	Z	Q4	Q4	Z	Q5	Q5	Z	Q6	Q6	Z	Q7	Q7	B
H	L	H	H or L	X	Q1	Q_n	Z	Q2	Q_n	Z	Q3	Q_n	Z	Q4	Q_n	Z	Q5	Q_n	Z	Q6	Q_n	Z	Q7	Q_n	Z	Q8	Q_n	Z	Shift
H	L	H	↑	H	H	H	Z	Q1	Q1	Z	Q2	Q2	Z	Q3	Q3	Z	Q4	Q4	Z	Q5	Q5	Z	Q6	Q6	Z	Q7	Q7	Z	To
H	L	H	↑	L	L	L	Z	Q1	Q1	Z	Q2	Q2	Z	Q3	Q3	Z	Q4	Q4	Z	Q5	Q5	Z	Q6	Q6	Z	Q7	Q7	Z	A
H	H	L	H or L	X	Z	Q_n	Z	Z	Q_n	Z	Z	Q_n	Z	Z	Q_n	Q4	Z	Q_n	Z	Z	Q_n	Q6	Z	Q_n	Q7	Z	Q_n	Z	
H	H	L	↑	H	Z	H	Z	Z	Q1	Z	Z	Q2	Z	Z	Q3	Q3	Z	Q4	Z	Z	Q5	Q5	Z	Q6	Q6	Z	Q7	Z	Shift
H	H	L	↑	L	Z	L	Z	Z	Q1	Z	Z	Q2	Z	Z	Q3	Q3	Z	Q4	Z	Z	Q5	Q5	Z	Q6	Q6	Z	Q7	Z	
H	H	H	H or L	X	Z	Q_n	Z	Z	Q_n	Z	Z	Q_n	Z	Z	Q_n	Z	Z	Q_n	Z	Z	Q_n	Z	Z	Q_n	Z	Z	Q_n	Z	Clear
H	H	H	↑	H	Z	H	Z	Z	L	Z	Z	L	Z	Z	L	Z	Z	L	Z	Z	L	Z	Z	L	Z	Z	L	Z	

n = level Of Q_n(n = 1, 2 . . . 8) established on most recent transition of CLK. Q1 thru Q8 are the shift register outputs; only Q8 is available externally. The double inversions that take place as data travels from port to port are ignored in this table.

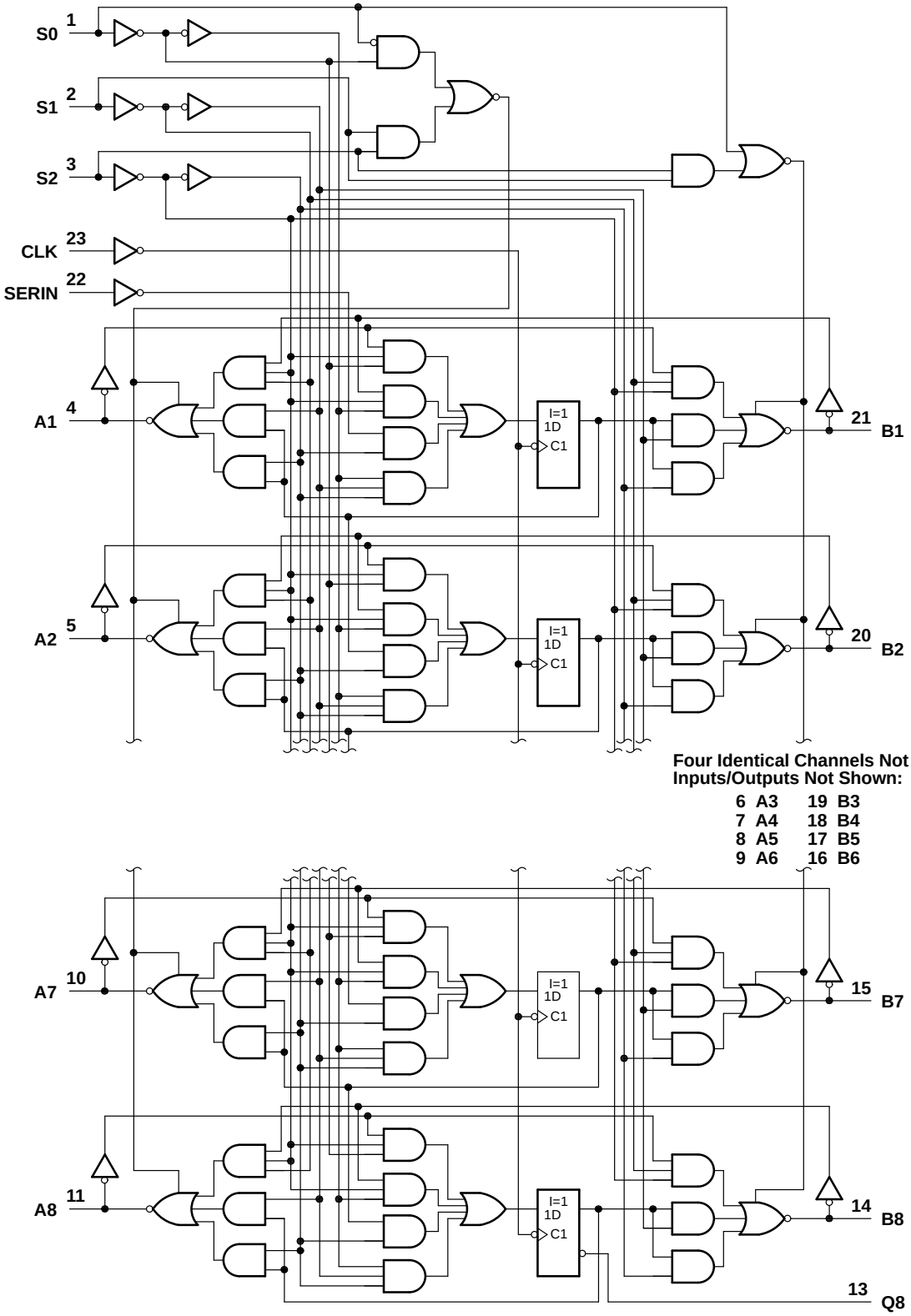
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

logic symbol †



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic)



Four Identical Channels Not Shown:
Inputs/Outputs Not Shown:

6	A3	19	B3
7	A4	18	B4
8	A5	17	B5
9	A6	16	B6

Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over free-air temperature range

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS877 . . . . . −55°C to 125°C
SN74AS877 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS877			SN74AS877			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level input voltage	A1-A8, B1-B8			−12			−15	mA
		Q8			−2			−2	
I_{OL}	Low-level input voltage	A1-A8, B1-B8			32			48	mA
		Q8			20			20	
f_{clock}	Clock frequency		0		45	0		50	MHz
t_w	Pulse duration, CLK		11			10			ns
t_{su}	Setup time before CLK↑	A1-A8, B1-B8 SERIN	5.5			5.5			ns
		S0, S1, S2	5.5			5.5			
t_h	Hold time, data after CLK↑	A1-A8, B1-B8 SERIN	0			0			ns
		S0, S1, S2	0			0			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS877			SN74AS877			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}	A1-A8	V_{CC} = 4.5 V,	I_{OH} = –12 mA	2	3.2					V
	B1-B8	V_{CC} = 4.5 V,	I_{OH} = –15 mA				2	3.3		
	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –2 mA	V_{CC}–2			V_{CC}–2			
V_{OL}	All outputs	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
	except Q8	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
	Q8	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.25	0.5		0.25	0.5	
I_I	S0, S1, S2	V_{CC} = 5.5 V,	V_I = 7 V			0.3			0.3	mA
	CLK and SERIN					0.1			0.1	
	A1-A8, B1-B8	V_{CC} = 5.5 V,	V_I = 5.5 V			0.2			0.2	
I_{IH}	S0, S1, S2	V_{CC} = 5.5 V,	V_I = 2.7 V			60			60	µA
	CLK and SERIN					20			20	
	A1-A8, B1-B8‡					70			70	
I_{IL}	S0, S1, S2	V_{CC} = 5.5 V,	V_I = 0.4 V			–1			–1	mA
	CLK and SERIN					–0.5			–0.5	
	A1-A8, B1-B8					–0.75			–0.75	
I_O§	Except Q8	V_{CC} = 5.5 V,	V_O = 2.25 V	–30		–112	–30		–112	mA
	Q8			–20		–112	–20		–112	
I_{CC}		V_{CC} = 5.5 V			136	220		136	220	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the output currents I_{OZH} and I_{OZL}, respectively.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

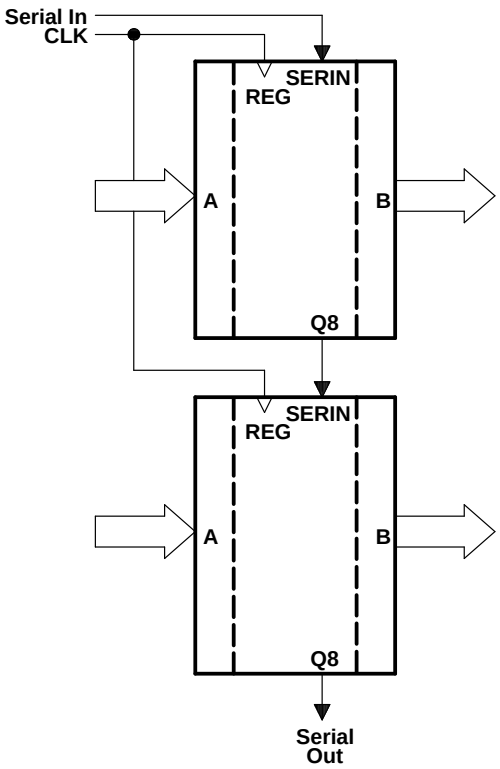
switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS877		SN74AS877		
			MIN	MAX	MIN	MAX	
f_{max}			45		50		MHz
t_{PLH}	Any A port	Any B port	2	8.5	2	7	ns
t_{PHL}			3	10.5	3	9	
t_{PLH}	Any B port	Any A port	2	9	2	7.5	ns
t_{PHL}			3	10.5	3	9	
t_{PLH}	S0, S1, S2 †	Any A or B port	2	11.5	2	10	ns
t_{PHL}			3	9.5	3	8	
t_{PLH}	CLk	Any A or B port	2	11	2	9	ns
t_{PHL}			3	13	3	11.5	
t_{PLH}	CLK	QB	2	10.5	2	8	ns
t_{PHL}			3	10	3	8.5	
t_{PHZ}	S0, S1, S2 †	Any A or B port	2	7.5	2	6.5	ns
t_{PLZ}			3	13	3	10.5	
t_{PZH}			2	9	2	7	ns
t_{PZL}			3	11.5	3	9.5	

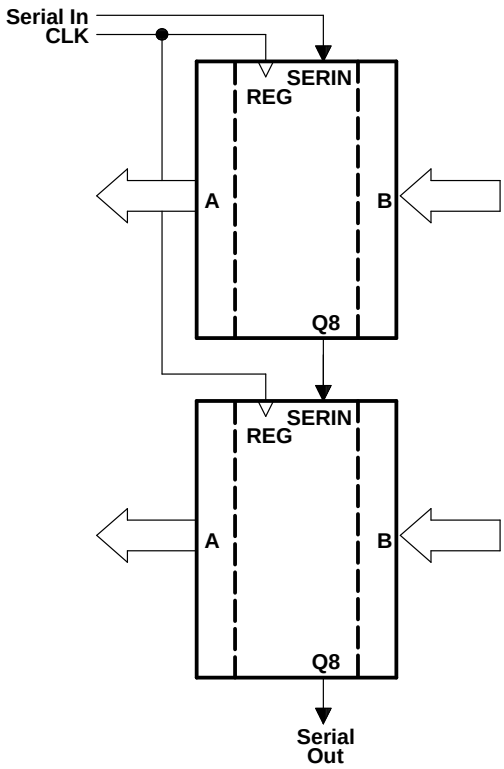
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.
† The positive transition of S2 will cause low-level data at the A output Bus or stored in the shift register to be invalid for 12 ns.

TYPICAL APPLICATION DATA

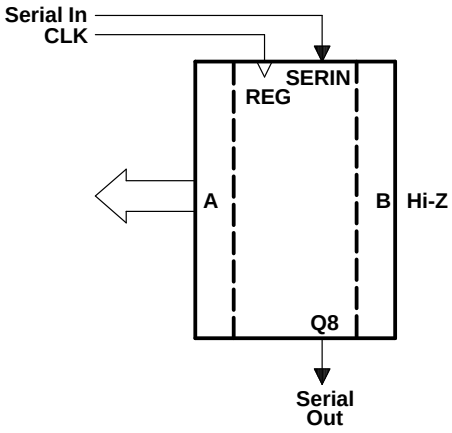
BUS A TO BUS B OR SERIAL TRANSMISSION



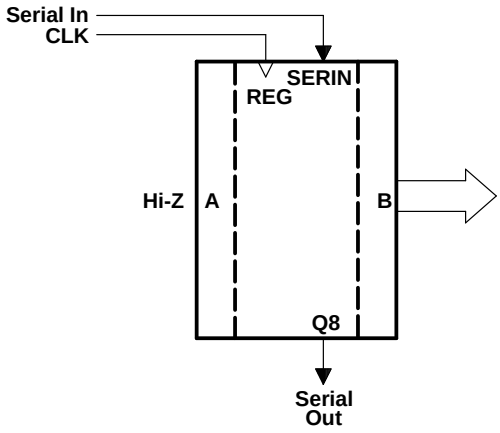
BUS B TO BUS A OR SERIAL TRANSMISSION



SERIAL IN TO A PORT



SERIAL IN TO B PORT



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.