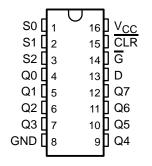
- 8-Bit Parallel-Out Storage Register Performs Serial-to-Parallel Conversion With Storage
- Asynchronous Parallel Clear
- Active-High Decoder
- Enable/Disable Input Simplifies Expansion
- Expandable for n-Bit Applications
- Four Distinct Functional Modes
- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

description

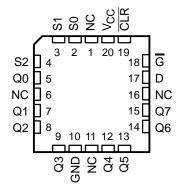
These 8-bit addressable latches are designed for general-purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and active-high decoders or demultiplexers. They are multifunctional devices capable of storing single-line data in eight addressable latches and being a 1-of-8 decoder or demultiplexer with active-high outputs.

Four distinct modes of operation are selectable by controlling the clear (\overline{CLR}) and enable (\overline{G}) inputs as shown in the function table. In the addressable-latch mode, data at the data-in terminal is written into the addressed latch. The

SN54ALS259 . . . J PACKAGE SN74ALS259 . . . D OR N PACKAGE (TOP VIEW)



SN54ALS259 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

addressed latch follows the data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latches, \overline{G} should be held high (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode, the addressed output follows the level of the D input with all other outputs low. In the clear mode, all outputs are low and unaffected by the address and data inputs.

The SN54ALS259 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ALS259 is characterized for operation from 0°C to 70°C.

Function Tables

FUNCTION

INPUTS CLR G		OUTPUT OF ADDRESSED	EACH OTHER	FUNCTION			
		LATCH	OUTPUT	FUNCTION			
Н	L	D	Q _{iO}	Addressable latch			
Н	Н	Q _{iO}	Q _{iO}	Memory			
L	L	D	L	8-line demultiplexer			
L	Н	L	L	Clear			

D = the level at the data input.

 Q_{iO} = the level of Q_i (i = Q, 1, . . . 7 as appropriate) before the indicated steady-state input conditions were established.

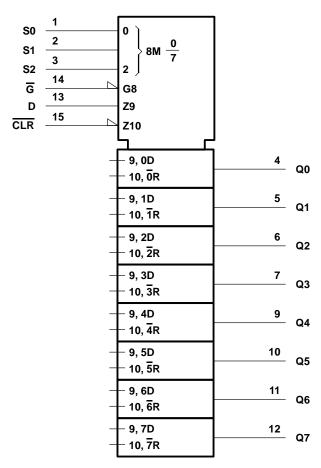


Function Tables (Continued)

LATCH SELECTION

SEL	ECT INP	LATCH			
S2	S1	S0	ADDRESSED		
L	L	L	0		
L	L	Н	1		
L	Н	L	2		
L	Н	Н	3		
Н	L	L	4		
Н	L	Н	5		
Н	Н	L	6		
Н	Н	Н	7		

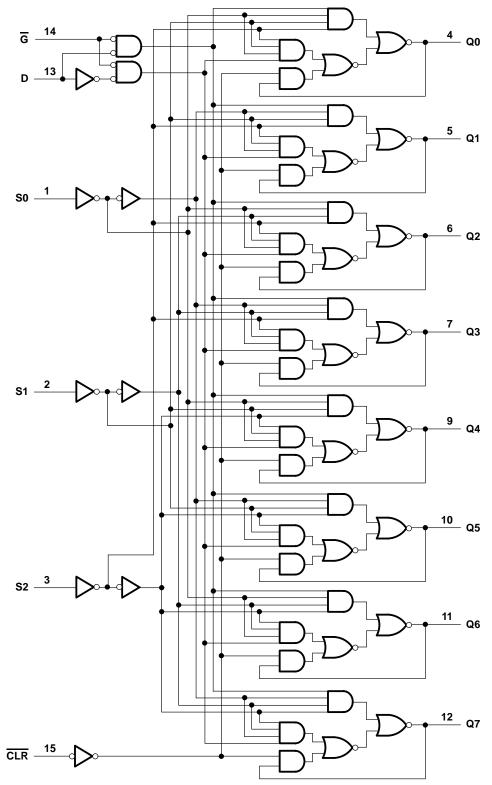
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, J, and N packages.



logic diagram (positive logic)



Pin numbers shown are for the D, J, and N packages.



SDAS217A - DECEMBER 1982 - REVISED DECEMBER 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC}	7 V
Input voltage, V _I	7 V
Operating free-air temperature range, T _A : SN54ALS259	-55°C to 125°C
SN74ALS259	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

			SN	SN54ALS259		SN74ALS259			UNIT	
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V	
V_{IH}	High-level input voltage		2			2			V	
V _{IL}	/ _{IL} Low-level input voltage				0.7			0.8	V	
IOH	H High-level output current				-0.4			-0.4	mA	
lOL	Low-level output current				4			8	mA	
, ,	Pulse duration	G low	20			15			ns	
t _W	r dise duration	CLR low	10			10			115	
	Setup time	Data before G↑	20			15				
t _{su}	Setup time	Address before G↑	20			15			ns	
t _h Hold tin	Hold time	Data after G↑	0			0			no	
	noid time	Address after G↑	0			0			ns	
TA	Operating free-air temperature		-55		125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS		SN	SN54ALS259			SN74ALS259		
PARAMETER			MIN	TYP [‡]	MAX	MIN	TYP‡	MAX	UNIT
VIK	$V_{CC} = 4.5 \text{ V},$	$I_{I} = -18 \text{ mA}$			-1.5			-1.5	٧
Voн	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -2	2		V _{CC} -2	2		V
Voi	V _{CC} = 4.5 V	$I_{OL} = 4 \text{ mA}$		0.25	0.4		0.25	0.4	V
V _{OL}		$I_{OL} = 8 \text{ mA}$					0.35	0.5	٧
lį	$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA
lН	$V_{CC} = 5.5 V$,	V _I = 2.7 V			20			20	μΑ
Ι _{ΙL}	$V_{CC} = 5.5 V$,	V _I = 0.4 V			-0.1			-0.1	mA
ΙΟ [§]	$V_{CC} = 5.5 V$,	V _O = 2.25 V	-20		-112	-30		-112	mA
lcc	V _{CC} = 5.5 V			14	22		14	22	mA

[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.



[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

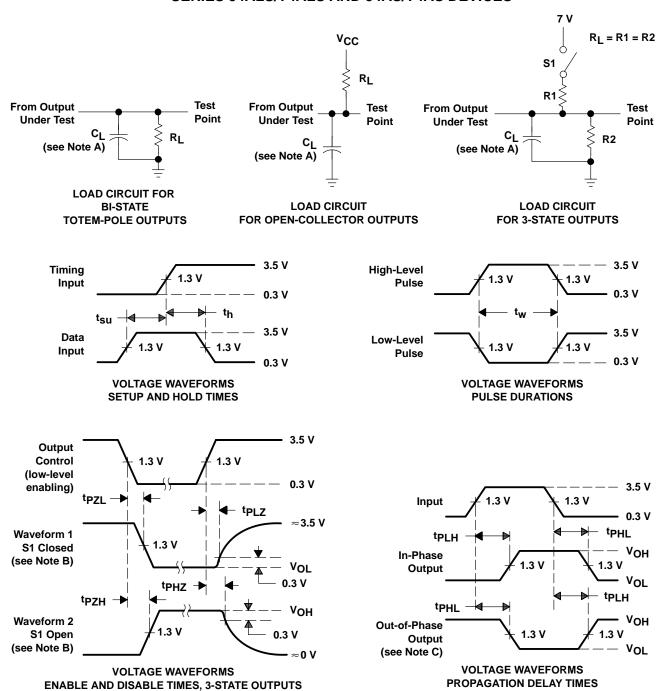
[§] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _C C _L R _L T _A	UNIT			
			SN54A	LS259	SN74ALS259		
			MIN	MAX	MIN	MAX	
t _{PHL}	CLR	Any Q	2	15	2	12	ns
^t PLH	Data	Any Q	4	22	4	19	ne
^t PHL	Data	Ally Q	2	15	2	12	ns
t _{PLH}	Address	Any Q	4	26	4	22	ns
t _{PHL}	Address		2	15	2	12	115
tPLH	Execute	Any O	4	22	4	20	ne
^t PHL	Execute	Any Q	2	16	2	13	ns

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
- All input pulses have the following characteristics: PRR \leq 1 MHz, $t_{\Gamma} = t_{f} = 2$ ns, duty cycle = 50%.
- The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



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