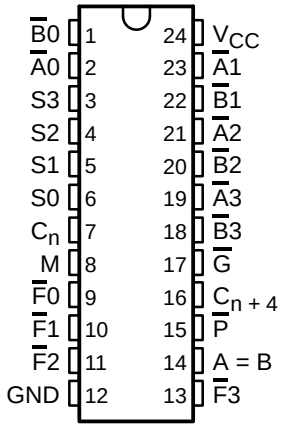
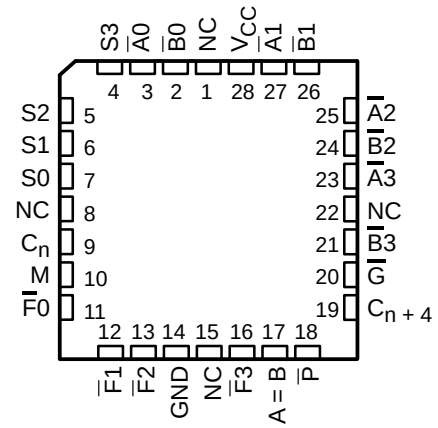
- **Full Look Ahead for High-Speed Operations on Long Words**
- **Arithmetic Operating Modes:**
  - **Addition**
  - **Subtraction**
  - **Shift Operand A One Position**
  - **Magnitude Comparison**
  - **Twelve Other Arithmetic Operations**
- **Logic Function Modes:**
  - **Exclusive-OR**
  - **Comparator**
  - **AND, NAND, OR, NOR**
- **Package Options Include Plastic Small-Outline (N) Packages, Ceramic (FK) Chip Carriers, Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs, and Ceramic (JW) 600-mil DIPs**

SN54AS181B . . . JT OR JW PACKAGE
SN74AS181A . . . N OR NT PACKAGE
(TOP VIEW)



SN54AS181B . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN54AS181B and SN74AS181A arithmetic logic units (ALUs)/function generators have a complexity of 75 equivalent gates on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select (S0, S1, S2, and S3) lines and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries are enabled by applying a low-level voltage to the mode-control (M) input. A full carry look-ahead scheme is used to generate fast, simultaneous carry by means of two cascade ($\overline{G}$ and $\overline{P}$) outputs for the four bits in the package.

If high speed is not important, a ripple-carry (C_n) input and a ripple-carry (C_{n+4}) output are available. The ripple-carry delay is minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

The SN54AS181B and SN74AS181A accommodate active-high or active-low data if the pin designations are interpreted as follows:

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-low data (Table 1)	$\overline{A}0$	$\overline{B}0$	$\overline{A}1$	$\overline{B}1$	$\overline{A}2$	$\overline{B}2$	$\overline{A}3$	$\overline{B}3$	$\overline{F}0$	$\overline{F}1$	$\overline{F}2$	$\overline{F}3$	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$
Active-high data (Table 2)	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3	$\overline{C}_n$	$\overline{C}_{n+4}$	X	Y

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A-B-1, which requires an end-around or forced carry to provide A-B.

description (continued)

The SN54AS181B and SN74AS181A also can be used as comparators. The A = B output is internally decoded from the function (F0, F1, F2, F3) outputs so that when two words of equal magnitude are applied at the A and B inputs, the output assumes a high level to indicate equality (A = B). The ALU must be in the subtract mode with C_n = H when performing this comparison. The A = B output is open collector so that it can be wire-AND connected to give a comparison for more than four bits. C_{n+4} also can be used to supply relative magnitude information. The ALU must be placed in the subtract mode by placing the function-select inputs S3, S2, S1, and S0 at L, H, H, and L, respectively.

INPUT C_n	OUTPUT C_{n+4}	ACTIVE-LOW DATA (Figure 1)	ACTIVE-HIGH DATA (Figure 2)
H	H	A ≥ B	A ≤ B
H	L	A < B	A > B
L	H	A > B	A < B
L	L	A ≤ B	A ≥ B

These circuits not only incorporate all of the designer's requirements for arithmetic operations, but also provide 16 possible functions of two Boolean variables without using external circuitry. These logic functions are selected by the four function-select inputs with M at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

TYPICAL ADDITION TIME
(C_L = 15 pF, R_L = 280 Ω, T_A = 25°C)

NUMBER OF BITS	ADDITION TIME USING ′S181 AND ′S182	PACKAGE COUNT		CARRY METHOD BETWEEN ALUs
		ALUs	LOOK-AHEAD CARRY GENERATORS	
1 to 4	11 ns	1		None
5 to 8	18 ns	2		Ripple
9 to 16	19 ns	3 or 4	1	Full look ahead
17 to 64	28 ns	5 to 16	2 to 5	Full look ahead

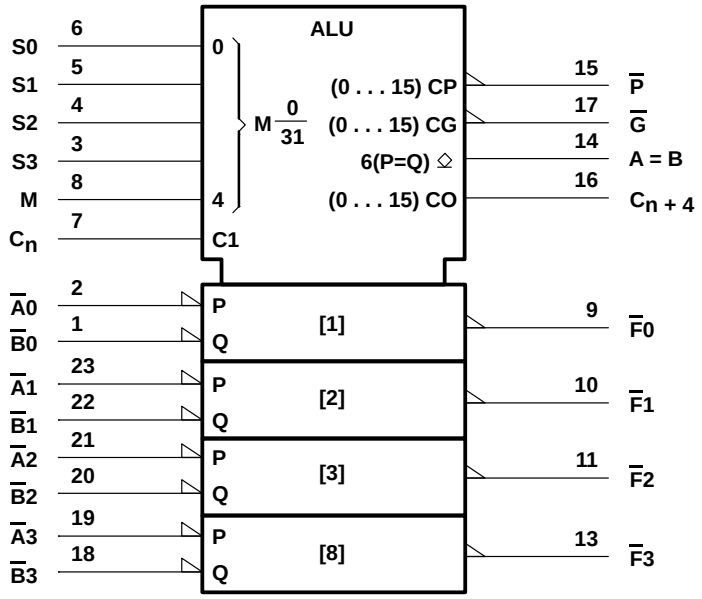
The SN54AS181B is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AS181A is characterized for operation from 0°C to 70°C.

application note

An application-specific problem has been identified in the SN54AS181B device. The F0–F4 outputs exhibit voltage transients when one or more B-data inputs transition from a high to a low state. The resultant voltage transients can have an amplitude of 2 V relative to V_{OL} with a width of 5 ns at an input threshold of 1.5 V. The transient pulse occurs coincidentally with the high-to-low transition of the B-data input(s) and appears to be caused by internal coupling.

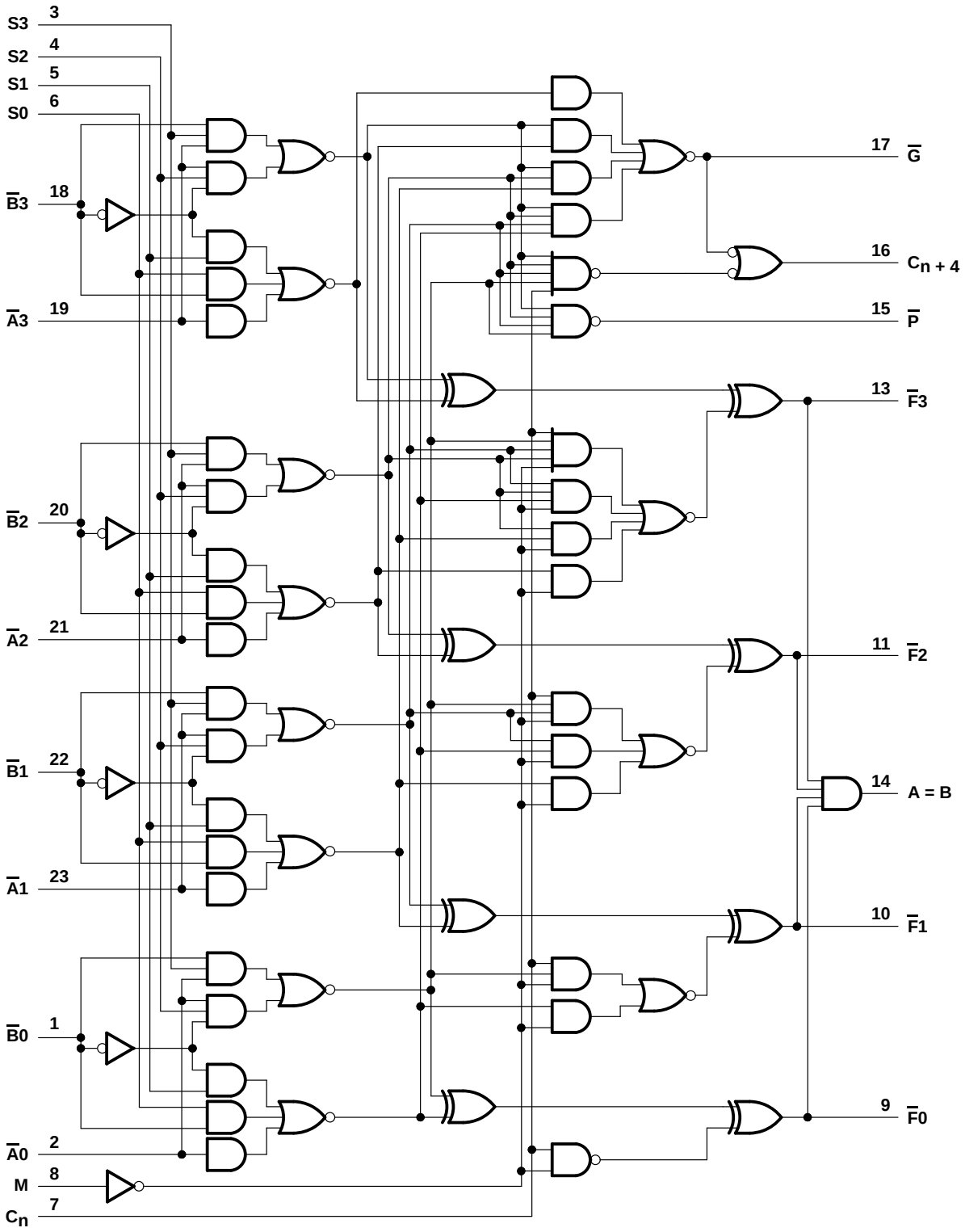
In system operations in which this device is used, it is likely that transmission-line effects minimize this anomaly. Narrow width of the voltage transient makes the pulse transparent to most circuitry; however, in certain applications, the transients can cause system errors.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the JT, JW, N, and NT packages.

logic diagram



Pin numbers shown are for the JT, JW, N, and NT packages.

signal designations

In Figures 1 and 2, the polarity indicators (◺) indicate that the associated input or output is active low with respect to the function shown inside the symbol. The symbols are the same in both figures. The signal designations in Figure 1 agree with the indicated internal functions based on active-low data and are for use with the logic functions and arithmetic operations shown in Table 1. The signal designations have been changed in Figure 2 to accommodate the logic functions and arithmetic operations for the active-high data given in Table 2. The SN54AS181B and SN74AS181A together with the ′S182 can be used with the signal designation of either Figure 1 or Figure 2.

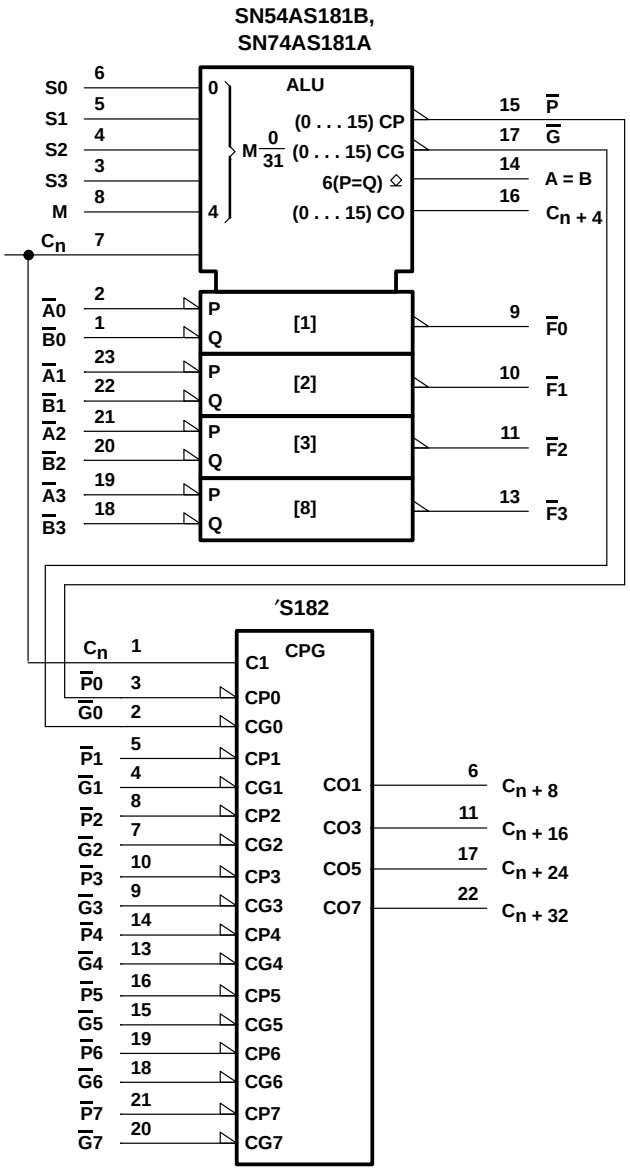


Figure 1
(use with Table 1)

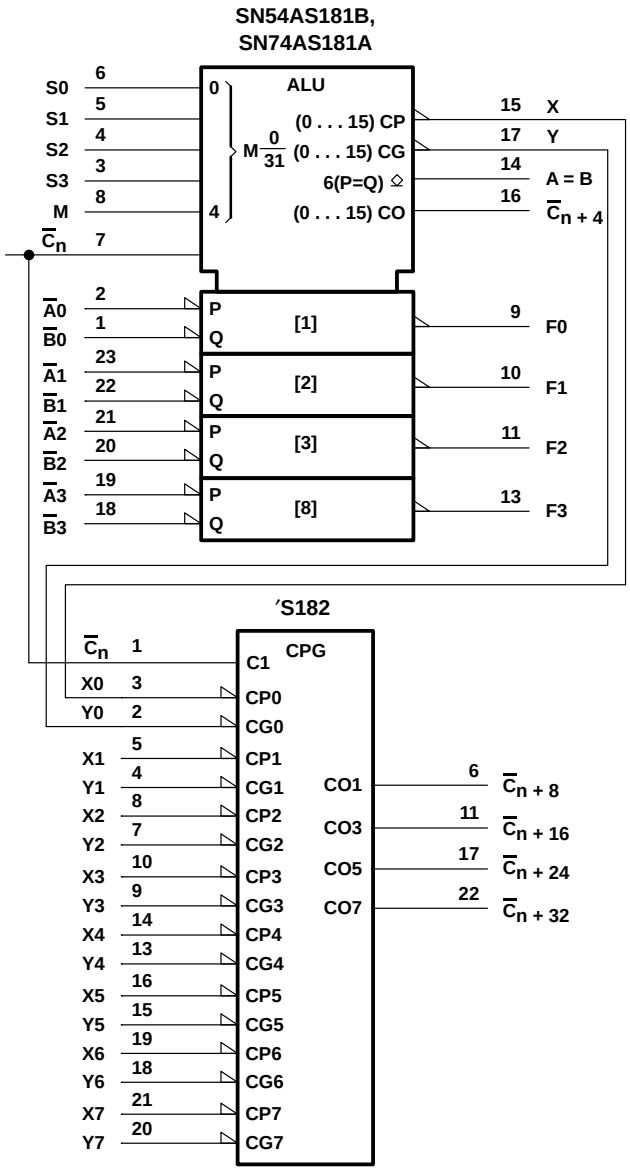


Figure 2
(use with Table 2)

Table 1

SELECTION				ACTIVE-LOW DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	C_n = L (no carry)	C_n = H (with carry)
L	L	L	L	F = $\overline{A}$	F = A MINUS 1	F = A
L	L	L	H	F = $\overline{AB}$	F = AB MINUS 1	F = AB
L	L	H	L	F = $\overline{A}$ + B	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
L	L	H	H	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	F = $\overline{A + B}$	F = A PLUS (A + $\overline{B}$)	F = A PLUS (A + $\overline{B}$) PLUS 1
L	H	L	H	F = $\overline{B}$	F = AB PLUS (A + $\overline{B}$)	F = AB PLUS (A + $\overline{B}$) PLUS 1
L	H	H	L	F = $\overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
H	L	L	L	F = $\overline{A}$B	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H	L	L	H	F = A ⊕ B	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = A$\overline{B}$ PLUS (A + B)	F = A$\overline{B}$ PLUS (A + B) PLUS 1
H	L	H	H	F = A + B	F = (A + B)	F = (A + B) PLUS 1
H	H	L	L	F = 0	F = A PLUS A†	F = A PLUS A PLUS 1
H	H	L	H	F = A$\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H	H	H	L	F = AB	F = A$\overline{B}$ PLUS A	F =A$\overline{B}$ PLUS A PLUS 1
H	H	H	H	F = A	F = A PLUS 1	F = A PLUS 1

† Each bit is shifted to the next more significant position.

Table 2

SELECTION				ACTIVE-HIGH DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	C_n = H (no carry)	C_n = L (with carry)
L	L	L	L	F = $\overline{A}$	F = A	F = A PLUS 1
L	L	L	H	F = $\overline{A + B}$	F = A + B	F = (A+ B) PLUS 1
L	L	H	L	F = $\overline{A}$B	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
L	L	H	H	F = 0	F = MINUS 1 (2's COMPL)	F = ZERO
L	H	L	L	F = $\overline{AB}$	F = A PLUS A$\overline{B}$	F = A PLUS A$\overline{B}$ PLUS 1
L	H	L	H	F = $\overline{B}$	F = (A + B) PLUS A$\overline{B}$	F =(A + B) PLUS A$\overline{B}$ PLUS 1
L	H	H	L	F = A ⊕ B	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A$\overline{B}$	F = A$\overline{B}$ MINUS 1	F = A $\overline{B}$
H	L	L	L	F = $\overline{A}$ + B	F = A PLUS AB	F = A PLUS AB PLUS 1
H	L	L	H	F = $\overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = (A + $\overline{B}$) PLUS AB	F = (A + $\overline{B}$) PLUS AB PLUS 1
H	L	H	H	F = AB	F = AB MINUS 1	F = AB
H	H	L	L	F = 1	F = A PLUS A†	F = A PLUS A PLUS 1
H	H	L	H	F = A + $\overline{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) PLUS A	F =(A + $\overline{B}$) PLUS A PLUS 1
H	H	H	H	F = A	F = A MINUS 1	F = A

† Each bit is shifted to the next more significant position.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Off-state output voltage (A = B output only) . . . . . 7 V
Operating free-air temperature range, T_A: SN54AS181B . . . . . –55°C to 125°C
SN74AS181A . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54AS181B			SN74AS181A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{OH}	High-level output voltage	A = B output only			5.5			5.5	V
I_{OH}	High-level output current	All outputs except A = B and $\overline{G}$			–2			–2	mA
		$\overline{G}$			–3			–3	
I_{OL}	Low-level output current	All outputs except $\overline{G}$			20			20	mA
		$\overline{G}$			48			48	
T_A	Operating free-air temperature		–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS181B			SN74AS181A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}	Any output except A = B	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –2 mA	V_{CC} –2			V_{CC} –2			V
	$\overline{G}$	V_{CC} = 4.5 V,	I_{OH} = –3 mA	2.4	3.4		2.4	3.4		
V_{OL}	Any output except $\overline{G}$	V_{CC} = 4.5 V	I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
	$\overline{G}$		I_{OL} = 48 mA		0.4	0.5		0.4	0.5	
I_{OH}	A = B	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
I_I	M	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	Any $\overline{A}$ or $\overline{B}$					0.3			0.3	
	Any S					0.4			0.4	
	C_n					0.6			0.6	
I_{IH}	M	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
	Any $\overline{A}$ or $\overline{B}$					60			60	
	Any S					80			80	
	C_n					120			120	
I_{IL}	M	V_{CC} = 5.5 V,	V_I = 0.4 V			–0.5			–2	mA
	Any $\overline{A}$ or $\overline{B}$					–1.5			–6	
	Any S					–2			–8	
	C_n					–3			–12	
I_O‡	All outputs except A = B and $\overline{G}$	V_{CC} = 5.5 V,	V_O = 2.25 V	–30	–45	–112	–30	–45	–112	mA
	$\overline{G}$			–30		–125	–30		–125	
I_{CC}		V_{CC} = 5.5 V			74	117		135	200	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS†	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX‡				UNIT
				SN54AS181B		SN74AS181A		
				MIN	MAX	MIN	MAX	
t_{PLH}	C_n	C_{n+4}		3	9	2	9	ns
t_{PHL}				2	7	2	9	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	C_{n+4}	M = 0, S1 = S2 = 0, S0 = S3 = 4.5 V (SUM mode)	2	16	2	12	ns
t_{PHL}				2	14	2	12	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	C_{n+4}	M = 0, S1 = S3 = 0, S1 = S2 = 4.5 V (DIFF mode)	3	18	4	16	ns
t_{PHL}				3	14.5	2	16	
t_{PLH}	C_n	Any $\overline{F}$	M = 0 (SUM or DIFF mode)	3	10.5	3	9	ns
t_{PHL}				3	10	3	9	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M = 0, S1 = S2 = 0, S0 = S3 = 4.5 V (SUM mode)	3	9.5	2	8	ns
t_{PHL}				2	7	2	7	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M = 0, S1 = S3 = 0, S1 = S2 = 4.5 V (DIFF mode)	3	12	2	9.5	ns
t_{PHL}				2	9	2	9	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{P}$	M = 0, S1 = S2 = 0, S0 = S3 = 4.5 V (SUM mode)	3	9.5	2	8	ns
t_{PHL}				2	7.5	2	8	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{P}$	M = 0, S1 = S3 = 0, S1 = S2 = 4.5 V (DIFF mode)	3	12	2	10	ns
t_{PHL}				3	8.5	2	10	
t_{PLH}	$\overline{A}i$ or $\overline{B}i$	$\overline{F}i$	M = 0, S1 = S2 = 0, S0 = S3 = 4.5 V (SUM mode)	3	11	2	9.5	ns
t_{PHL}				3	9	2	8	
t_{PLH}	$\overline{A}i$ or $\overline{B}i$	$\overline{F}i$	M = 0, S1 = S3 = 0, S1 = S2 = 4.5 V (DIFF mode)	3	13.5	2	10.5	ns
t_{PHL}				3	11	2	10	
t_{PLH}	$\overline{A}i$ or $\overline{B}i$	$\overline{F}i$	M = 4.5 V (LOGIC mode)	3	16	2	11	ns
t_{PHL}				3	10	2	11	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	A = B	M = 0, S1 = S3 = 0, S1 = S2 = 4.5 V (DIFF mode)	2	19	4	21	ns
t_{PHL}				3	22	4	21	

† Refer to the parameter measurement information tables for the SUM-, DIFF-, and LOGIC-mode test tables.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

PARAMETER MEASUREMENT INFORMATION

SUM-MODE TEST TABLE
(Function Inputs: S0 = S3 = 4.5 V, S1 = S2 = M = 0)

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (See Note 1)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}i$	In phase
t_{PLH} t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}i$	In phase
t_{PLH} t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In phase
t_{PLH} t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In phase
t_{PLH} t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In phase
t_{PLH} t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In phase
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}	In phase
t_{PLH} t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	Out of phase
t_{PLH} t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	Out of phase

PARAMETER MEASUREMENT INFORMATION

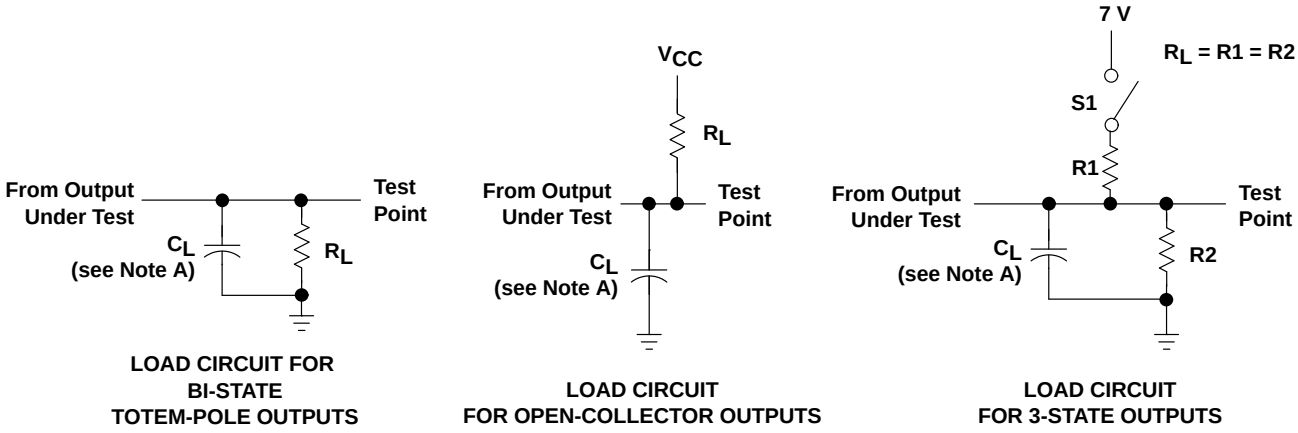
DIFF-MODE TEST TABLE
(Function Inputs: S1 = S2 = 4.5 V, S0 = S3 = M = 0)

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (See Note 1)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} / t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}i$	In phase
t_{PLH} / t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}i$	Out of phase
t_{PLH} / t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In phase
t_{PLH} / t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	Out of phase
t_{PLH} / t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	In phase
t_{PLH} / t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	Out of phase
t_{PLH} / t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	In phase
t_{PLH} / t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	Out of phase
t_{PLH} / t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	C_{n+4} or any $\overline{F}$	In phase
t_{PLH} / t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$, $\overline{B}$, C_n	C_{n+4}	Out of phase
t_{PLH} / t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	None	Remaining $\overline{A}$, $\overline{B}$, C_n	C_{n+4}	In phase

LOGIC-MODE TEST TABLE
(Function Inputs: S1 = S2 = M = 4.5 V, S0 = S3 = 0)

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (See Note 1)
		APPLY 4.5 V	APPLY GND	APPLY GND	APPLY 4.5 V		
t_{PLH} / t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}i$	Out of phase
t_{PLH} / t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}i$	Out of phase

PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



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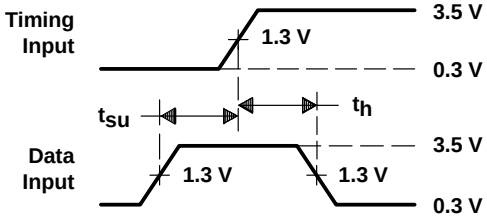
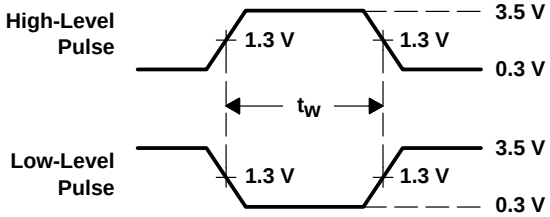
LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS

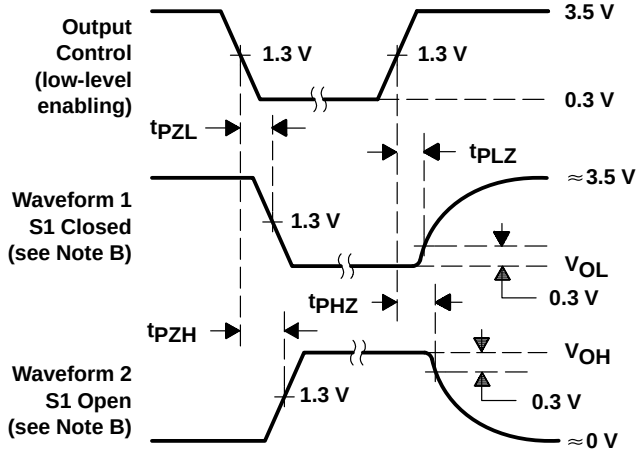
LOAD CIRCUIT FOR 3-STATE OUTPUTS



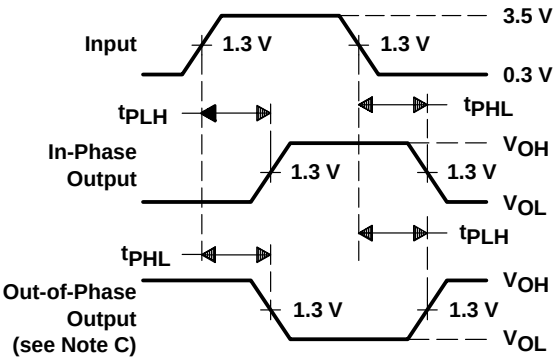
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

Figure 3. Load Circuits and Voltage Waveforms

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