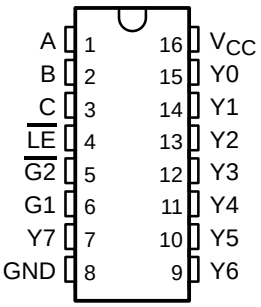
- **Combines Decoder and 3-Bit Address Latch**
- **Incorporates Two Output Enables to Simplify Cascading**
- **Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

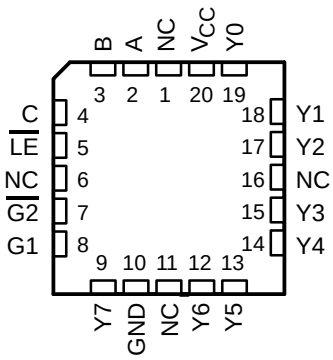
The SN54ALS137A, SN74ALS137A, and SN74AS137 are 3-line to 8-line decoders/demultiplexers with latches on the three address inputs. When the latch-enable ($\overline{LE}$) input is low, the devices act as decoders/demultiplexers. When $\overline{LE}$ goes from low to high, the address present at the select (A, B, and C) inputs is stored in the latches. Further address changes are ignored as long as $\overline{LE}$ remains high. The output-enable controls (G1 and $\overline{G2}$) control the outputs independently of the select or latch-enable inputs. All of the outputs are forced high if G1 is low or $\overline{G2}$ is high. These devices are ideally suited for implementing glitch-free decoders in strobed (stored-address) applications in bus-oriented systems.

The SN54ALS137A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ALS137A and SN74AS137 are characterized for operation from 0°C to 70°C.

SN54ALS137A . . . J PACKAGE
SN74ALS137A, SN74AS137 . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS137A . . . FK PACKAGE
(TOP VIEW)

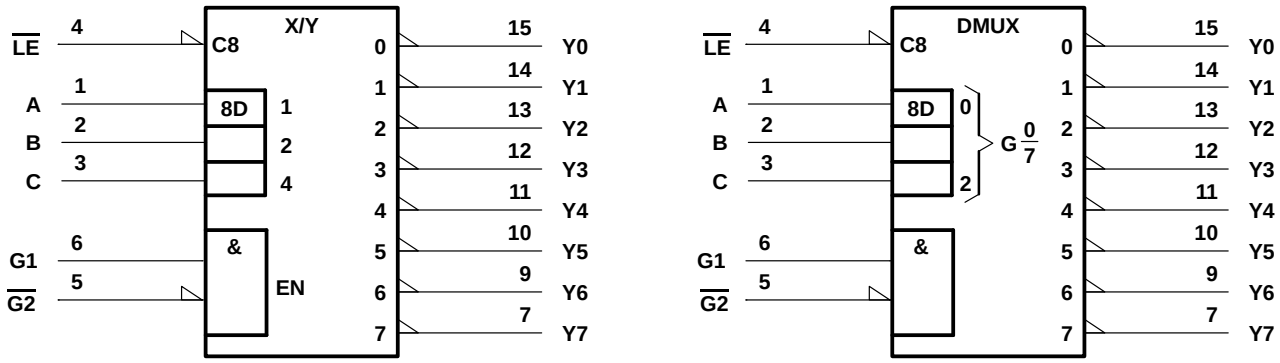


NC – No internal connection

FUNCTION TABLE

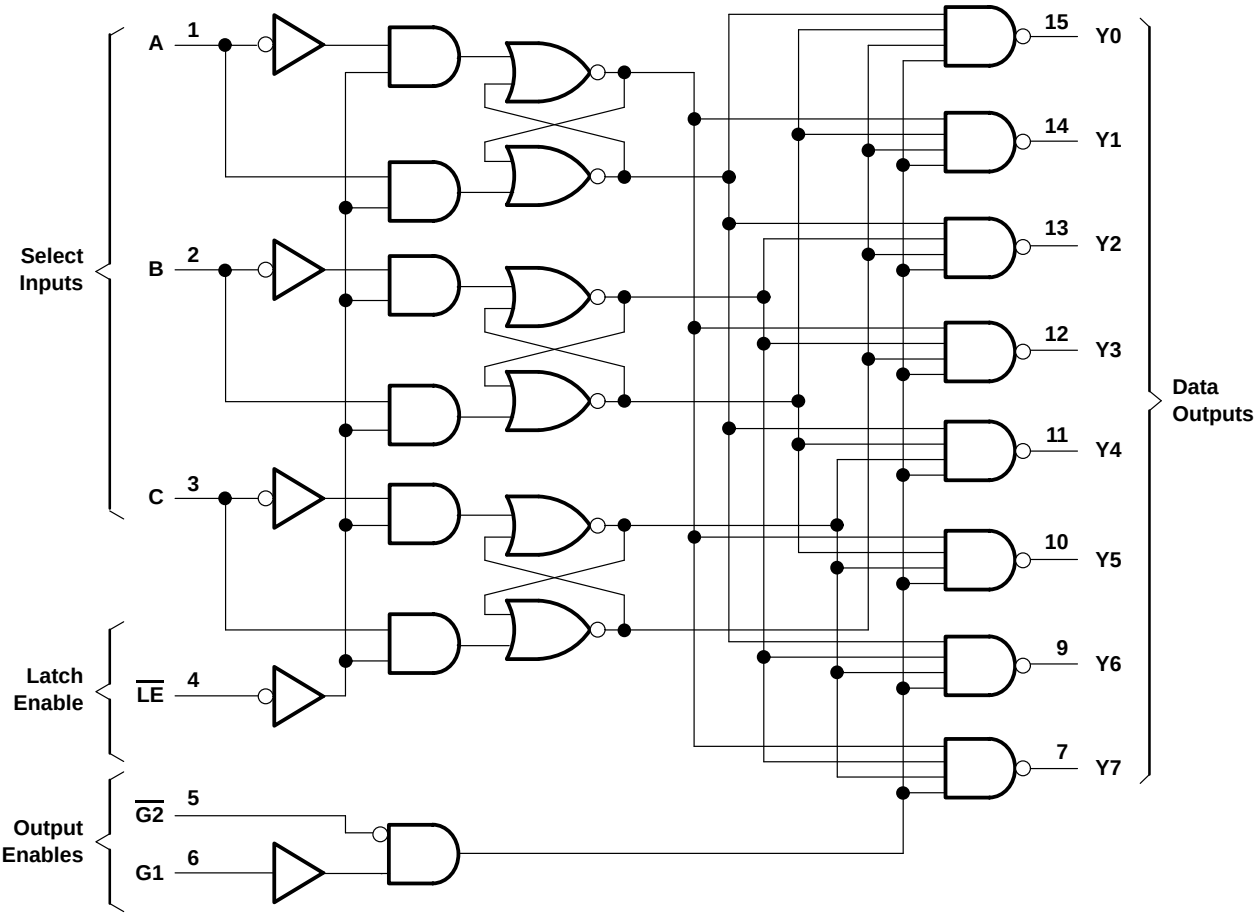
INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{LE}$	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Outputs corresponding to stored address = L; all others = H							

logic symbols (alternatives)†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for the D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Operating free-air temperature range, T_A: SN54ALS137A . . . . . –55°C to 125°C
SN74ALS137A . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54ALS137A			SN74ALS137A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			–0.4			–0.4	mA
I_{OL}	Low-level output current			4			8	mA
t_w	Pulse duration, $\overline{LE}$ low	15			10			ns
t_{su}	Setup time at A, B, and C before $\overline{LE}\uparrow$	15			10			ns
t_h	Hold time at A, B, and C after $\overline{LE}\uparrow$	5			5			ns
T_A	Operating free-air temperature	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS137A			SN74ALS137A			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA			–1.5			–1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –0.4 mA	V_{CC} –2			V_{CC} –2			V
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			–0.1			–0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	–20		–112	–30		–112	mA
I_{CC}	V_{CC} = 5.5 V			5	11		5	11	mA

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX†				UNIT
			SN54ALS137A		SN74ALS137A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A, B, C	Y	5	25	5	20	ns
t_{PHL}			6	25	6	20	
t_{PLH}	$\overline{G2}$	Y	4	15	3	12	ns
t_{PHL}			5	18	4	15	
t_{PLH}	G1	Y	5	21	4	17	ns
t_{PHL}			5	19	4	15	
t_{PLH}	$\overline{LE}$	Y	7	27	6	22	ns
t_{PHL}			7	25	7	20	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) ‡

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Operating free-air temperature range, T_A: SN74AS137 . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN74AS137			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–2	mA
I_{OL}	Low-level output current			20	mA
t_w	Pulse duration, $\overline{LE}$ low	6.5			ns
t_{su}	Setup time at A, B, and C before $\overline{LE}\uparrow$	4			ns
t_h	Hold time at A, B, and C after $\overline{LE}\uparrow$	1			ns
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN74AS137			UNIT
			MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA			–1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –2 mA	V_{CC}–2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			–1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	–30		– 112	mA
I_{CC}	V_{CC} = 5.5 V			15	24	mA

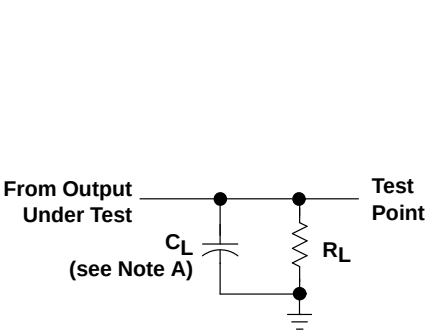
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

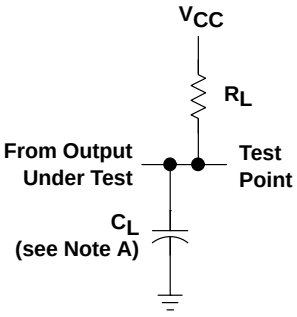
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX§		UNIT
			SN74AS137		
			MIN	MAX	
t_{PLH}	A, B, C	Y	2	12.5	ns
t_{PHL}			2	12.5	
t_{PLH}	$\overline{G2}$	Y	2	8	ns
t_{PHL}			2	8.5	
t_{PLH}	G1	Y	2	10	ns
t_{PHL}			2	9	
t_{PLH}	$\overline{LE}$	Y	3	13.5	ns
t_{PHL}			3	14	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

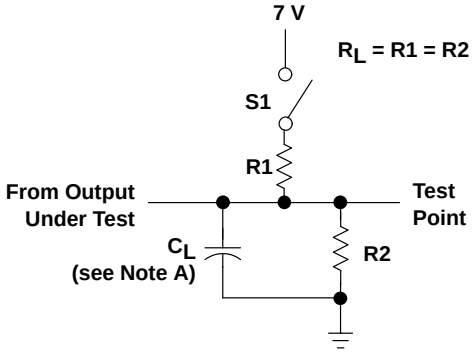
PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



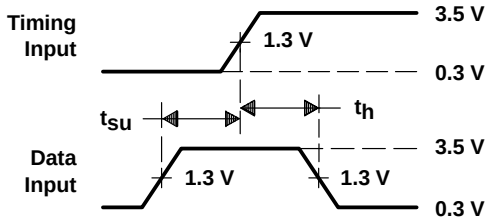
LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS



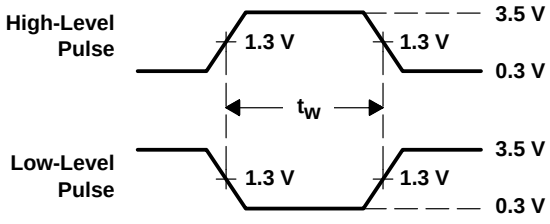
LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS



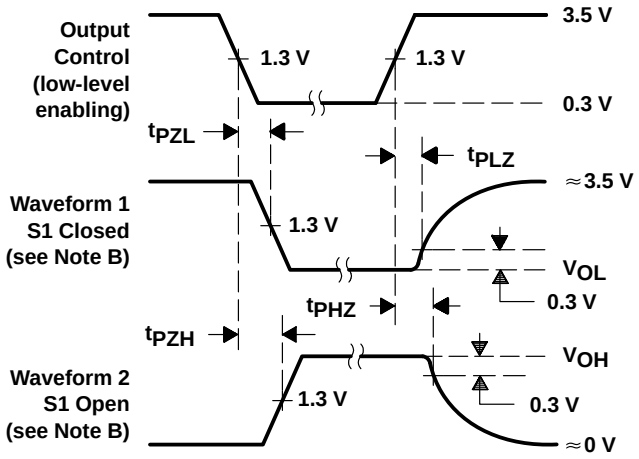
LOAD CIRCUIT
FOR 3-STATE OUTPUTS



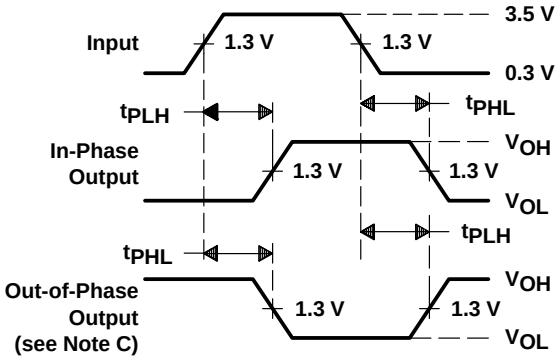
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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