# SN54ALS40A, SN74ALS40A
# DUAL 4-INPUT POSITIVE-NAND BUFFERS

SDAS197 – D2661, APRIL 1984 – REVISED MAY 1986

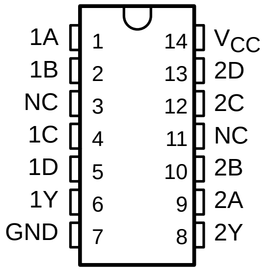
- **Package Options include Plastic Small Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

## description

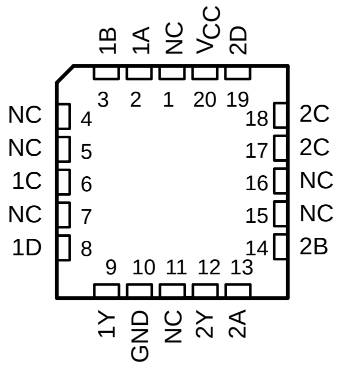
These devices contain two independent 4-input NAND buffer gates. They perform the Boolean functions $Y = \overline{A \bullet B \bullet C \bullet D}$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$ in positive logic.

The SN54ALS40A is characterized for operation over the full military temperature range of – 55°C to 125°C. The SN74ALS40A is characterized for operation from 0°C to 70°C.

**SN54ALS40A . . . J PACKAGE**
**SN74ALS40A . . . D OR N PACKAGE**
**(TOP VIEW)**



**SN54ALS40A . . . FK PACKAGE**
**(TOP VIEW)**

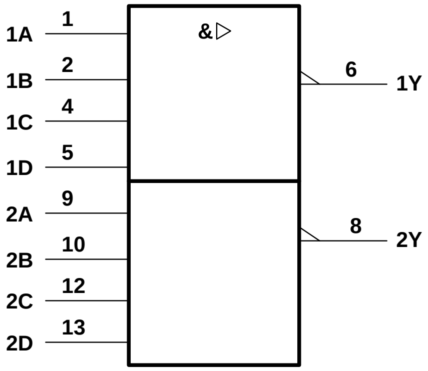


NC – No internal connection

**FUNCTION TABLE**
**(each gate)**

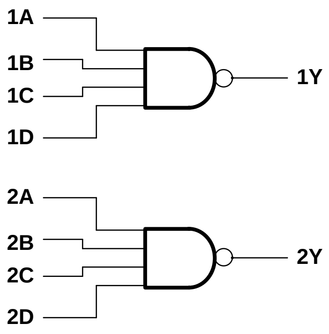
| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| A | B | C | D | Y |
| H | H | H | H | L |
| L | X | X | X | H |
| X | L | X | X | H |
| X | X | L | X | H |
| X | X | X | L | H |

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

## logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | | |
|---|---|---|
| Supply voltage, $V_{CC}$ | | 7 V |
| Input voltage | | 7 V |
| Operating free-air temperature range: | SN54ALS40A | –55°C to 125°C |
| | SN74ALS40A | 0°C to 70°C |
| Storage temperature range | | –65°C to 150°C |

### recommended operating conditions

| | | SN54ALS40A | | | SN74ALS40A | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.7 | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | –1 | | | –2.6 | mA |
| $I_{OL}$ | Low-level output current | | | 12 | | | 24 | mA |
| $T_A$ | Operating free-air temperature | –55 | | 125 | 0 | | 70 | °C |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54ALS40A | | | SN74ALS40A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP[†] | MAX | MIN | TYP[†] | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | –1.5 | | | –1.5 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V to 5.5 V, | $I_{OH}$ = –0.4 mA | $V_{CC}$–2 | | | $V_{CC}$–2 | | | V |
| | $V_{CC}$ = 4.5 V, | $I_{OH}$ = –1 mA | 2.3 | 3.3 | | | | | |
| | $V_{CC}$ = 4.5 V, | $I_{OH}$ = –2.6 mA | | | | 2.4 | 3.2 | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 12 mA | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 24 mA | | | | | 0.35 | 0.5 | |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.4 V | | | –0.1 | | | –0.1 | mA |
| $I_O$[‡] | $V_{CC}$ = 5.5 V, | $V_O$ = 2.25 V | –30 | | –112 | –30 | | – 112 | mA |
| $I_{CCH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0 V | | 0.43 | 0.8 | | 0.43 | 0.8 | mA |
| $I_{CCL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 4.5 V | | 2.4 | 3.9 | | 2.4 | 3.9 | mA |

[†] All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25_C.

[‡] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, $I_{OS}$

### switching characteristics (see Note 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V,<br>$C_L$ = 50 pF,<br>$R_L$ = 500 Ω,<br>$T_A$ = 25°C | $V_{CC}$ = 4.5 V to 5.5 V,<br>$C_L$ = 50 pF,<br>$R_L$ = 500 Ω,<br>$T_A$ = MIN to MAX | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | ’ALS40A | SN54ALS40A | | SN74ALS40A | | |
| | | | TYP | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | Any | Y | 5 | 2 | 10 | 2 | 8 | ns |
| $t_{PHL}$ | | | 5 | 2 | 10 | 2 | 7 | |

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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