- **Low-Power Versions of ′ALS244 Series**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **pnp Inputs Reduce dc Loading**
- **Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**
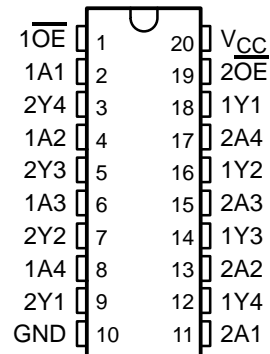
description

These octal buffers and drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.
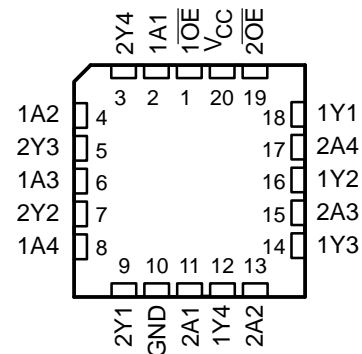
Taken together with the SN74ALS1240, these devices provide the choice of inverting and noninverting outputs.

The SN54ALS1244A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1244A is characterized for operation from 0°C to 70°C.

SN54ALS1244A . . . J PACKAGE
SN74ALS1244A . . . DW OR N PACKAGE
(TOP VIEW)

1$\overline{\text{OE}}$	1	20	V$_{CC}$
1A1	2	19	2$\overline{\text{OE}}$
2Y4	3	18	1Y1
1A2	4	17	2A4
2Y3	5	16	1Y2
1A3	6	15	2A3
2Y2	7	14	1Y3
1A4	8	13	2A2
2Y1	9	12	1Y4
GND	10	11	2A1

SN54ALS1244A . . . FK PACKAGE
(TOP VIEW)

Top pins: 2Y4 (3), 1A1 (2), 1$\overline{\text{OE}}$ (1), V$_{CC}$ (20), 2$\overline{\text{OE}}$ (19)

1A2	4	18	1Y1
2Y3	5	17	2A4
1A3	6	16	1Y2
2Y2	7	15	2A3
1A4	8	14	1Y3

Bottom pins: 2Y1 (9), GND (10), 2A1 (11), 1Y4 (12), 2A2 (13)

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logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and
IEC Publication 617-12.

logic diagram (positive logic)
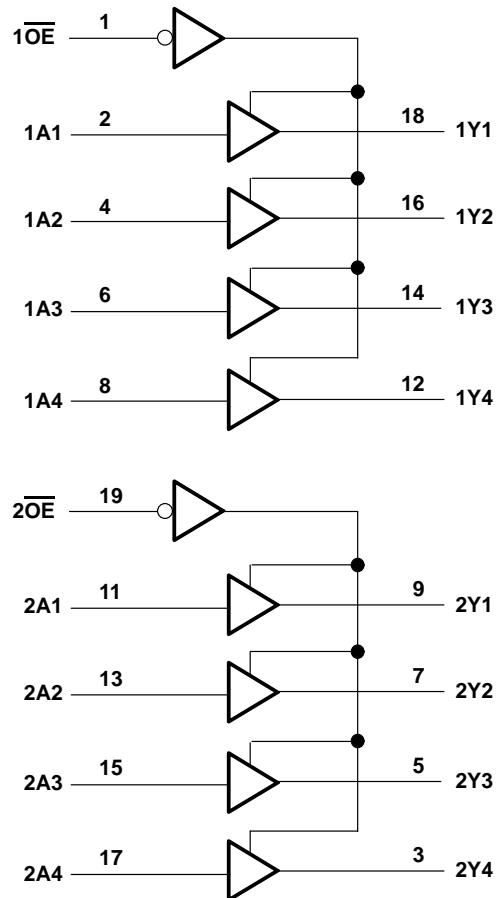
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} .... 7 V
Input voltage, V_I .... 7 V
Voltage applied to a disabled 3-state output .... 5.5 V
Operating free-air temperature range, T_A: SN54ALS1244A .... −55°C to 125°C
SN74ALS1244A .... 0°C to 70°C
Storage temperature range .... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

TEXAS
INSTRUMENTS

recommended operating conditions

		SN54ALS1244A			SN74ALS1244A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			-12			-15	mA
I_{OL}	Low-level output current			8			16	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1244A			SN74ALS1244A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 4.5$ V,	$I_I = -18$ mA			-1.5			-1.5	V
V_{OH}	$V_{CC} = 4.5$ V to 5.5 V,	$I_{OH} = -0.4$ mA	$V_{CC} - 2$			$V_{CC} - 2$			V
	$V_{CC} = 4.5$ V	$I_{OH} = -3$ mA	2.4	3.2		2.4	3.2		
		$I_{OH} = -12$ mA	2						
		$I_{OH} = -15$ mA				2			
V_{OL}	$V_{CC} = 4.5$ V	$I_{OL} = 8$ mA		0.25	0.4		0.25	0.4	V
		$I_{OL} = 16$ mA					0.35	0.5	
I_{OZH}	$V_{CC} = 5.5$ V,	$V_O = 2.7$ V			20			20	µA
I_{OZL}	$V_{CC} = 5.5$ V,	$V_O = 0.4$ V			-20			-20	µA
I_I	$V_{CC} = 5.5$ V,	$V_I = 7$ V			0.1			0.1	mA
I_{IH}	$V_{CC} = 5.5$ V,	$V_I = 2.7$ V			20			20	µA
I_{IL}	$V_{CC} = 5.5$ V,	$V_I = 0.4$ V			-0.1			-0.1	mA
I_O‡	$V_{CC} = 5.5$ V,	$V_O = 2.25$ V	-20		-112	-30		-112	mA
I_{CC}	$V_{CC} = 5.5$ V	Outputs high		6	15		6	11	mA
		Outputs low		10	20		10	17	
		Outputs disabled		11	25		11	20	

† All typical values are at $V_{CC} = 5$ V, $T_A = 25$°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX[†]				UNIT
			SN54ALS1244A		SN74ALS1244A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3	21	3	14	ns
t_{PHL}			3	16	3	14	
t_{PZH}	$\overline{OE}$	Y	6	28	6	22	ns
t_{PZL}			6	26	6	22	
t_{PHZ}	$\overline{OE}$	Y	2	15	2	13	ns
t_{PLZ}			3	25	3	16	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

TEXAS
INSTRUMENTS

PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES

LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS

LOAD CIRCUIT FOR 3-STATE OUTPUTS

VOLTAGE WAVEFORMS SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS PULSE DURATIONS

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES
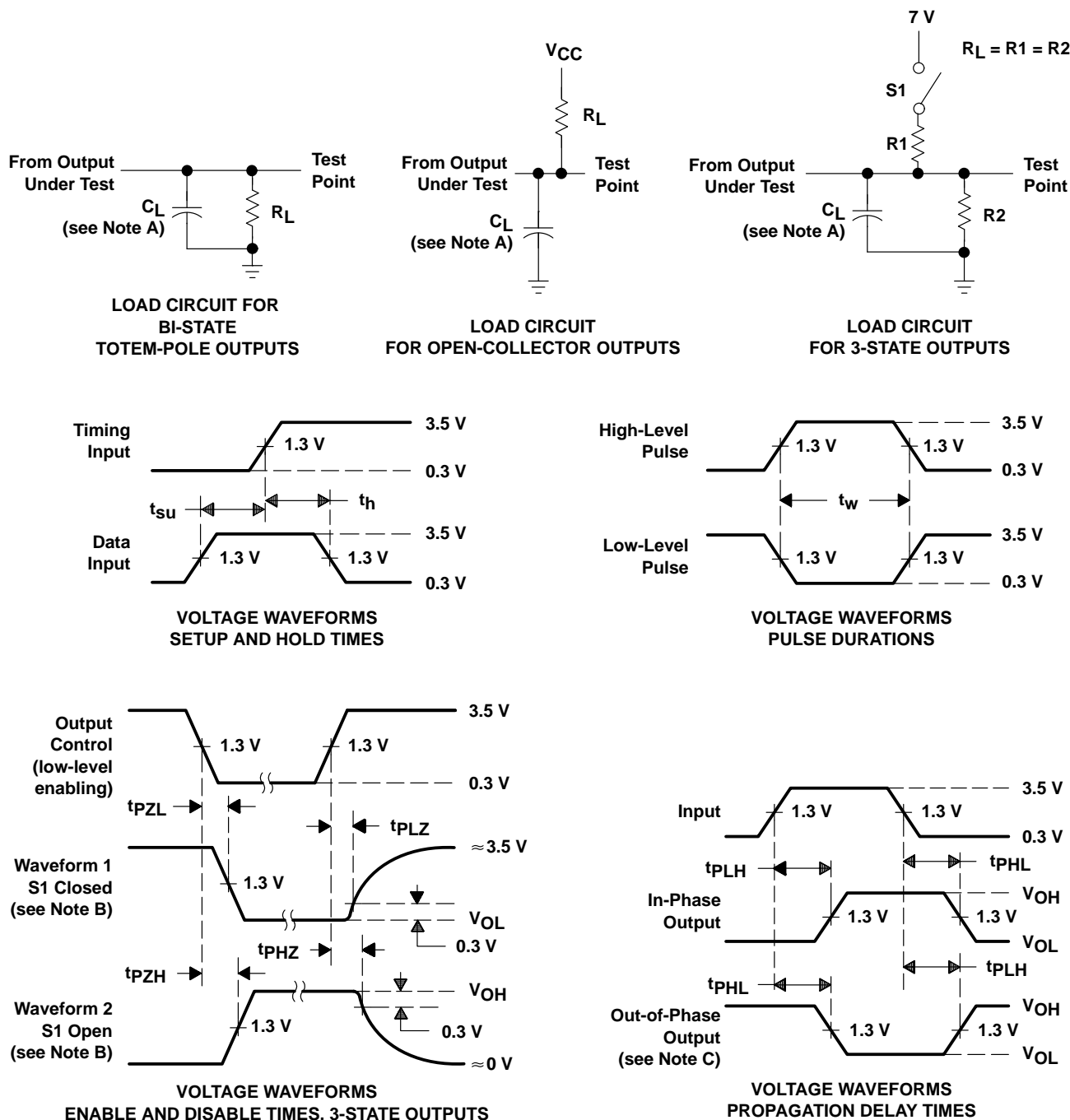
NOTES: A. C_L includes probe and jig capacitance.
      B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
         Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
      C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
      D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
      E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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