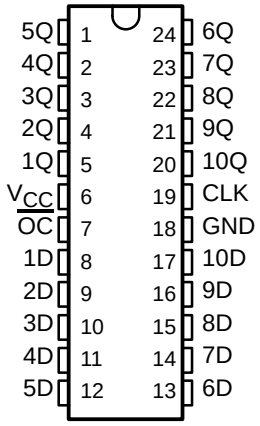
SDAS131 – APRIL 1987

- **Center V_{CC} and GND Configuration Provides Minimum Lead Inductance in High Current Switching Applications**
- **Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity**
- **Outputs Have Undershoot Protection Circuitry**
- **Power-Up High-Impedance State**
- **Package Options include Plastic DIPS. Use the 'AS821 for Plastic and Ceramic Chip Carriers and "Small Outline" Package Options.**
- **Buffered Control inputs to Reduce DC Loading Effects**

NT PACKAGE
(TOP VIEW)



description

This 10-bit flip-flop device features three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers. The ten flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs on the 'AS1821 will be true.

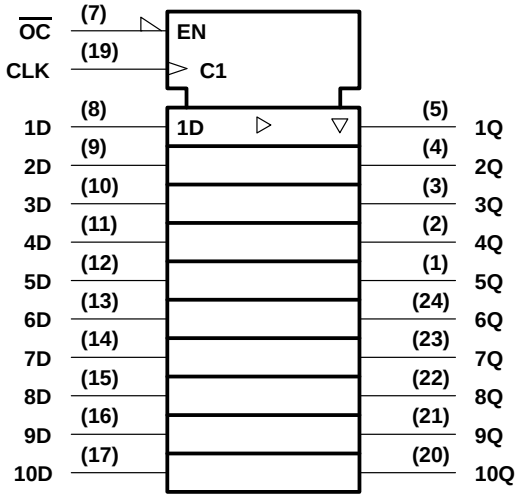
A buffered output-control input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control ($\overline{OC}$) does not affect the internal operation of the flipflops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74AS1821 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each flip-flop)

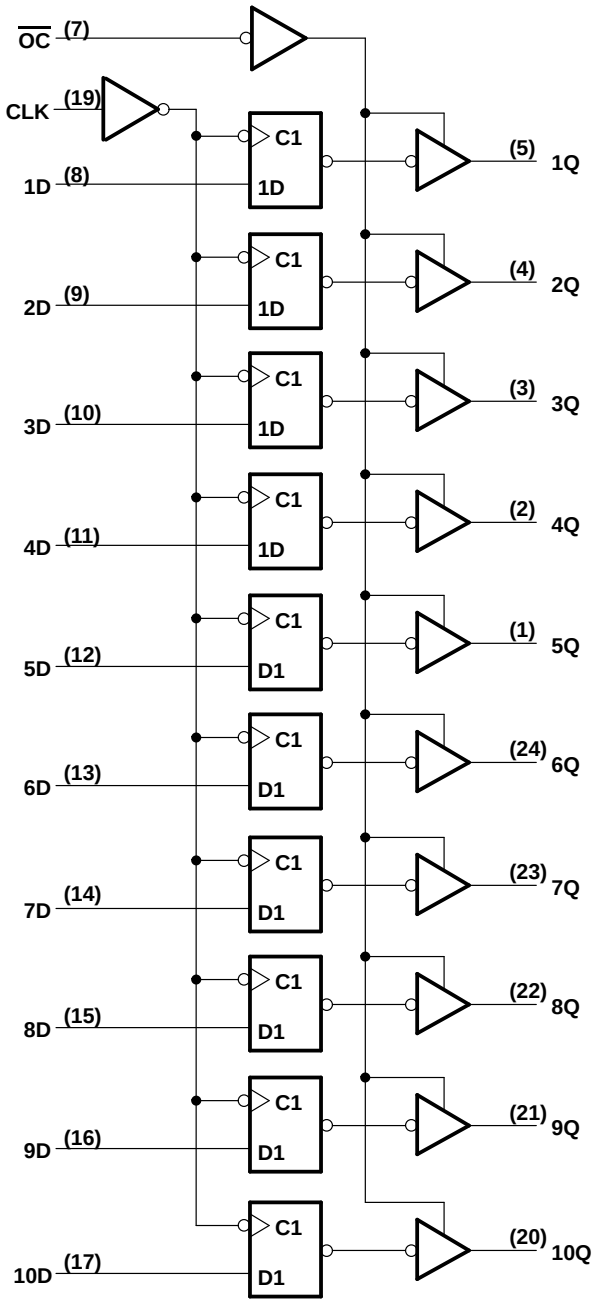
INPUTS			OUTPUT
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_O
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (uness otherwise noted)

Supply voltage, V_{CC} 7V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High-level input voitage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_{OH}	High-level output current			–24	mA
I_{OL}	Low-level output current			48	mA
t_w	Pulse duration, CLK high or low	8			ns
t_{su}	Setup time, data before CLK↑	6			ns
t_h	Hold time, data after CLK↑	0			ns
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V	I_I = –18 mA			–1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –2mA	V_{CC}–2			V
	V_{CC} = 4.5 V,	I_{OH} = –15 mA	2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = –24 mA	2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 32 mA				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			–50	µA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_L	V_{CC} = 5.5 V,	V_I = 0.4 V			0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	–30		–112	mA
I_{CC}	V_{CC} 5.5 V	Outputs high		55	88	mA
		Outputs low		68	09	
		Outputs disabled		70	113	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I[OS]

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX		UNIT
			MIN	MAX	
t_{PLH}	CLK	Any Q	3.5	7.5	ns
t_{PHL}			3.5	10.5	
t_{PZH}	$\overline{OC}$	Any Q	4	11	ns
t_{PZL}			4	2	
t_{PHZ}	$\overline{OC}$	Any Q	2	8	ns
t_{PLZ}			2	8	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1 of the *ALS/AS Logic Data Book, 1986.*

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