

# SN74AS1843

## 9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

SDAS127 – APRIL 1987

- Center  $V_{CC}$  and GND Configuration Provides Minimum Lead Inductance in High Current Switching Applications
- 3-State Buffer-Type Outputs Drive Bus-Lines Directly
- Bus-Structured Pinout
- Provide Extra Bus Driving Latches Necessary for Wider Address/Data Paths or Buses With Parity
- Buffered Control Inputs to Reduce DC Loading
- Power-Up High Impedance
- Package Options Include Plastic DIPs. Use the 'AS843 for Plastic and Ceramic Chip Carriers and "Small Outline" Package Options
- Dependable Texas Instruments Quality and Reliability

### description

This 9-bit latch device features three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

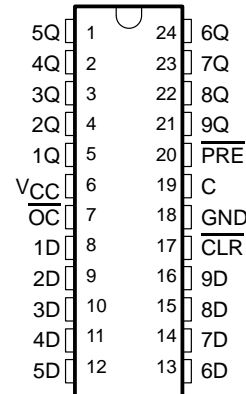
The nine latches are transparent D-type and have noninverting data (D) inputs.

A buffered output control ( $\overline{OC}$ ) input can be used to place the nine outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pullup components.

The output control ( $\overline{OC}$ ) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

The SN74AS1843 is characterized for operation from 0°C to 70°C.

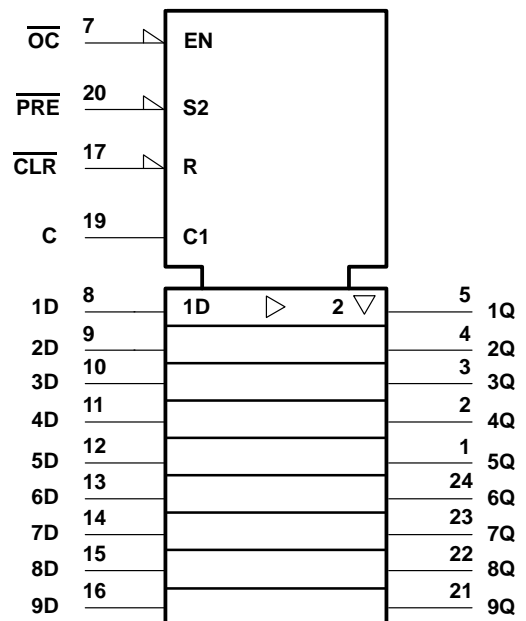
NT Package  
(Top View)



FUNCTION TABLE

INPUTS					OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OC}$	C	D	Q
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	L
H	H	L	H	H	H
H	H	L	L	X	$Q_O$
X	X	H	X	X	Z

### logic symbol †



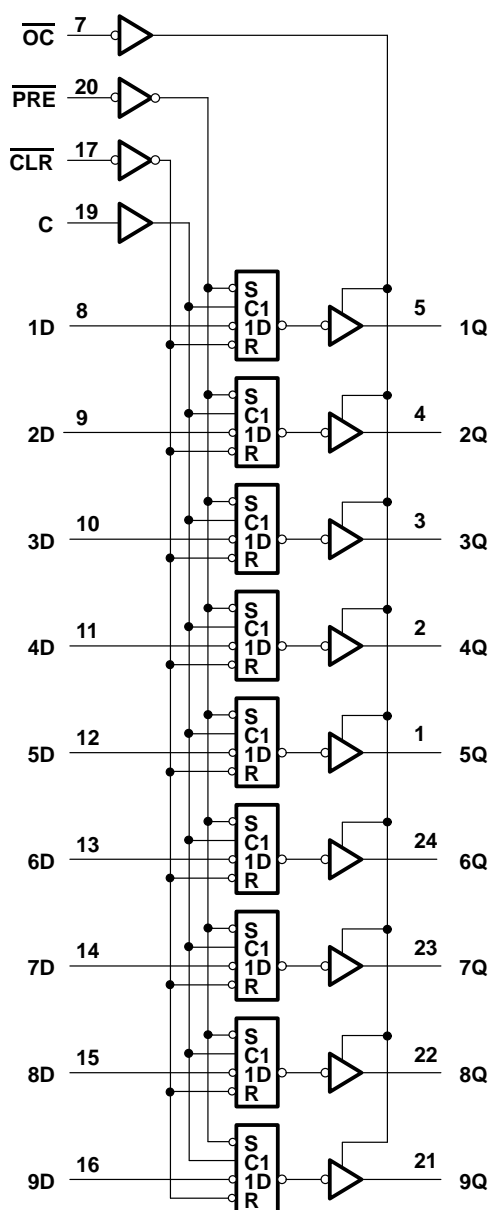
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12,

# SN74AS1843

## 9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

SDAS127 – APRIL 1987

logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	– 65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

# SN74AS1843

## 9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

SDAS127 – APRIL 1987

### recommended operating conditions

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{OH}$	High-level output current			-24	mA
$I_{OL}$	Low-level output current			48	mA
$t_w$	Pulse duration, enable C high	$\overline{CLR}$ or $\overline{PRE}$ low		4	ns
		C high		4	
$t_{su}$	Setup time, data before enable C ↓	2.5			ns
$t_h$	Hold time, data after enable C ↓	2.5			ns
$t_r$	Recovery time	$\overline{PRE}$		15	ns
		$\overline{CLR}$		14	
$T_A$	Operating free-air temperature	0		70	°C

### electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ ,	$I_I = -18\text{ mA}$			-1.2	V
$V_{OH}$	$V_{CC} = 4.5\text{ V}$ ,	$I_{OH} = -2\text{ mA}$	$V_{CC} - 2$			V
	$V_{CC} = 4.5\text{ V}$ ,	$I_{OH} = -15\text{ mA}$	2.4	3.2		
	$V_{CC} = 4.5\text{ V}$ ,	$I_{OH} = -24\text{ mA}$	2			
$V_{OL}$	$V_{CC} = 4.5\text{ V}$ ,	$I_{OL} = 32\text{ mA}$				V
	$V_{CC} = 4.5\text{ V}$ ,	$I_{OL} = 48\text{ mA}$	0.35	0.5		
$I_{OZH}$	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 2.7\text{ V}$			50	μA
$I_{OZL}$	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 0.4\text{ V}$			-50	μA
$I_I$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 7\text{ V}$			0.1	mA
$I_{IH}$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 2.7\text{ V}$			20	μA
$I_{IL}$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 0.4\text{ V}$			-0.05	mA
$I_{O}^{\ddagger}$	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 2.25\text{ V}$	-30		-112	mA
$I_{CC}$	$V_{CC} = 5.5\text{ V}$ ,	Output high		37	62	mA
		Output low		56	92	
		Outputs disabled		56	92	

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

switching characteristics over recommended ranges of supply voltage and free-air temperature (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = 500 Ω, R <sub>2</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX		UNIT
			MIN	MAX	
t <sub>PLH</sub>	D	Q	1	6.5	ns
t <sub>PHL</sub>			1	9	
t <sub>PLH</sub>	C	Q	2	12	ns
t <sub>PHL</sub>			2	12	
t <sub>PLH</sub>	$\overline{\text{PRE}}$	Q	2	10	ns
t <sub>PHL</sub>	$\overline{\text{CLR}}$	Q	2	13	ns
t <sub>PZH</sub>	$\overline{\text{OC}}$	Q	2	10.5	ns
t <sub>PZL</sub>			2	13.5	
t <sub>PHZ</sub>	$\overline{\text{OC}}$	Q	1	8	ns
t <sub>PLZ</sub>			1	8	

NOTE 2: Load circuit and voltage waveforms are shown in Section 1 of the *ALS/AS Logic Data Book, 1986*.

## **IMPORTANT NOTICE**

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

**TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.**

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.