

# SN74AS4374B

## OCTAL EDGE-TRIGGERED D-TYPE DUAL-RANK FLIP-FLOP WITH 3-STATE OUTPUTS

SDAS109D – APRIL 1989 – REVISED JANUARY 1995

- 3-State Outputs Drive Bus Lines Directly
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (N) 300-mil DIPs

### description

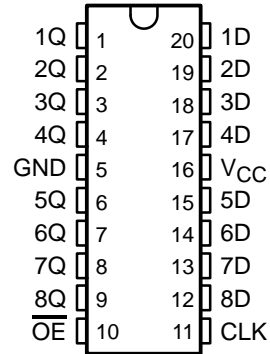
This 8-bit flip-flop features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the SN74AS4374B are edge-triggered D-type flip-flops. On the second positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

The output-enable ( $\overline{OE}$ ) input does not affect internal operations of the flip-flops. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74AS4374B is characterized for operation from 0°C to 70°C.

DW OR N PACKAGE  
(TOP VIEW)



FUNCTION TABLE  
(each flip-flop)

| INPUTS          |     |                | OUTPUT<br>Q    |
|-----------------|-----|----------------|----------------|
| $\overline{OE}$ | CLK | D <sup>†</sup> |                |
| H               | X   | X              | Z              |
| L               | ↑   | L              | L              |
| L               | ↑   | H              | H              |
| L               | L   | X              | Q <sub>0</sub> |

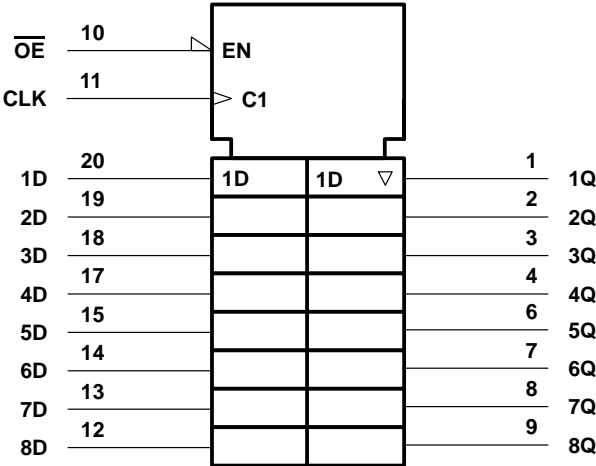
<sup>†</sup> Data presented at the D inputs require two clock cycles to appear at the Q outputs.

SN74AS4374B

OCTAL EDGE-TRIGGERED D-TYPE DUAL-RANK FLIP-FLOP  
WITH 3-STATE OUTPUTS

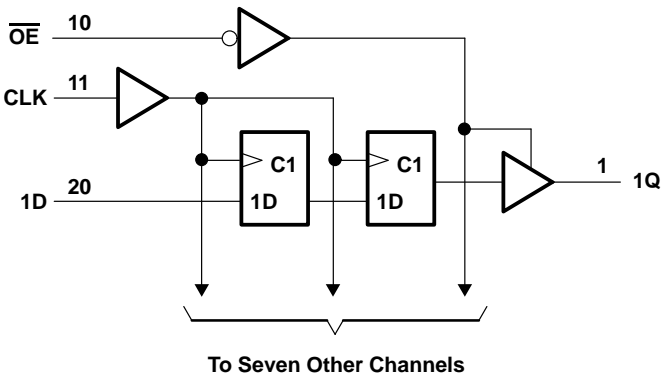
SDAS109D – APRIL 1989 – REVISED JANUARY 1995

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

|   |                |
|---|----------------|
| Supply voltage, $V_{CC}$  | 7 V            |
| Input voltage, $V_I$  | 5.5 V          |
| Voltage applied to any output in the high state or power-off state, $V_O$ | 5.5 V          |
| Operating free-air temperature range, $T_A$                               | 0°C to 70°C    |
| Storage temperature range   | –65°C to 150°C |

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

|          |                                | MIN | NOM | MAX | UNIT |
|----------|--------------------------------|-----|-----|-----|------|
| $V_{CC}$ | Supply voltage                 | 4.5 | 5   | 5.5 | V    |
| $V_{IH}$ | High-level input voltage       | 2   |     |     | V    |
| $V_{IL}$ | Low-level input voltage        |     |     | 0.8 | V    |
| $I_{OH}$ | High-level output current      |     |     | –15 | mA   |
| $I_{OL}$ | Low-level output current       |     |     | 48  | mA   |
| $T_A$    | Operating free-air temperature | 0   |     | 70  | °C   |

# SN74AS4374B

## OCTAL EDGE-TRIGGERED D-TYPE DUAL-RANK FLIP-FLOP WITH 3-STATE OUTPUTS

SDAS109D – APRIL 1989 – REVISED JANUARY 1995

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER       | TEST CONDITIONS           |                          | MIN | TYP† | MAX  | UNIT          |
|-----------------|---------------------------|--------------------------|-----|------|------|---------------|
| $V_{IK}$        | $V_{CC} = 4.5\text{ V}$ , | $I_I = -18\text{ mA}$    |     |      | -1.5 | V             |
| $V_{OH}$        | $V_{CC} = 4.5\text{ V}$   | $I_{OH} = -3\text{ mA}$  | 2.4 | 3.2  |      | V             |
|                 |                           | $I_{OH} = -15\text{ mA}$ | 2   |      |      |               |
| $V_{OL}$        | $V_{CC} = 4.5\text{ V}$   | $I_{OL} = 32\text{ mA}$  |     | 0.25 | 0.4  | V             |
|                 |                           | $I_{OL} = 48\text{ mA}$  |     | 0.35 | 0.5  |               |
| $I_{OZH}$       | $V_{CC} = 5.5\text{ V}$ , | $V_O = 2.7\text{ V}$     |     |      | 20   | $\mu\text{A}$ |
| $I_{OZL}$       | $V_{CC} = 5.5\text{ V}$ , | $V_O = 0.4\text{ V}$     |     |      | -20  | $\mu\text{A}$ |
| $I_I$           | $V_{CC} = 5.5\text{ V}$ , | $V_I = 7\text{ V}$       |     |      | 0.1  | mA            |
| $I_{IH}$        | $V_{CC} = 5.5\text{ V}$ , | $V_I = 2.7\text{ V}$     |     |      | 20   | $\mu\text{A}$ |
| $I_{IL}$        | $V_{CC} = 5.5\text{ V}$ , | $V_I = 0.5\text{ V}$     |     |      | -0.2 | mA            |
| $I_{O\ddagger}$ | $V_{CC} = 5.5\text{ V}$ , | $V_O = 2.25\text{ V}$    | -30 |      | -112 | mA            |
| $I_{CC}$        | $V_{CC} = 5.5\text{ V}$ , | $\overline{OE}$ high     |     | 100  | 150  | mA            |

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

**timing requirements over recommended operating free-air temperature range (unless otherwise noted)**

|   | MIN | MAX | UNIT |
|---|-----|-----|------|
| $f_{\text{clock}}$ Clock frequency              | 0   | 125 | MHz  |
| $t_w$ Pulse duration, CLK high or low           | 4   |     | ns   |
| $t_{su}$ Setup time, data before CLK $\uparrow$ | 4   |     | ns   |
| $t_h$ Hold time, data after CLK $\uparrow$      | 1   |     | ns   |

**switching characteristics (see Figure 1)**

| PARAMETER        | FROM<br>(INPUT) | TO<br>(OUTPUT) | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ,<br>$C_L = 50\text{ pF}$ ,<br>$R_1 = 500\ \Omega$ ,<br>$R_2 = 500\ \Omega$ ,<br>$T_A = \text{MIN to MAX}\S$ |     | UNIT |
|------------------|-----------------|----------------|--|-----|------|
|                  |                 |                | MIN  | MAX |      |
| $f_{\text{max}}$ |                 |                | 125  |     | MHz  |
| $t_{PLH}$        | CLK             | Q              | 2  | 8   | ns   |
| $t_{PHL}$        |                 |                | 2  | 8   |      |
| $t_{PZH}$        | $\overline{OE}$ | Q              | 1.5  | 6   | ns   |
| $t_{PZL}$        |                 |                | 2.5  | 8   |      |
| $t_{PHZ}$        | $\overline{OE}$ | Q              | 2  | 6.5 | ns   |
| $t_{PLZ}$        |                 |                | 2.5  | 7   |      |

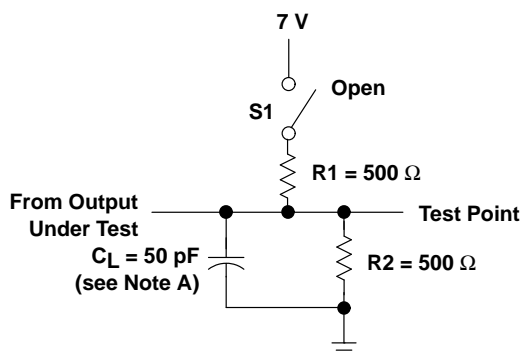
§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

# SN74AS4374B

## OCTAL EDGE-TRIGGERED D-TYPE DUAL-RANK FLIP-FLOP WITH 3-STATE OUTPUTS

SDAS109D – APRIL 1989 – REVISED JANUARY 1995

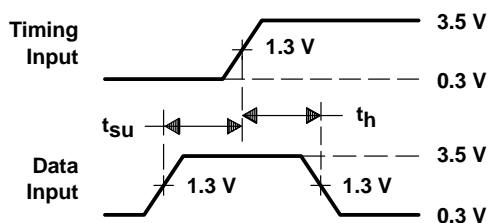
### PARAMETER MEASUREMENT INFORMATION



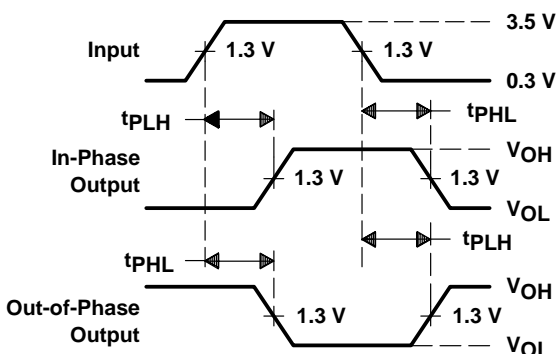
LOAD CIRCUIT FOR 3-STATE OUTPUTS

SWITCH POSITION TABLE

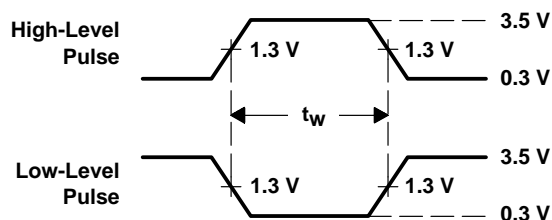
| TEST      | S1     |
|-----------|--------|
| $t_{PLH}$ | Open   |
| $t_{PHL}$ | Open   |
| $t_{PZH}$ | Open   |
| $t_{PZL}$ | Closed |
| $t_{PHZ}$ | Open   |
| $t_{PLZ}$ | Closed |



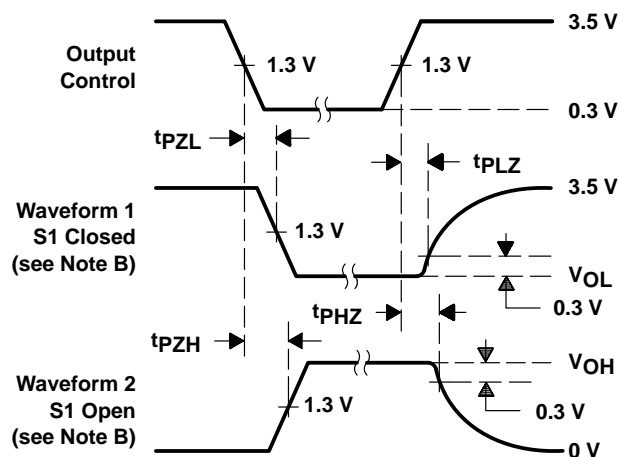
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50$   $\Omega$ ,  $t_r \leq 2$  ns,  $t_f \leq 2$  ns.
  - The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## **IMPORTANT NOTICE**

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

**TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.**

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.