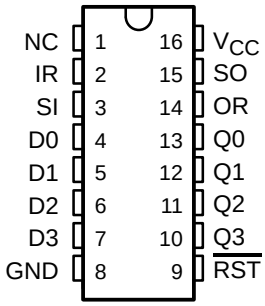
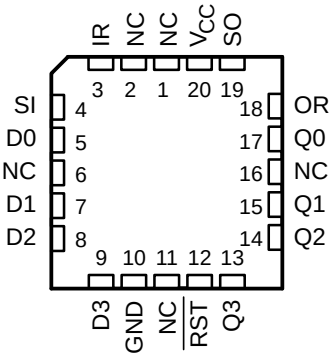
SDAS107A – OCTOBER 1986 – REVISED SEPTEMBER 1993

- **Asynchronous Operation**
- **Organized as 64 Words by 4 Bits**
- **Data Rates From 0 to 30 MHz**
- **3-State Outputs**
- **Package Options Include Plastic Small-Outline Packages (DW), Plastic J-Leaded Chip Carriers (FN), and Standard Plastic 300-mil DIPs (N)**

DW OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN74ALS236 is a 256-bit memory utilizing advanced low-power Schottky IMPACT™ technology. It features high speed with fast fall-through times and is organized as 64 words by 4 bits.

A first-in, first-out (FIFO) memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ALS236 is designed to process data at rates from 0 to 30 MHz in a bit-parallel format, word by word.

Data is written into memory on the rising edge of the shift-in (SI) input. When SI goes low, the first data word ripples through to the output (see Figure 1). As the FIFO fills up, the data words stack up in the order they were written. When the FIFO is full, additional shift-in pulses have no effect. Data is shifted out of memory on the falling edge of the shift-out (SO) input (see Figure 2). When the FIFO is empty, additional SO pulses have no effect. The last data word remains at the outputs until a new word falls through or reset ($\overline{RST}$) goes low.

Status of the SN74ALS236 FIFO memory is monitored by the output-ready (OR) and input-ready (IR) flags. When OR is high, valid data is available at the outputs. OR is low when SO is high and stays low when the FIFO is empty. IR is high when the inputs are ready to receive more data. IR is low when SI is high and stays low when the FIFO is full.

When the FIFO is empty, input data is shifted to the output automatically when SI goes low. If SO is held high during this time, the OR flag pulses high indicating valid data at the outputs (see Figure 3).

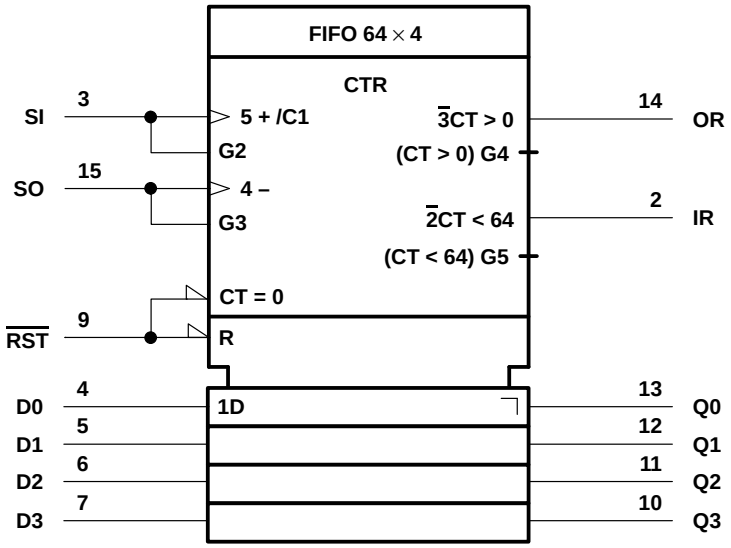
When the FIFO is full, data can be shifted in automatically by holding SI high and taking SO low. One propagation delay after SO goes low, IR will go high. If SI is still high when IR goes high, data at the inputs are automatically shifted in. Since IR is normally low when the FIFO is full and SI is high, only a high-level pulse is seen on the IR output (see Figure 4).

description (continued)

The FIFO must be reset after power up with a low-level pulse on the master reset ($\overline{RST}$) input. This sets IR high and OR low signifying that the FIFO is empty. Resetting the FIFO sets the outputs to a low logic level (see Figure 1). If SI is high when $\overline{RST}$ goes high, the input data is shifted in and IR goes low and remains low until SI goes low. If SI goes low before $\overline{RST}$ goes high, the input data will not be shifted in and IR goes high. Data outputs are noninverting with respect to the data inputs.

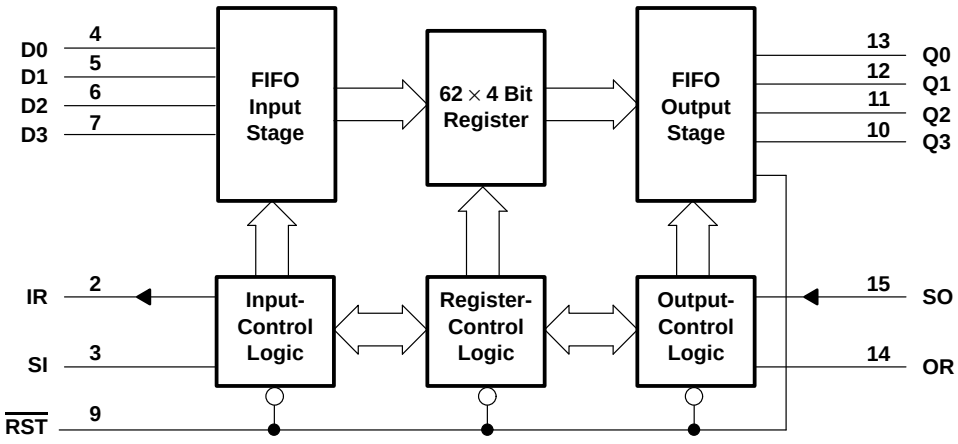
The SN74ALS236 is characterized for operation from 0°C to 70°C.

logic symbol†



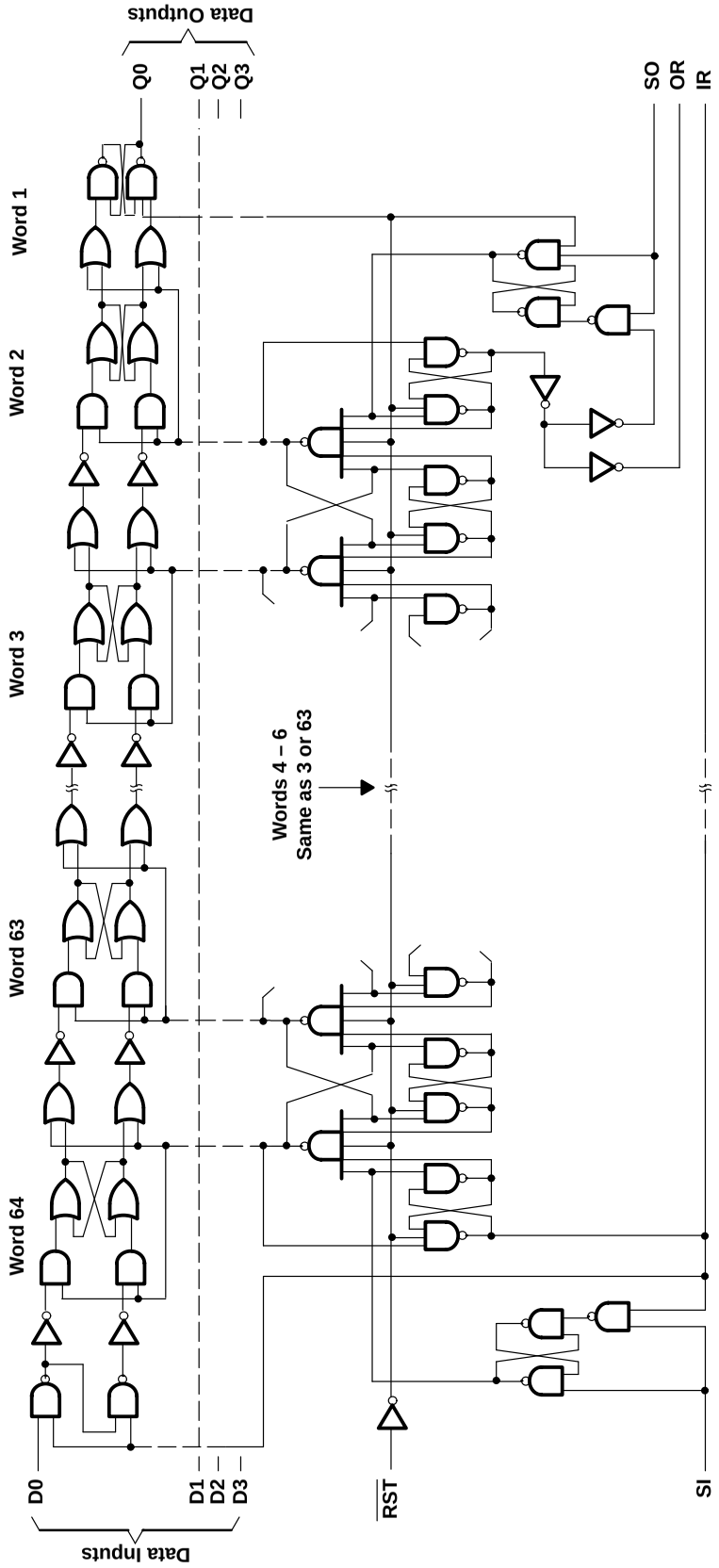
† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12.

functional block diagram

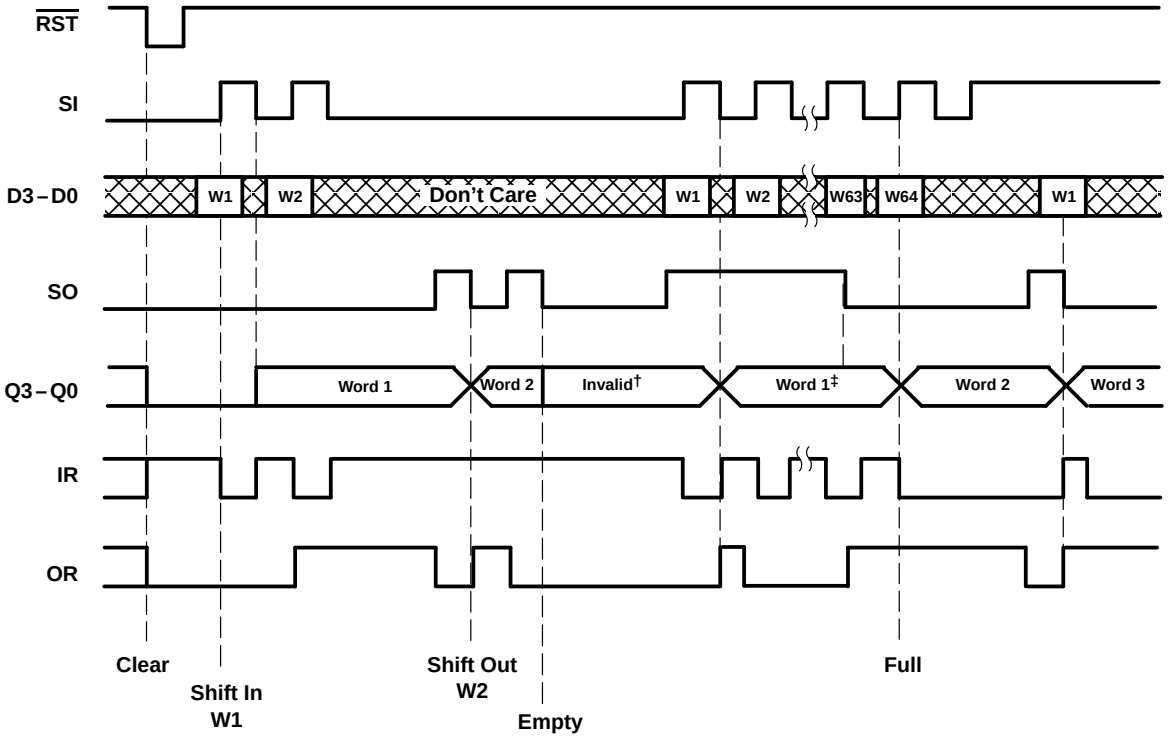


Pin numbers shown are for the DW and N packages.

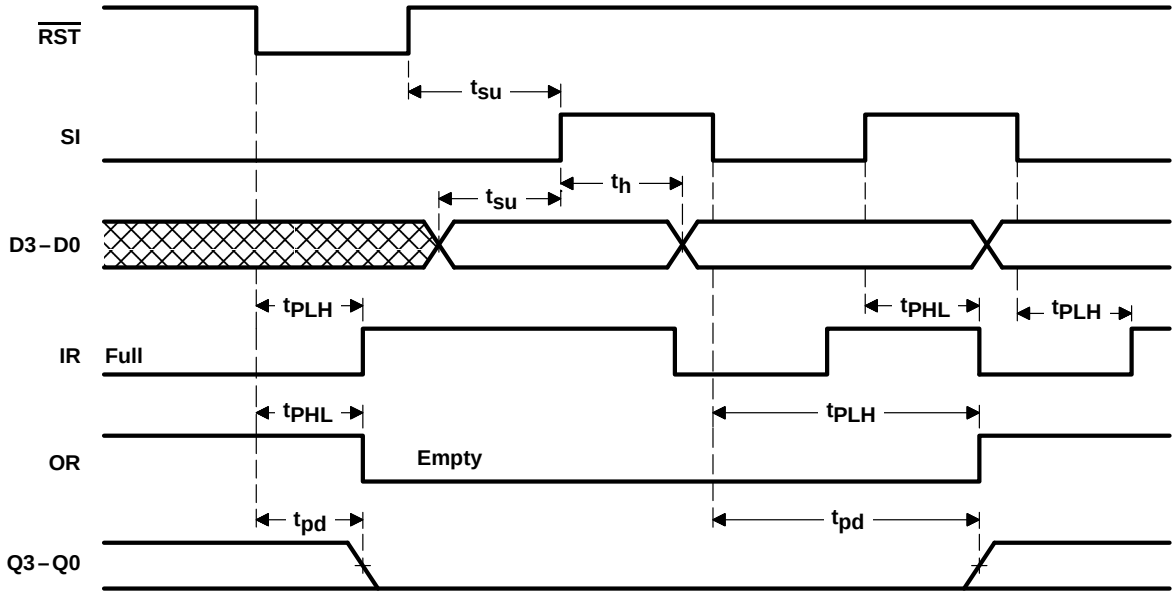
logic diagram (positive logic)



timing diagram

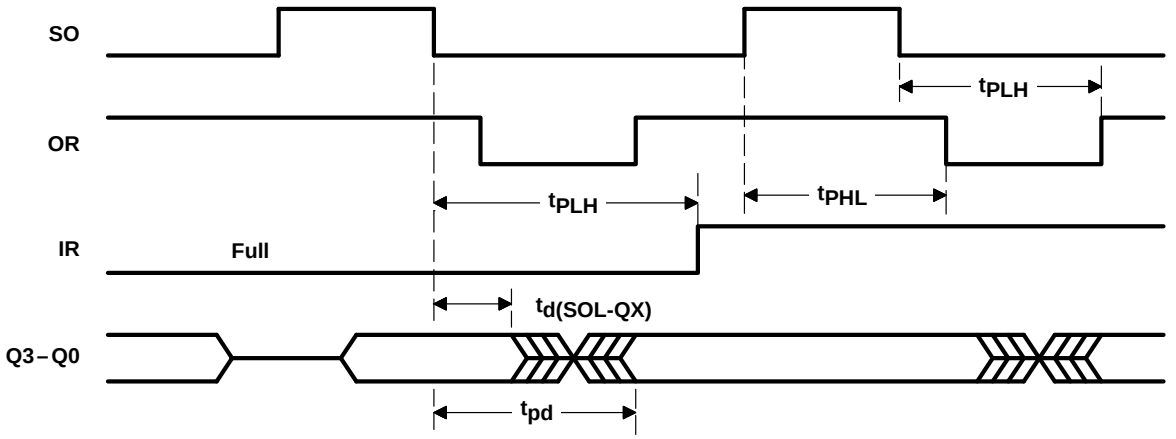


† The last data word shifted out of the FIFO remains at the output until a new word falls through or a $\overline{RST}$ pulse clears the FIFO.
‡ While the output data is considered valid only when the OR flag is high, the stored data remains at the outputs. Any additional words written into the FIFO will stack up behind the first word and will not appear at the output until SO is taken low.



NOTE A: SO is low.

Figure 1. Master Reset and Data-In Waveforms



NOTE A: SI is low.

Figure 2. Data-Out Waveforms

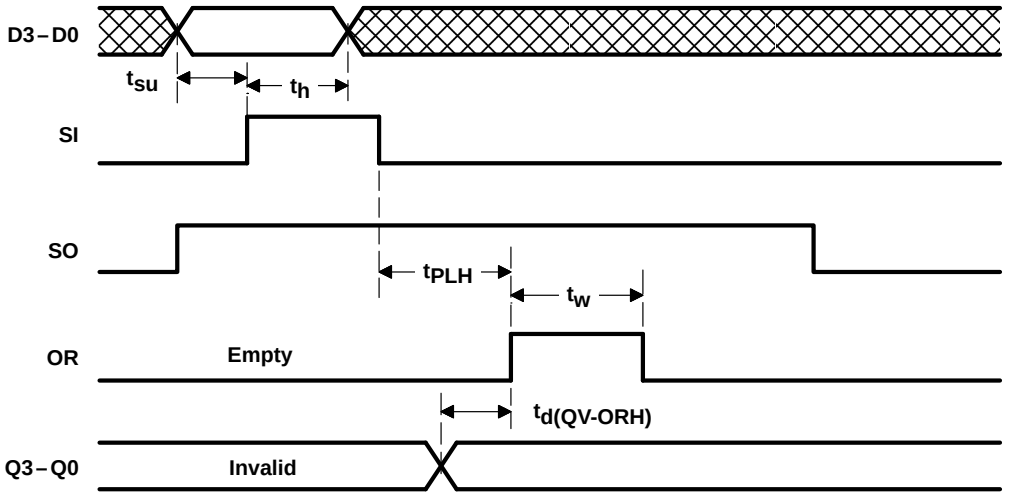


Figure 3. Data Fall-Through Waveforms

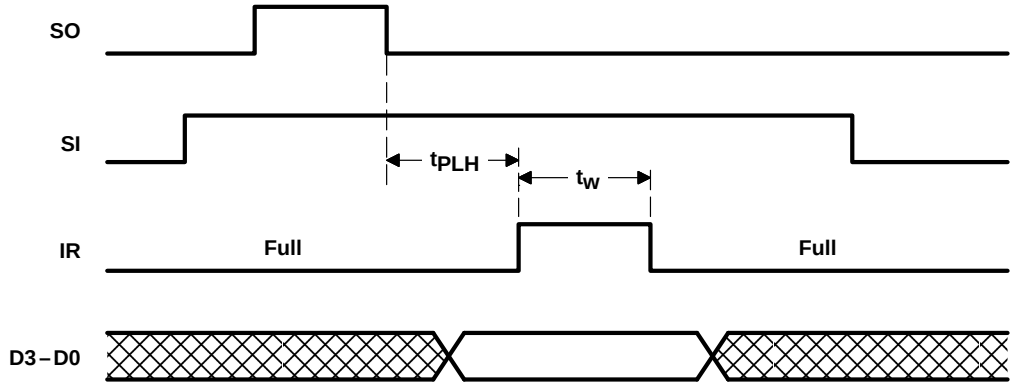


Figure 4. Automatic Data-In Waveforms

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Operating free-air temperature range, T_A . . . . . 0°C to 70°
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage			4.5	5	5.5	V
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
I_{OH}	High-level output current	Q outputs				– 2.6	mA
		IR and OR				– 0.4	
I_{OL}	Low-level output current	Q outputs				24	mA
		IR and OR				8	
f_{clock}	Clock frequency	SI or SO		0		30	MHz
t_w	Pulse duration	SI or SO	High or low	15			ns
		$\overline{RST}$	Low	15			
t_{su}	Setup time before SI↑	Data		0			ns
		$\overline{RST}$	High (inactive)	15			
t_h	Hold time, data after SI↑			17			ns
T_A	Operating free-air temperature			0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2	V
V_{OH}	Any Q	V_{CC} = 4.5 V	I_{OH} = –1 mA				V
			I_{OH} = –2.6 mA	2.4	3.2		
	IR, OR	V_{CC} = 4.5 V,	I_{OH} = –0.4 mA	2.7	3.4		
V_{OL}	Any Q	V_{CC} = 4.5 V	I_{OL} = 12 mA		0.25	0.4	V
			I_{OL} = 24 mA		0.35	0.5	
	IR, OR	V_{CC} = 4.5 V	I_{OL} = 4 mA		0.25	0.4	
			I_{OL} = 8 mA		0.35	0.5	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			–0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	–30		–112	mA
I_{CC}		V_{CC} = 5.5 V	Low		100	145	mA
			High		97	142	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 6)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}	SI			35		30		MHz
	SO			35		30		
t_w‡	IR high			15		8		ns
t_w§	OR high			19		8		ns
$t_{d(QV-ORH)}$	Q valid before OR↑			6	9	−5	12	ns
$t_{d(SOL-QX)}$	Q valid after SO↓			13		4		ns
t_{pd}	SI↓	Q		600	800	350	1000	ns
t_{PHL}	SI↑	IR		20	26	8	30	ns
t_{PLH}	SI↓			16	21	6	25	
t_{PLH}#	SI↓	OR		600	800	350	1000	ns
t_{pd}	SO↓	Q		13	17	4	22	ns
t_{PHL}	SO↑	OR		23	27	7	33	ns
t_{PLH}	SO↓			20	24	6	30	
t_{PLH}#	SO↓	IR		600	800	350	1000	ns
t_{PHL}	RST↓	OR		22	26	10	34	ns
t_{PLH}		IR		17	21	6	27	
t_{PHL}	$\overline{RST}$↓	Q	14	14	17	5	19	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ The IR output pulse occurs when the FIFO is full, SI is high, and SO is pulsed (see Figure 4).
§ The OR output pulse occurs when the FIFO is empty, SO is high, and SI is pulsed (see Figure 3).
¶ Data throughput or fall-through times

APPLICATION INFORMATION

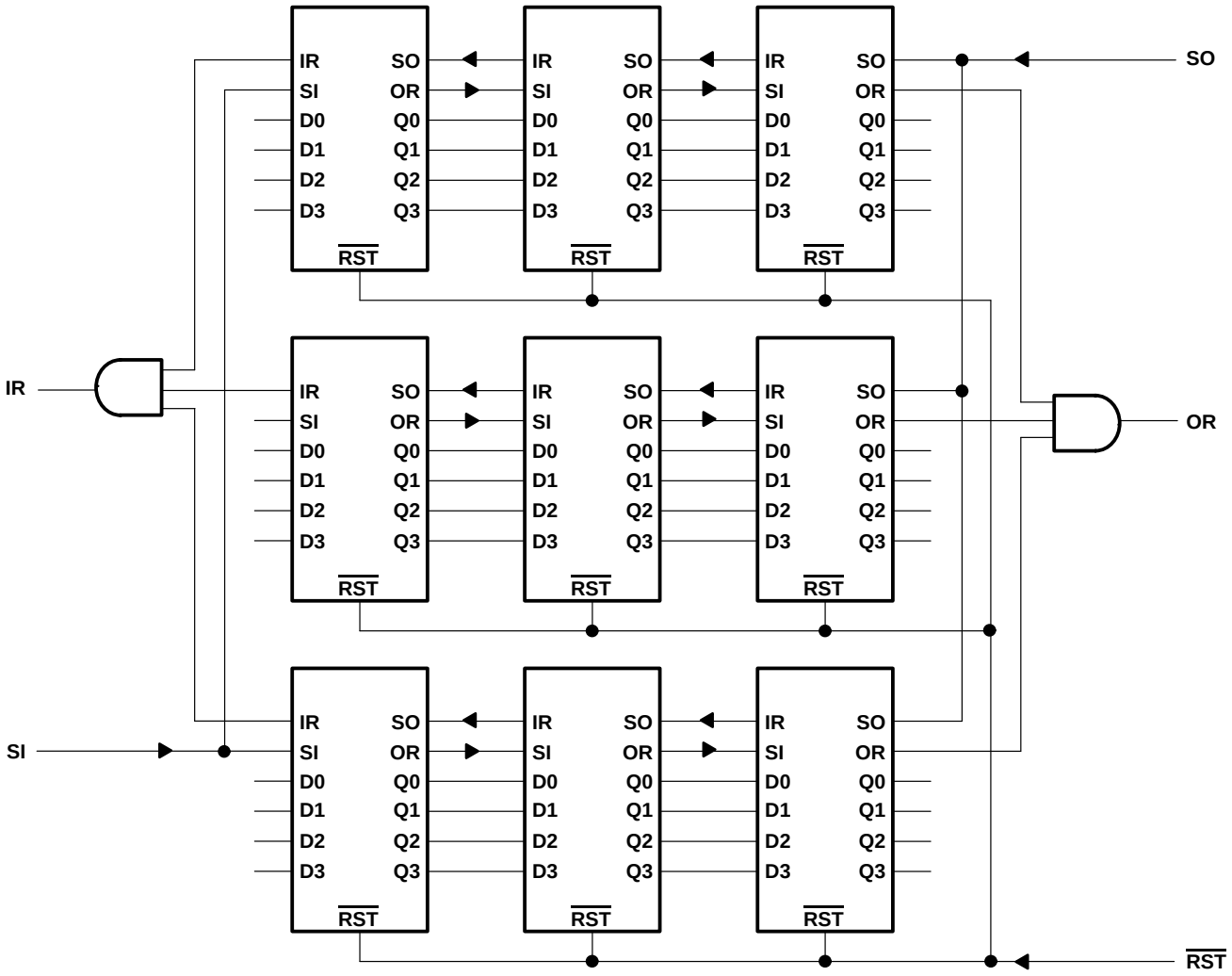
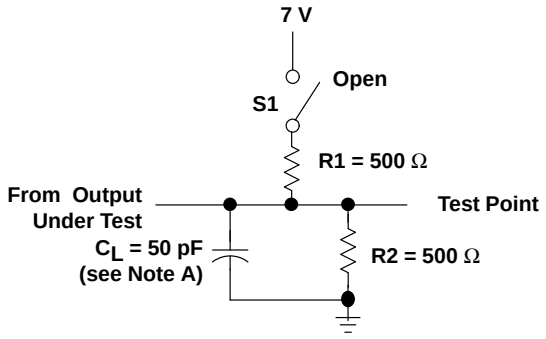


Figure 5. 192-Word by 12-Bit Expansion

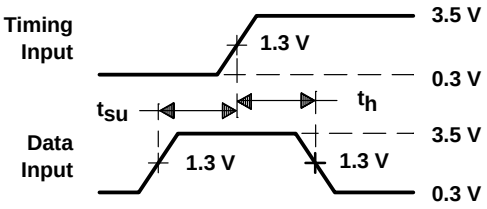
PARAMETER MEASUREMENT INFORMATION



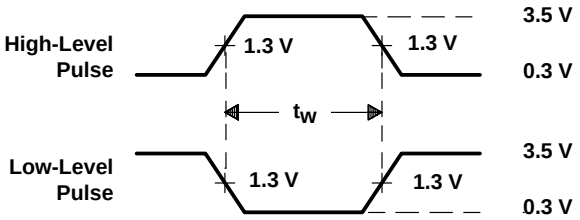
LOAD CIRCUIT FOR 3-STATE OUTPUTS

SWITCH POSITION TABLE

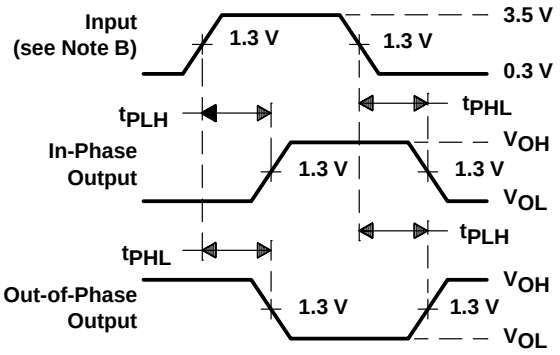
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



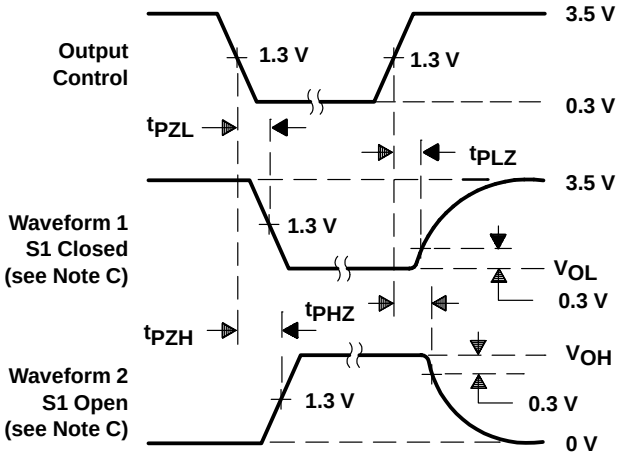
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 6. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.