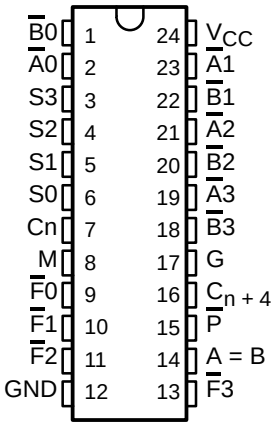
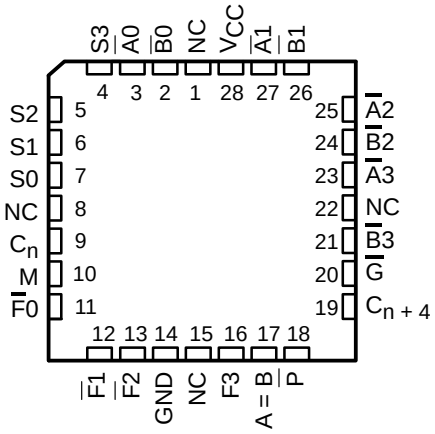
SDAS093A – D2661, DECEMBER 1985 – REVISED MAY 1986

- **Package Options Include Compact 300-mil or Standard 600-mil DIPs and Both Plastic and Ceramic Chip Carriers**
- **Full Look-Ahead for High-Speed Operations on Long Words**
- **Arithmetic Operating Modes:**
  - **Addition**
  - **Subtraction**
  - **Shift Operand A One Position**
  - **Magnitude Comparison**
- **Plus Twelve Other Arithmetic Operations**
- **Logic Function Modes**
  - **Exclusive-OR**
  - **Comparator**
  - **AND, NAND, OR, NOR**
- **Dependable Texas Instruments Quality and Reliability**

SN54AS181B . . . JT OR JW PACKAGE
SN74AS181B . . . N OR NT PACKAGE
(TOP VIEW)

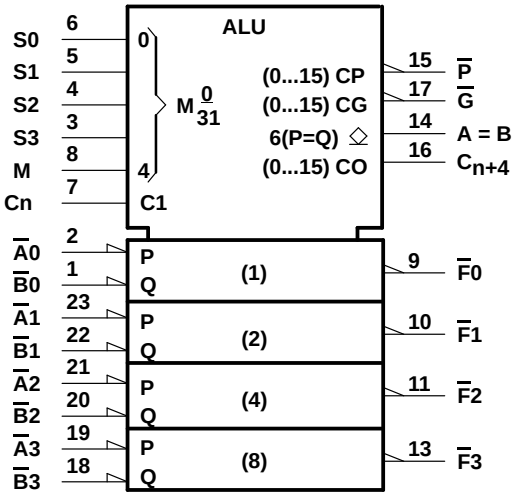


SN54AS181B . . . FK PACKAGE
SN74AS181B . . . FN PACKAGE
(TOP VIEW)



NC–No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for J, JT, N, and NT packages.

TYPICAL ADDITION TIMES (C_L = 15 pF, R_L = 280 Ω, T_A = 25°C)

NUMBER OF BITS	ADDITION TIMES			PACKAGE COUNT		CARRY METHOD BETWEEN ALUs
	USING 'AS181B AND 'AS882	USING 'AS881B AND 'AS882	USING 'S181 AND 'S182	ARITHMETIC LOGIC UNITS	LOOK-AHEAD CARRY GENERATORS	
1 to 4	5 ns	5 ns	11 ns	1		None
5 to 8	10 ns	10 ns	18 ns	2		Ripple
9 to 16	14 ns	14 ns	19 ns	3 or 4	1	Full Look-Ahead
17 to 64	19 ns	19 ns	28 ns	5 to 16	2 to 5	Full Look-Ahead

description

The ’AS181B arithmetic logic units (ALU)/function generators have a complexity of 75 equivalent gates on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs, $\overline{G}$ and $\overline{P}$, for the four bits in the package. When used in conjunction with the SN54AS882 or SN74AS882 full carry look-ahead circuits, high-speed arithmetic operations can be performed. The typical addition times shown previously illustrate the little additional time required for addition of longer words when full carry look-ahead is employed. The method of cascading ’AS882 circuits with these ALUs to provide multilevel full carry look-ahead is illustrated under signal designations.

If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

The ’AS181B will accommodate active-high or active-low data if the pin designations are interpreted as follows:

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-low data (Table 1)	$\overline{A0}$	$\overline{B0}$	$\overline{A1}$	$\overline{B1}$	$\overline{A2}$	$\overline{B2}$	$\overline{A3}$	$\overline{B3}$	$\overline{F0}$	$\overline{F1}$	$\overline{F2}$	$\overline{F3}$	$\overline{C_n}$	$\overline{C_{n+4}}$	$\overline{P}$	$\overline{G}$
Active-low data (Table 2)	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3	$\overline{C_n}$	$\overline{C_{n+4}}$	X	Y

Subtraction is accomplished by 1’s complement addition where the 1’s complement of the subtrahend is generated internally. The resultant output is A–B–1 , which requires an end-around or forced carry to provide A–B.

The ’AS181B can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU must be in the subtract mode with C_n = H when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU must be placed in the subtract mode by placing the function select input S3, S2, S1, S0 at L, H, H, L, respectively.

INPUT C_n	OUTPUT C_{n+4}	ACTIVE-LOW DATA (Figure 1)	ACTIVE-HIGH DATA Figure 2)
H	H	A ≥ B	A ≤ B
H	L	A < B	A > B
L	H	A > B	A < B
L	L	A ≤ B	A ≥ B

These circuits have been designed to not only incorporate all of the designer’s requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

signal designations

In both Figures 1 and 2, the polarity indicators (◺) indicate that the associated input or output is active-low with respect to the function shown inside the symbol and the symbols are the same in both figures. The signal designations in Figure 1 agree with the indicated internal functions based on active-low data, and are for use with the logic functions and arithmetic operations shown in Table 1. The signal designations have been changed in Figure 2 to accommodate the logic functions and arithmetic operations for the active-high data given in Table 2. The 'AS181B together with 'AS882 and 'S182 can be used with the signal designation of either Figure 1 or Figure 2.

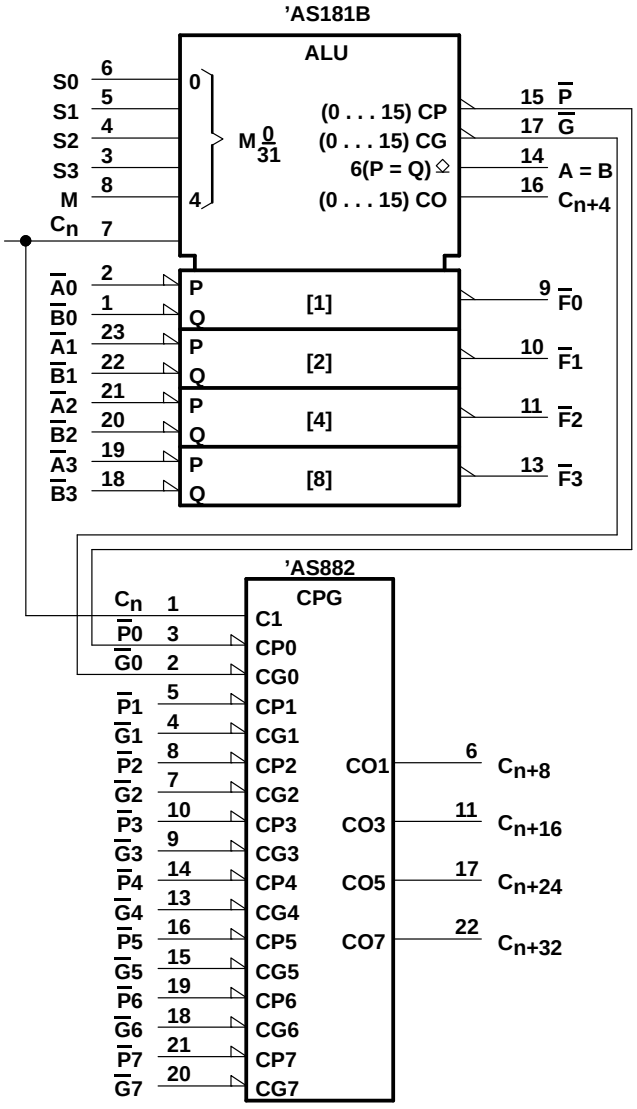


Figure 1
(Use With Table 1)

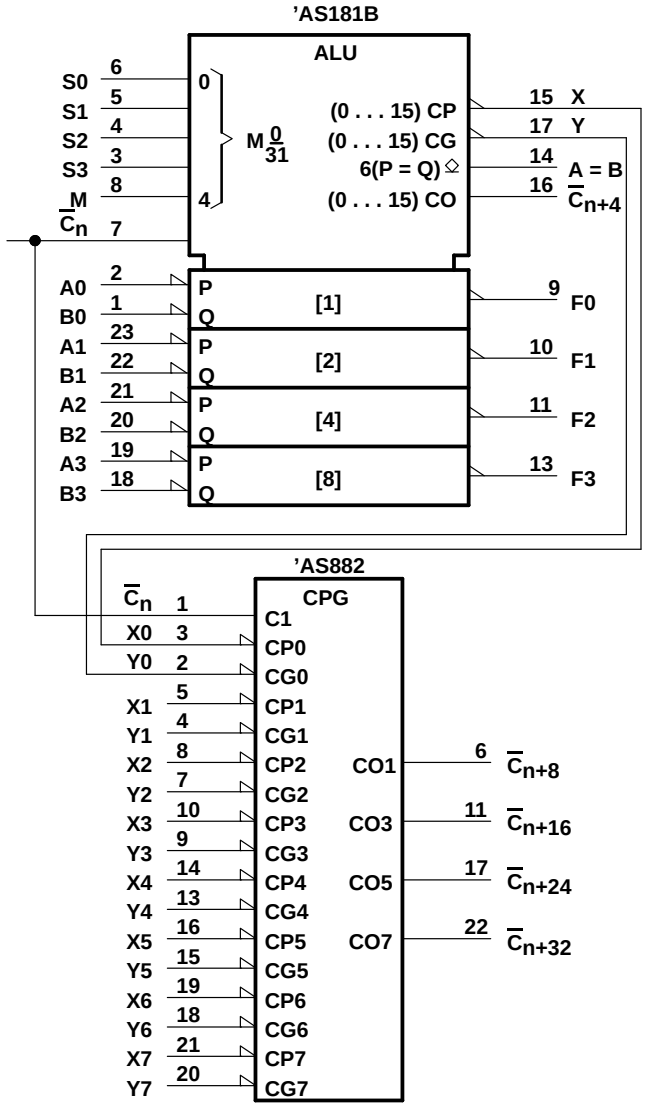


Figure 2
(Use With Table 2)

TABLE 1

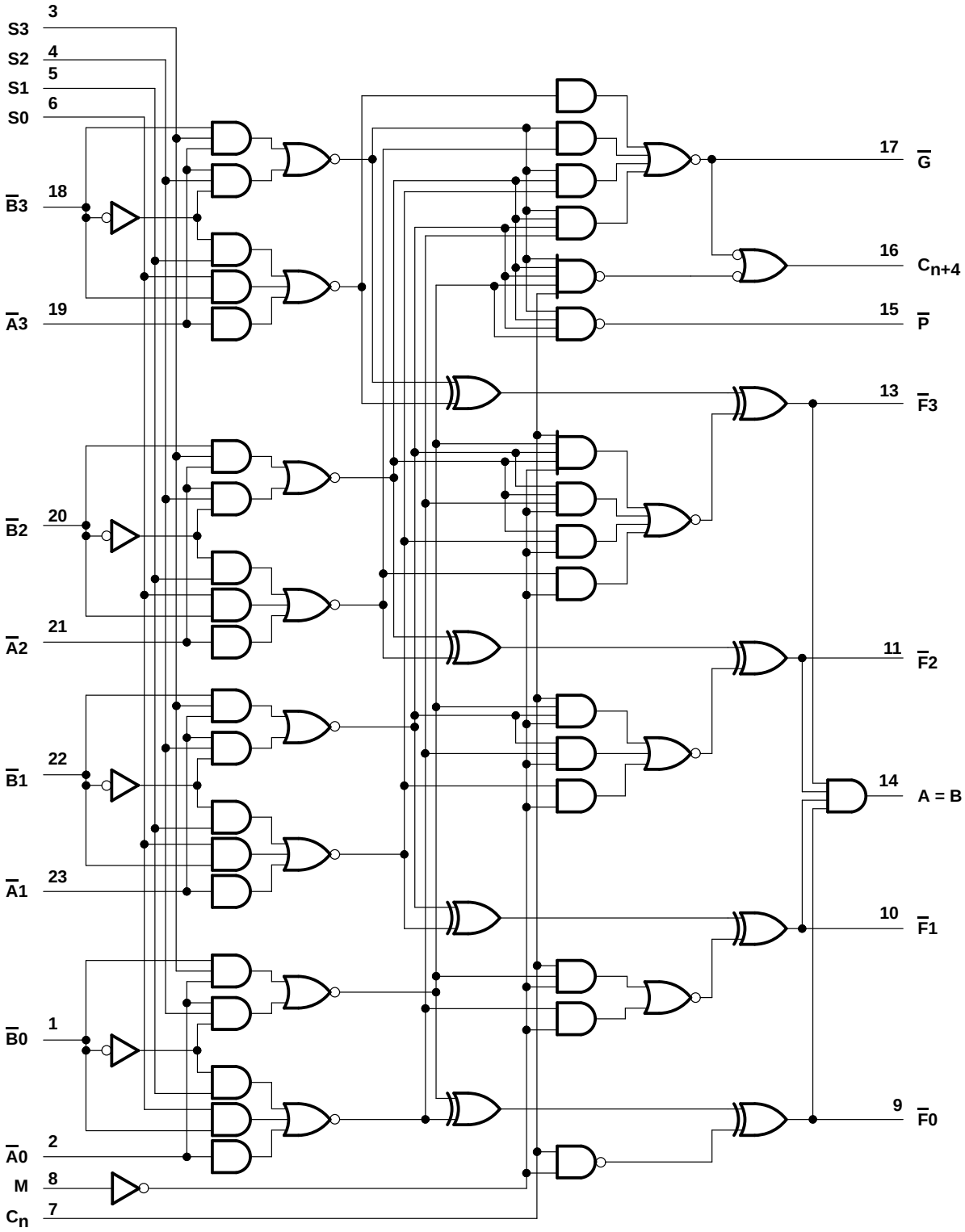
SELECTION				ACTIVE-LOW DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
				LOGIC	C_n = L	C_n = H
S3	S2	S1	S0	FUNCTIONS	(no carry)	(with carry)
L	L	L	L	F = $\overline{A}$	F = A MINUS 1	F = A
L	L	L	H	F = $\overline{AB}$	F = AB MINUS 1	F = AB
L	L	H	L	F = $\overline{A}$ + B	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
L	L	H	H	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	F = $\overline{A + B}$	F = A PLUS (A + $\overline{B}$)	F = A PLUS (A + $\overline{B}$) PLUS 1
L	H	L	H	F = $\overline{B}$	F = AB PLUS (A + $\overline{B}$)	F = AB PLUS (A + $\overline{B}$) PLUS 1
L	H	H	L	F = $\overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
H	L	L	L	F = $\overline{A}$B	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H	L	L	H	F = A ⊕ B	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = A$\overline{B}$ PLUS (A + B)	F = A$\overline{B}$ PLUS (A + B) PLUS 1
H	L	H	H	F = A ⊕ B	F = (A + B)	F = (A + B) PLUS 1
H	H	L	L	F = 0	F = A PLUS A[	F = A PLUS A PLUS 1
H	H	L	H	F = A$\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H	H	H	L	F = AB	F = A$\overline{B}$ PLUS A	F =A$\overline{B}$ PLUS A PLUS 1
H	H	H	H	F = A	F = A PLUS 1	F = A PLUS 1

TABLE 2

SELECTION				ACTIVE-LOW DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
				LOGIC	$\overline{C}_n$ = L	$\overline{C}_n$ = H
S3	S2	S1	S0	FUNCTIONS	(no carry)	(with carry)
L	L	L	L	F = $\overline{A}$	F = A	F = A PLUS 1
L	L	L	H	F = $\overline{A + B}$	F = A + B	F = (A+ B) PLUS 1
L	L	H	L	F = $\overline{A}$B	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
L	L	H	H	F = 0	F = MINUS 1 (2's COMPL)	F = ZERO
L	H	L	L	F = $\overline{AB}$	F = A PLUS A$\overline{B}$	F = A PLUS A$\overline{B}$ PLUS 1
L	H	L	H	F = $\overline{B}$	F = (A + B) PLUS A + $\overline{B}$	F =(A + B) PLUS A$\overline{B}$ PLUS 1
L	H	H	L	F = A ⊕ B	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A$\overline{B}$	F = A$\overline{B}$ MINUS 1	F = A $\overline{B}$
H	L	L	L	F = $\overline{A}$ + B	F = A PLUS AB	F = A PLUS AB PLUS 1
H	L	L	H	F = $\overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = (A + $\overline{B}$) PLUS AB	F = (A + $\overline{B}$) PLUS AB PLUS 1
H	L	H	H	F = AB	F = AB MINUS 1	F = AB
H	H	L	L	F = 1	F = A PLUS A†	F = A PLUS A PLUS 1
H	H	L	H	F = A + $\overline{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) PLUS A	F =(A + $\overline{B}$) PLUS A PLUS 1
H	H	H	H	F = A	F = A MINUS 1	F = A

† Each bit is shifted to the next more significant position.

logic diagram (positive logic)



Pin numbers shown are for JT, JW, N, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage (A = B output only) . . . . . 7 V
Operating free-air temperature range: SN54AS181B . . . . . –55°C to 125°C
SN74AS181B . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

recommended operating conditions

			SN54AS181B			SN74AS181B			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{OH}	High-level output voltage	A = B output only			5.5			5.5	V
I_{OH}	High-level output current	All outputs except A = B and $\overline{G}$			–2			–2	mA
		$\overline{G}$			–3			– 3	
I_{OL}	Low-level output current	All outputs except $\overline{G}$			20			20	mA
		$\overline{G}$			48			48	
T_A	Operating free-air temperature		–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS181B			SN74AS181B			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}	Any output except A = B	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –2 mA	V_{CC}–2			V_{CC}–2			V
	$\overline{G}$	V_{CC} = 4.5 V,	I_{OH} = –3 mA	2.4	3.4		2.4	3.4		V
V_{OL}	Any output except $\overline{G}$	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
	$\overline{G}$	V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.4	0.5		0.4	0.5	V
I_{OH}	A = B	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
I_I	M input	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	Any A or B input					0.3			0.3	
	Any S input					0.4			0.4	
	Carry input					0.6			0.6	
I_{IH}	M input	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
	Any A or B input					60			60	
	Any S input					80			80	
	Carry input					120			120	
I_{IL}	M input	V_{CC} = 5.5 V,	V_I = 0.4 V			–0.5			–0.5	mA
	Any A or B input					–1.5			–1.5	
	Any S input					–2			–2	
	Carry input					–3			–3	
I_O‡	All outputs except A = B and $\overline{G}$	V_{CC} = 5.5 V,	V_O = 2.25 V	–30	–45	–112	–30	–45	–112	mA
	$\overline{G}$			–30		–125	–30		–125	
I_{CC}		V_{CC} = 5.5 V			74	117		74	117	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
				SN54AS181B		SN74AS181B		
				MIN	MAX	MIN	MAX	
t_{PLH}	C_n	C_{n+4}		3	9	3	8.5	ns
t_{PHL}				2	7	2	6.5	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	C_{n+4}	M = 0 V, S1 = S2 = 0 V,	3.5	13	3.5	12	ns
t_{PHL}			S0 = S3 = 4.5 V (SUM mode)	3.5	12.5	3.5	12	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	C_{n+4}	M = 0 V, S0 = S3 = 0 V,	5	14.5	5	13	ns
t_{PHL}			S1 = S2 = 4.5 V (DIFF mode)	5	13.5	5	12.5	
t_{PLH}	C_n	Any $\overline{F}$	M = 0 V (SUM or DIFF mode)	3	10.5	3	9	ns
t_{PHL}				3	8	3	7.5	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M = 0 V, S1 = S2 = 0 V,	3	8.5	3	8	ns
t_{PHL}			S0 = S3 = 4.5 V (SUM mode)	2	7	2	6	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M = 0 V, S0 = S3 = 0 V,	3	10.5	3	9.5	ns
t_{PHL}			S1 = S2 = 4.5 V (DIFF mode)	2	9	2	7	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{P}$	M = 0 V, S1 = S2 = 0 V,	3	8.5	3	7.5	ns
t_{PHL}			S0 = S3 = 4.5 V (SUM mode)	2	7.5	2	6	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{P}$	M = 0 V, S0 = S3 = 0 V,	3	10.5	3	9	ns
t_{PHL}			S1 = S2 = 4.5 V (DIFF mode)	3	8.5	3	8	
t_{PLH}	$\overline{A}i$ or $\overline{B}i$	$\overline{F}i$	M = 0 V, S1 = S2 = 0 V,	3	11	3	9.5	ns
t_{PHL}			S0 = S3 = 4.5 V (SUM mode)	3	9	3	7.5	
t_{PLH}	$\overline{A}i$ or $\overline{B}i$	$\overline{F}i$	M = 0 V, S0 = S3 = 0 V,	3	12	3	10.5	ns
t_{PHL}			S1 = S2 = 4.5 V (DIFF mode)	3	11	3	9.5	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	Any $\overline{F}$	M = 0 V, S1 = S2 = 0 V,	3	13.5	3	12	ns
t_{PHL}			S0 = S3 = 4.5 V (SUM mode)	3	13	3	11.5	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	Any $\overline{F}$	M = 0 V, S0 = S3 = 0 V,	3	16	3	14.5	ns
t_{PHL}			S1 = S2 = 4.5 V (DIFF mode)	3	13	3	12.5	
t_{PLH}	$\overline{A}i$ or $\overline{B}i$	$\overline{F}i$	M = 4.5 V (LOGIC mode)	3	12.5	3	11	ns
t_{PHL}				3	10	3	9.5	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	A = B	M = 0 V, S0 = S3 = 0 V,	4	19	4	17	ns
t_{PHL}			S1 = S2 = 4.5 V (DIFF mode)	5	18.5	5	15	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

PARAMETER MEASUREMENT INFORMATION

SUM MODE TEST TABLE
FUNCTION INPUTS: S0 = S3 = 4.5 V, S1 = S2 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE 1)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}i$	In-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}i$	In-Phase
t_{PLH} t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH} t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}	In-Phase
t_{PLH} t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	Out-of-Phase

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

PARAMETER MEASUREMENT INFORMATION

DIFF MODE TEST TABLE

FUNCTION INPUTS: S1 = S2 = 4.5 V, S0 = S3 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE 1)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} / t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{A}$	Remaining B, C_n	$\overline{F}i$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$	Remaining B, C_n	$\overline{F}i$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	Out-of-Phase
t_{PLH} / t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	$C_n + 4$ or any $\overline{F}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$, $\overline{B}$, C_n	$C_n + 4$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	None	Remaining $\overline{A}$, $\overline{B}$, C_n	$C_n + 4$	In-Phase

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

PARAMETER MEASUREMENT INFORMATION

LOGIC MODE TEST TABLE
FUNCTION INPUTS: S1 = S2 = M = 4.5 V, S0 = S3 = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (see Note 1)
		APPLY 4.5 V	APPLY GND	APPLY GND	APPLY 4.5 V		
t_{PLH} / t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}i$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}i$	Out-of-Phase

INPUT BITS EQUAL/NOT EQUAL TEST TABLE
FUNCTION INPUTS: S0 = S3 = M = 4.5 V, S1 = S2 = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE 1)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} / t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$	Out-of-Phase
t_{PLH}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$	In-Phase
t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$	In-Phase
t_{PLH}	$\overline{B}i$	None	$\overline{A}i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$	In-Phase
t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_{n+4}	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_{n+4}	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_{n+4}	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_{n+4}	Out-of-Phase

INPUT PAIRS HIGH/NOT HIGH TEST TABLE
FUNCTION INPUTS: S2 = M = 4.5 V, S0 = S1 = S3 = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE 1)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} / t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	Remaining $\overline{A}$, C_n	Remaining $\overline{B}$	$\overline{P}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{P}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	Remaining $\overline{A}$, C_n	Remaining $\overline{B}$	C_{n+4}	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	C_{n+4}	Out-of-Phase

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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