DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

SDAS062A – D2661, APRIL 1982 – REVISED MAY 1986

- **3-State Bus Driving Outputs**
- **Full Parallel-Access for Loading**
- **Buffered Control Inputs**
- **Choice of True or Inverting Logic**
  - **'ALS878A, 'AS878 True Outputs**
  - **'ALS879A, 'AS879 Inverting Outputs**
- **Synchronous Clear**
- **Package Options Include Plastic Small Outline Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

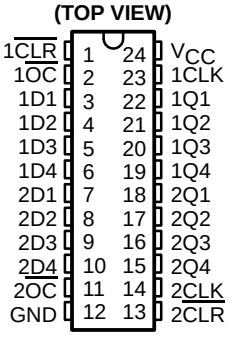
description

These dual 4-bit registers feature 3-state outputs designed specifically for bus driving. This makes these devices particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

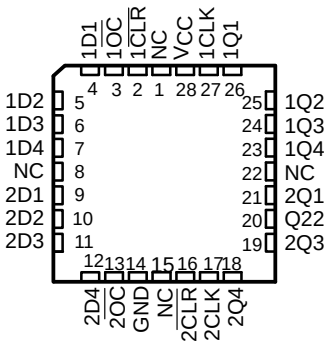
The dual 4-bit edge-triggered flip-flops enter data on the low-to-high transition of the clock (1CLK and 2CLK). All types have individual synchronous clear inputs and output control pins for each group of 4-bit registers.

The SN54ALS' and SN54AS' devices are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS' and SN74AS' devices are characterized for operation from 0°C to 70°C.

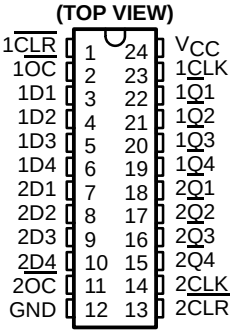
SN54ALS878A, SN54AS878 . . . JT PACKAGE
SN74ALS878A, SN74AS878 . . . DW OR NT PACKAGE
(TOP VIEW)



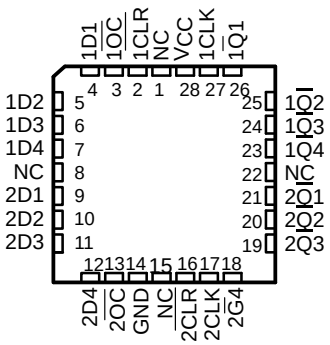
SN54ALS878A, SN54AS878 . . . FK PACKAGE
SN74ALS878A, SN74AS878 . . . FN PACKAGE
(TOP VIEW)



SN54ALS879A, SN54AS879 . . . JT PACKAGE
SN74ALS879A, SN74AS879 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ALS879A, SN54AS879 . . . FK PACKAGE
SN74ALS879A, SN74AS879 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLES

'ALS878A, 'AS878 (each flip-flop)

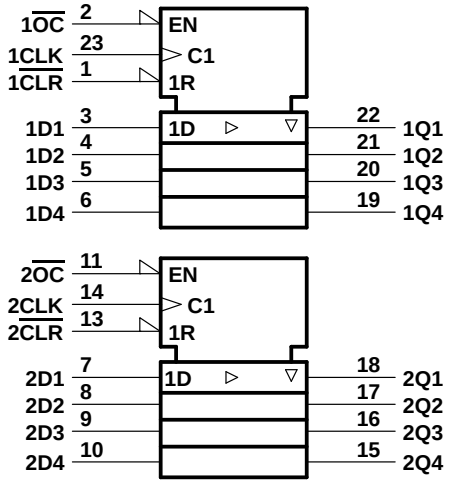
INPUTS				OUTPUT
$\overline{OC}$	$\overline{CLR}$	CLK	D	Q
L	L	↑	X	L
L	H	↑	H	H
L	H	↑	L	L
L	H	L	X	Q_0
H	X	X	X	Z

'ALS879A, 'AS879 (each flip-flop)

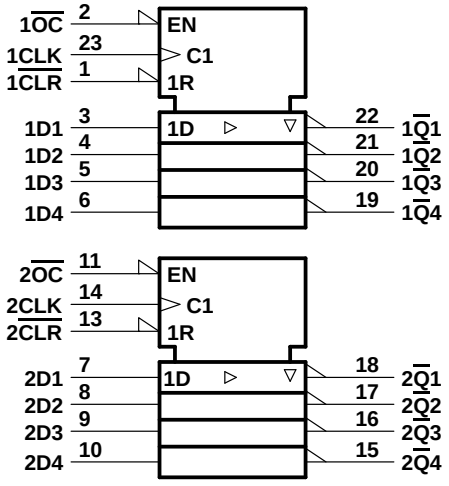
INPUTS				OUTPUT
$\overline{OC}$	$\overline{CLR}$	CLK	D	$\overline{Q}$
L	L	↑	X	H
L	H	↑	H	L
L	H	↑	L	H
L	H	L	X	Q_0
H	X	X	X	Z

logic symbols †

'ALS878A, 'AS878



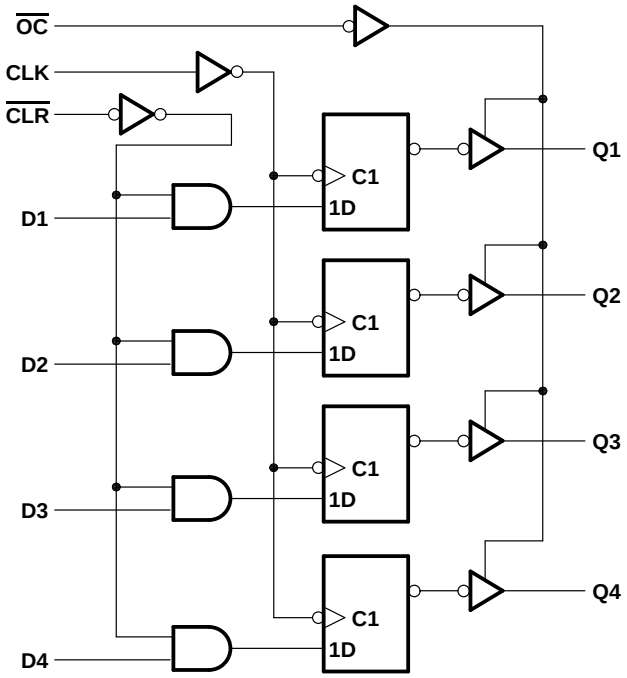
'ALS879A, 'AS879



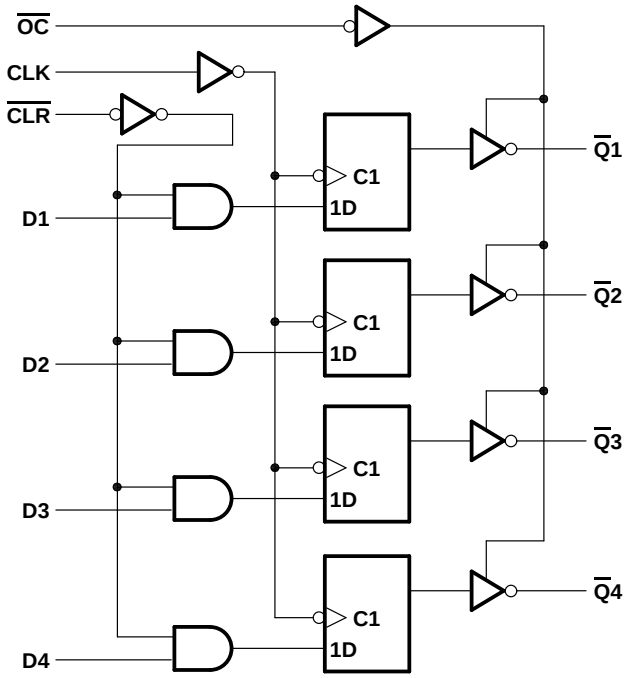
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

logic diagrams (positive logic)

'ALS878A, 'AS878
(each quad flip-flop)



'ALS879A, 'AS879
(each quad flip-flop)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS878A, SN54ALS879A . . . . . –55°C to 125°C
SN74ALS878A, SN74ALS879A . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

recommended operating conditions

			SN54ALS878A SN54ALS879A			SN74ALS878A SN74ALS879A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				–1			–2.6	mA
I_{OL}	Low-level output current				12			24	mA
f_{clock}	Clock frequency	’ALS878A	0		25	0		30	MHz
		’ALS879A	0		20	0		25	
t_w	Pulse duration	’ALS878A CLK high or low	20			16.5			ns
		’ALS879A CLK high or low	25			20			
tsu	Setup time before CLK↑	Data	15			15			ns
		$\overline{CLR}$	20			20			
t_h	Hold time after CLK↑	Data	4			4			ns
		$\overline{CLR}$	0			0			
T_A	Operating free-air temperature		–55		125	0		70°	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS878A SN54ALS879A			SN74ALS878A SN74ALS879A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –0.4 mA	V_{CC}–2			V_{CC}–2			V
	V_{CC} = 4.5 V,	I_{OH} = –1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = –2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2. 7 V			20			20	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			–20			–20	µA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0 .4 V			–0.2			–0.2	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	–30		–112	–30		–112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		14	23		14	23	mA
		Outputs low		18	31		18	31	
		Outputs disabled		20	33		20	33	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS878A 'ALS879A			SN54ALS878A SN54ALS879A		SN74ALS878A SN74ALS879A		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	'ALS878A		40	50		25		30		MHz
	'ALS879A		40	50		20		25		
t_{PLH}	CLK	Q or $\overline{Q}$		8	10	4	15	4	14	ns
t_{PHL}				9	13	4	17	4	16	
t_{PZH}	$\overline{OC}$	Q or $\overline{Q}$		9	13	4	22	4	20	ns
t_{PZL}				11	15	4	22	4	20	
t_{PHZ}	$\overline{OC}$	Q or $\overline{Q}$		6	8	2	12	2	10	ns
t_{PLZ}				7	10	3	18	3	15	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS878, SN54AS879 . . . . . –55°C to 125°C
SN74AS878, SN74AS879 . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

recommended operating conditions

			SN54AS878 SN54AS879			SN74AS878 SN74AS879			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				–12			–15	mA
I_{OL}	Low-level output current				32			48	mA
f_{clock}	Clock Frequency		0		100	0		125	MHz
t_w	Pulse duration	CLK low	4			2			ns
		CLK high	5			4			
tsu	Setup time before CLK↑	Data	3			2			ns
		$\overline{CLR}$	6.5			5.5			
t_h	Hold time after CLK↑	Data	3			2			ns
		$\overline{CLR}$	0			0			
T_A	Operating free-air temperature		–55		125	0		70°	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS878 SN54AS879			SN74AS878 SN74AS879			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –2 mA	V_{CC}–2			V_{CC}–2			V
		V_{CC} = 4.5 V,	I_{OH} = –12 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = –15 mA				2.4	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.29	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.33	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	µA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			–50			–50	µA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	D	V_{CC} = 5.5 V,	V_I = ?0.4 V			–3			–2	mA
	All other					–0.5			–0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	–30		–112	–30		–112	mA
I_{CC}	’AS878	V_{CC} = 5.5 V, See Note 2	Outputs high		82	132		82	132	mA
			Outputs low		96	155		96	155	
			Outputs disabled		100	160		100	160	
	’AS879		Outputs high		88	142		88	142	
			Outputs low		94	150		94	150	
			Outputs disabled		100	160		100	160	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 2: I_{CC} is measured with $\overline{CLR}$ and all D inputs grounded, and CLK and $\overline{OC}$ at 4.5 V.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS878 SN54AS879		SN74AS878 SN74AS879		
			MIN	MAX	MIN	MAX	
t_{max}			100		125		MHz
t_{PLH}	CLK	Q or $\overline{Q}$	3	11.5	3	8.5	ns
t_{PHL}			4	12.5	4	10.5	
t_{PZH}	$\overline{OC}$	Q or $\overline{Q}$	2	8	2	7	ns
t_{PZL}			3	11.5	3	10.5	
t_{PHZ}	$\overline{OC}$	Q or $\overline{Q}$	2	7	2	6	ns
t_{PLZ}			2	7	2	6	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.