- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **pnp Inputs Reduce dc Loading**
- **Data Flow-Through Pinout (All Inputs on Opposite Side From Outputs)**
- **Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

These octal buffers and line drivers are designed to have the performance of the popular SN54ALS240A / SN74ALS240A series and, at the same time, offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly facilitates printed-circuit-board layout.
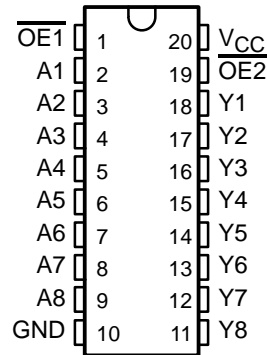
The 3-state control gate is a 2-input NOR such that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all eight outputs are in the high-impedance state.

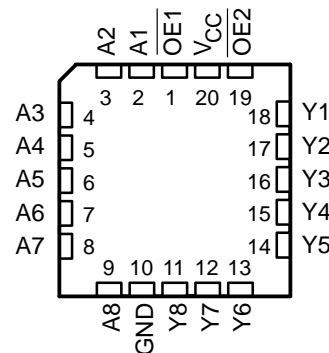The SN74ALS540 provides inverted data. The ′ALS541 provide true data at the outputs.

The -1 versions of SN74ALS540 and SN74ALS541 are identical to the standard versions, except that the recommended maximum I_{OL} is increased to 48 mA. There is no -1 version of the SN54ALS541.

The SN54ALS541 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS540 and SN74ALS541 are characterized for operation from 0°C to 70°C.

SN54ALS541 . . . J PACKAGE
SN74ALS540, SN74ALS541 . . . DW OR N PACKAGE
(TOP VIEW)

$\overline{OE1}$	1	20	V_{CC}
A1	2	19	$\overline{OE2}$
A2	3	18	Y1
A3	4	17	Y2
A4	5	16	Y3
A5	6	15	Y4
A6	7	14	Y5
A7	8	13	Y6
A8	9	12	Y7
GND	10	11	Y8

SN54ALS541 . . . FK PACKAGE
(TOP VIEW)

Top pins: A2 (3), A1 (2), $\overline{OE1}$ (1), V_{CC} (20), $\overline{OE2}$ (19)

A3	4	18 Y1
A4	5	17 Y2
A5	6	16 Y3
A6	7	15 Y4
A7	8	14 Y5

Bottom pins: A8 (9), GND (10), Y8 (11), Y7 (12), Y6 (13)

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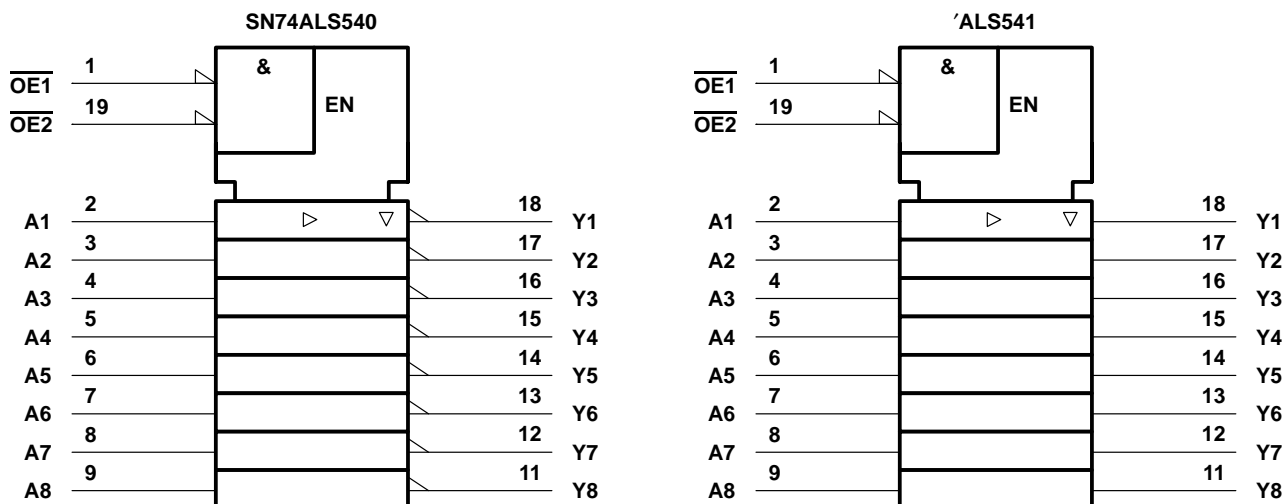
TEXAS INSTRUMENTS

SN54ALS541, SN74ALS540, SN74ALS541
OCTAL BUFFERS AND LINE DRIVERS
WITH 3-STATE OUTPUTS

SDAS025C – APRIL 1982 – REVISED JANUARY 1995

logic symbols†

SN74ALS540

$\overline{OE1}$ 1	& EN
$\overline{OE2}$ 19	

A1	2		18	Y1
A2	3		17	Y2
A3	4		16	Y3
A4	5		15	Y4
A5	6		14	Y5
A6	7		13	Y6
A7	8		12	Y7
A8	9		11	Y8

´ALS541

$\overline{OE1}$ 1	& EN
$\overline{OE2}$ 19	

A1	2		18	Y1
A2	3		17	Y2
A3	4		16	Y3
A4	5		15	Y4
A5	6		14	Y5
A6	7		13	Y6
A7	8		12	Y7
A8	9		11	Y8

† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

SN74ALS540

$\overline{OE1}$ 1
$\overline{OE2}$ 19

A1 2   18 Y1

To Seven Other Channels

´ALS541

$\overline{OE1}$ 1
$\overline{OE2}$ 19

A1 2   18 Y1

To Seven Other Channels
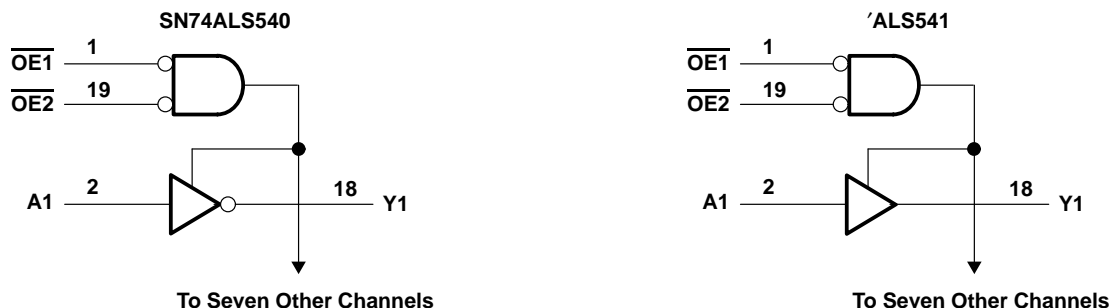
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} .... 7 V
Input voltage, V_I .... 7 V
Voltage applied to a disabled 3-state output .... 5.5 V
Operating free-air temperature range, T_A: SN54ALS541 .... −55°C to 125°C
                         SN74ALS540, SN74ALS541 .... 0°C to 70°C
Storage temperature range .... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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recommended operating conditions

		SN54ALS541			SN74ALS540 SN74ALS541			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
							48[†]	
T_A	Operating free-air temperature	−55		125	0		70	°C

[†] Applies only to the -1 version and only if V_{CC} is between 4.75 V and 5.25 V

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS541			SN74ALS540 SN74ALS541			UNIT
				MIN	TYP[‡]	MAX	MIN	TYP[‡]	MAX	
V_{IK}		$V_{CC} = 4.5$ V,	$I_I = -18$ mA			−1.2			−1.2	V
V_{OH}		$V_{CC} = 4.5$ V to 5.5 V,	$I_{OH} = -0.4$ mA	$V_{CC} - 2$			$V_{CC} - 2$			V
		$V_{CC} = 4.5$ V	$I_{OH} = -3$ mA	2.4	3.2		2.4	3.2		
			$I_{OH} = -12$ mA	2						
			$I_{OH} = -15$ mA				2			
V_{OL}		$V_{CC} = 4.5$ V	$I_{OL} = 12$ mA		0.25	0.4		0.25	0.4	V
			$I_{OL} = 24$ mA					0.35	0.5	
			$I_{OL} = 48$ mA[†]					0.35	0.5	
I_{OZH}		$V_{CC} = 5.5$ V,	$V_O = 2.7$ V			20			20	µA
I_{OZL}		$V_{CC} = 5.5$ V,	$V_O = 0.4$ V			−20			−20	µA
I_I		$V_{CC} = 5.5$ V,	$V_I = 7$ V			0.1			0.1	mA
I_{IH}		$V_{CC} = 5.5$ V,	$V_I = 2.7$ V			20			20	µA
I_{IL}		$V_{CC} = 5.5$ V,	$V_I = 0.4$ V			−0.2			−0.1	mA
I_O[§]		$V_{CC} = 5.5$ V,	$V_O = 2.25$ V	−20		−112	−30		−112	mA
I_{CC}	SN74ALS540	$V_{CC} = 5.5$ V	Outputs high		5	10		5	10	mA
			Outputs low		13	22		13	22	
			Outputs disabled		11	19		11	19	
	'ALS541	$V_{CC} = 5.5$ V	Outputs high		6	14		6	14	
			Outputs low		15	25		15	25	
			Outputs disabled		13.5	32		13.5	22	

[†] Applies only to the -1 version and only if V_{CC} is between 4.75 V and 5.25 V
[‡] All typical values are at $V_{CC} = 5$ V, $T_A = 25$°C.
[§] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX[†]						UNIT
			SN54ALS541		SN74ALS540		SN74ALS541		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	4	17	2	12	4	14	ns
t_{PHL}			2	14	2	9	2	10	
t_{PZH}	$\overline{OE}$	Y	5	18	5	15	5	15	ns
t_{PZL}			8	28	8	20	8	20	
t_{PHZ}	$\overline{OE}$	Y	1	12	1	10	1	10	ns
t_{PLZ}			2	14	2	12	2	12	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES

LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS

LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS

LOAD CIRCUIT
FOR 3-STATE OUTPUTS

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PULSE DURATIONS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
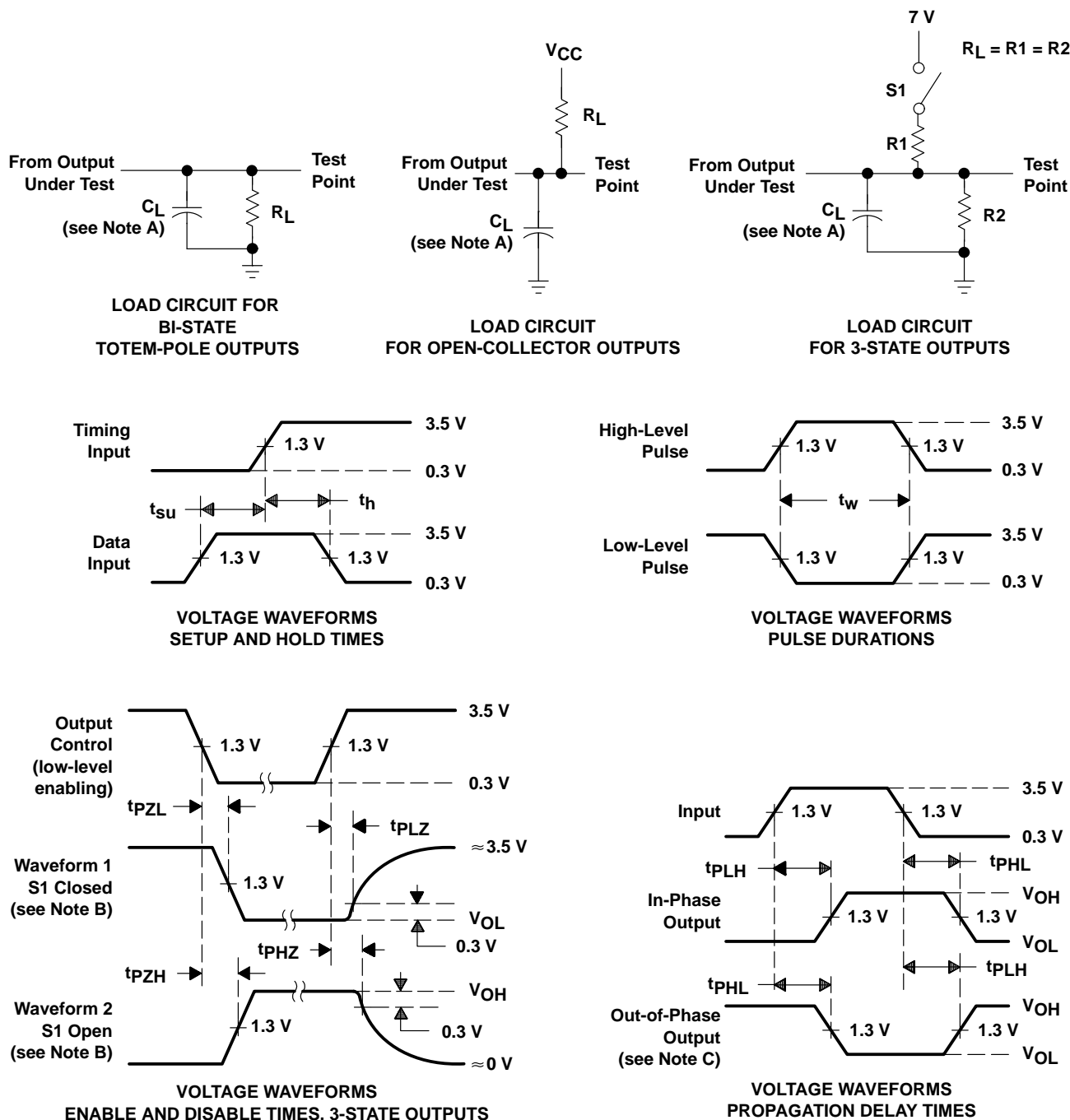
NOTES: A. C_L includes probe and jig capacitance.
   B.   Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
        Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
   C.   When measuring propagation delay items of 3-state outputs, switch S1 is open.
   D.   All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
   E.   The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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