Metastable Characteristics of Texas Instruments Advanced Bipolar Logic Families

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TEXAS INSTRUMENTS

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INTRODUCTION

At some point in every system designers career, they are faced with the problem of synchronizing two digital signals operating at two different frequencies. This problem is typically solved by synchronizing one of the signals, to the local clock, through a flip-flop. However, this solution presents an awkward dilemma, the setup and hold time specifications associated with the flip-flop are sure to be violated. The metastable characteristics of the flip-flop used can influence overall system reliability. The purpose of this application report is to give the system designer a better understanding of the metastable characteristics pertaining to Texas Instruments Advanced Schottky Bipolar Logic Family.

METASTABLE DEFINITION

Whenever a flip-flops setup and hold time is violated, the flip-flops output response is uncertain. Presently, there is no circuit that can 100% guarantee its response. This is why the device manufacturer does not guarantee its operation. Specifically, the metastable state is defined as that time period when the output of a digital logic device, is not at a logic level 1 (V_{out} less than 2 V) or a logic level 0 (V_{out} greater than 0.8 V), but instead between 0.8 V and 2 V. Since the input data is changing at the time of being clocked, the system designer does not care if the flip-flop goes to either a high or low logic level, just so long as the output does not hang up in the metastable region. The metastable characteristics for a particular flip-flop will determine how long the device stays in the metastable region. This concept is illustrated in the timing diagram of Figure 1.

METASTABLE EVALUATION

Anyone who has tried to evaluate the metastable characteristics for a particular flip-flop, has probably found it is not an easy task. The number of times the output hangs up in the metastable region is extremely small when compared to total number of clock transitions. In addition, the amount of time the output is actually in the metastable region is a variable and dependent on the type of flip-flop used (LS, ALS, AS, etc.).

From the design engineers viewpoint, when using a flip-flop as a data synchronizer, they can no longer use the specified data sheet maximum for propagation delay. Instead, to guarantee reliable system operation, they need to know how long after the specified data sheet maximum they need to wait before using the data. Conventional test equipment is not designed to measure these parameters, so a special test circuit is required for characterizing MTBF (Mean Time Between Failures) and Δt (time between CLK and Q valid). With these two parameters specified, the system designer can make a rational decision about what type of flip-flop to use, and how long to wait before using the data.

Circuit Description

The circuit in Figure 2 can be used in evaluating MTBF and Δt for a selected flip-flop (DUT, Device Under Test). Two 'AS04s are used to detect whenever the Q output of the DUT is in the metastable region. This is accomplished by adjusting the input threshold to 2 V on one inverter and 0.8 V on the other. Notice that input thresholds are adjusted by referencing the ground input pins to 0.6 V and −0.6 V respectively. Therefore, whenever the Q output of the DUT

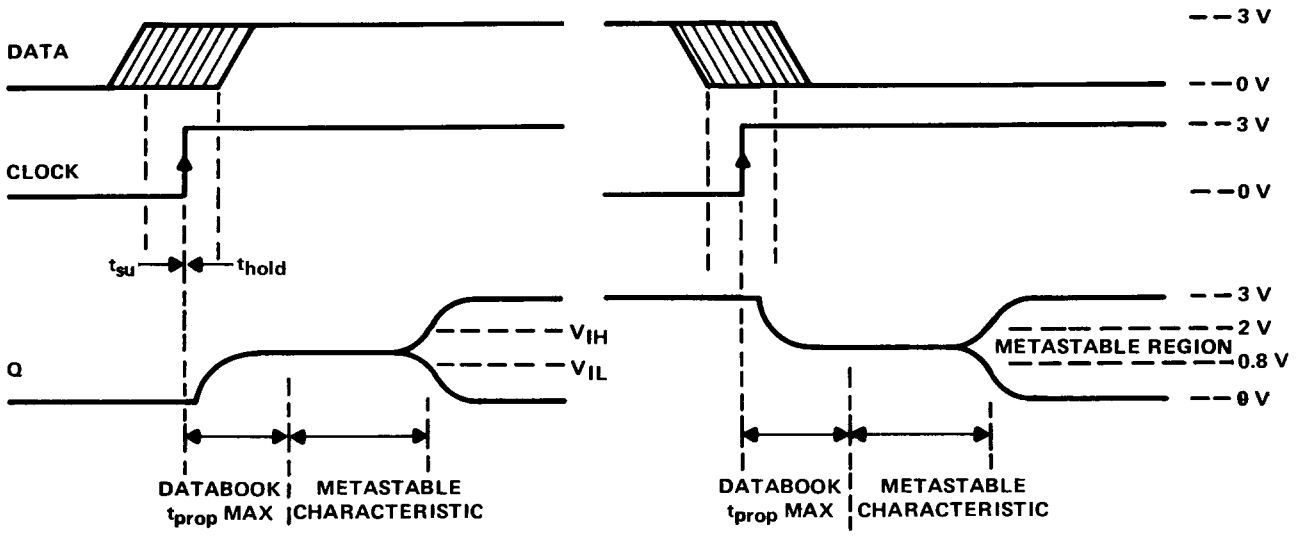

Figure 1. Metastable Timing Diagram

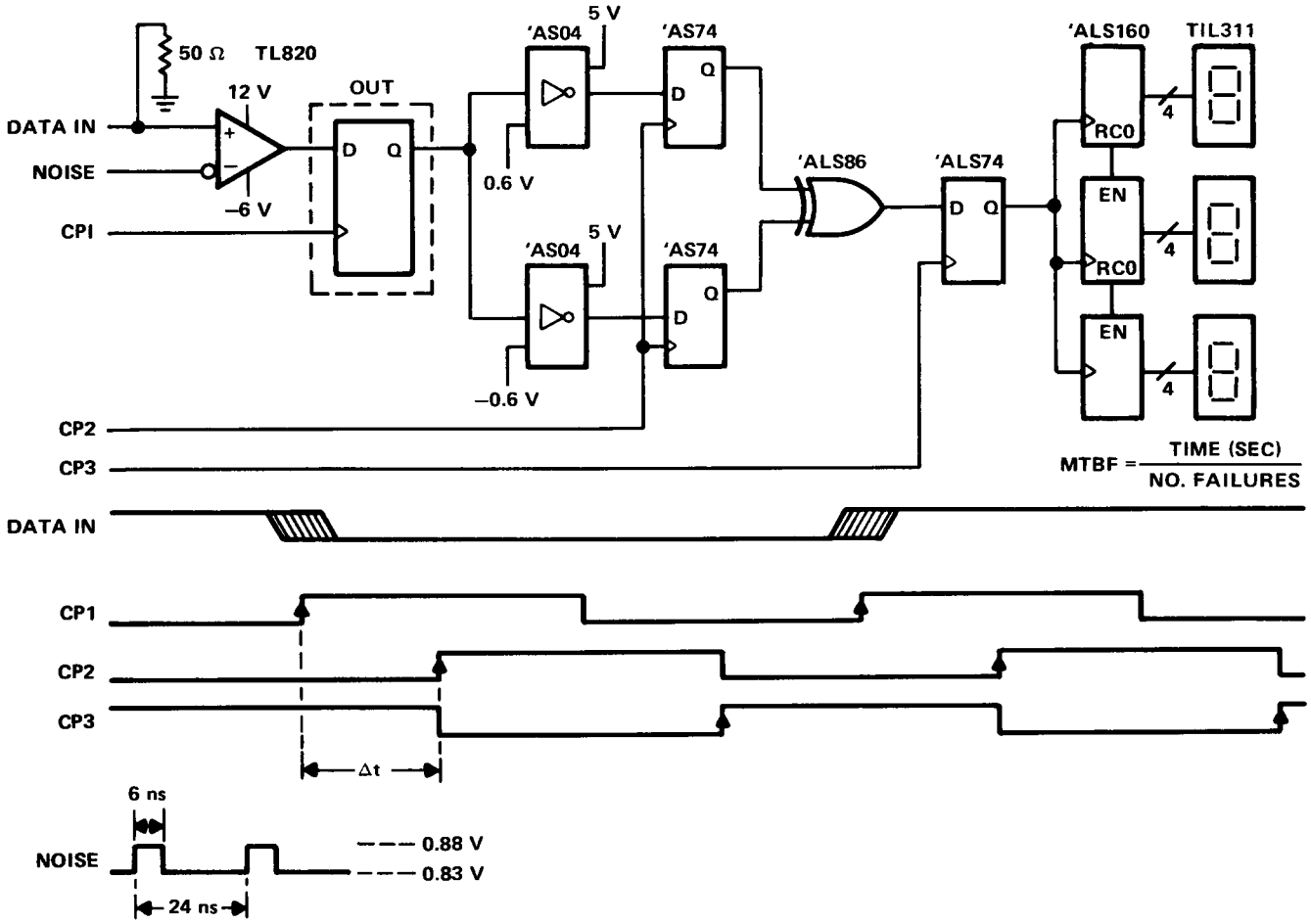

Figure 2. Metastable Evaluation Test Circuit

is between 0.8 V and 2 V, the inverters will be in opposite states. Whenever the Q output of the DUT is higher than 2 V or lower than 0.8 V, both inverters will be at the same logic level. The outputs of the 'AS04s are then clocked (CP2) into two 'AS74s a selected time (Δt) after the DUT clock (CP1). The outputs of the 'AS74s are compared through an 'ALS86 and clocked (CP3) into another 'ALS74. This guarantees against any false clocking by the evaluation circuit. The output of the 'ALS74 is then feed to a series of three 'ALS160 counters, and on into three TIL311s for counter display.

In order to maximize the possibility of forcing the DUT into a metastable state, the input data signal must jitter around the threshold of the input clock. The width of the jitter should equal, or exceed the setup and hold time specification for the device. In our evaluation circuit, this is accomplished by feeding a low level noise signal into the negative input of a TIL820 operational amplifier. The pictures shown in Figure 3 show the noise generated around the DUT clock (CP1) for both input data transitions.

It should be intuitively obvious that the worst-case condition, for any specified input data frequency, will be when the input data **always violates the data setup and hold times**. This condition is shown in the timing diagram of Figure 2. Any other relationship of CP1 to DATA IN, would provide less chance for the device to enter the metastable state. Therefore, it can be concluded that the worst-case condition for a given input data frequency, will be 0.5 times the DUT clock rate where the input data always violates the setup and hold time.

By using the described circuit, MTBF can be determined for several different values of Δt. Plotting this information on semilog paper reveals the metastable characteristics, for the selected flip-flop, at the desired input data frequency.

Test Circuit Limitations

Before we proceed to the AS/ALS test results, it is important to analyze the limitations of our test circuit. In this way, we can better understand its effects on the test results. Two major areas which can greatly affect the test results are not centering the jitter around the input clock, and propagation delay of the 'AS04s. By not centering the jitter around the input clock, the risk of entering the metastable state is reduced. Proper care must be taken to ensure that the jitter is always centered around the input clock to guarantee worst-case conditions.

The propagation delay of the 'AS04s affect the test results because they add propagation delay between the output of the DUT, and the data being clocked into the 'AS74s. For

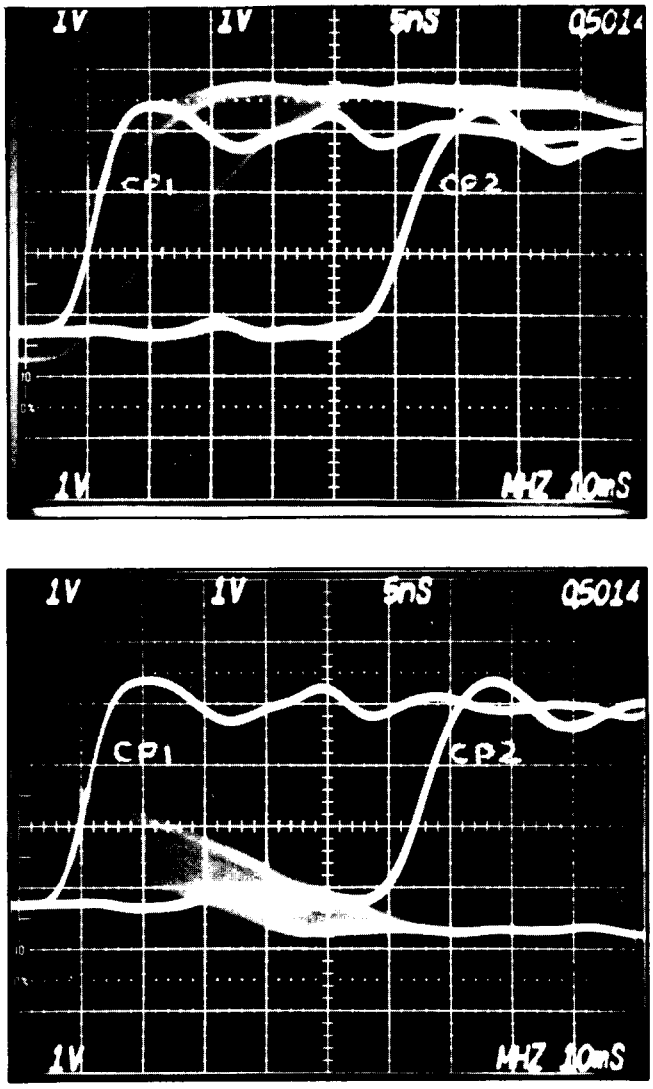

Figure 3. Test Waveforms

example, the output on the DUT may come out of the metastable region, but the 'AS04s may not switch before CP2 occurs. This causes an inappropriate reading. The typical propagation delay of the 'AS04s, **as configured in the test circuit**, is approximately 4 ns. This 4 ns delay should be considered when evaluating the test results. If inverters slower than the 'AS04s are used in the test circuit, a larger offset must be considered.

ALS/AS Test Results

Using the test circuit described in Figure 2, 'ALS74s, 'ALS273s and 'ALS374s were evaluated at several different Δt time periods. The input clock frequency used was 1 MHZ with an input data frequency of 500 kHz. The devices were allowed to run until an appropriate amount of errors were recorded. The number of errors were then divided by the total time the devices were allowed to run. This results in a MTBF for the selected Δt. The information was then recorded on semilog paper for analysis. It was found that all three device types exibited basically the same metastable characteristics within +3 ns of each other. This was expected since all three device types come from the same technology. The same experiment was performed using AS and LS devices. The average characteristics for all three device families are shown in Figure 4. The 4-ns offset generated by the test circuit has not been subtracted from the data.

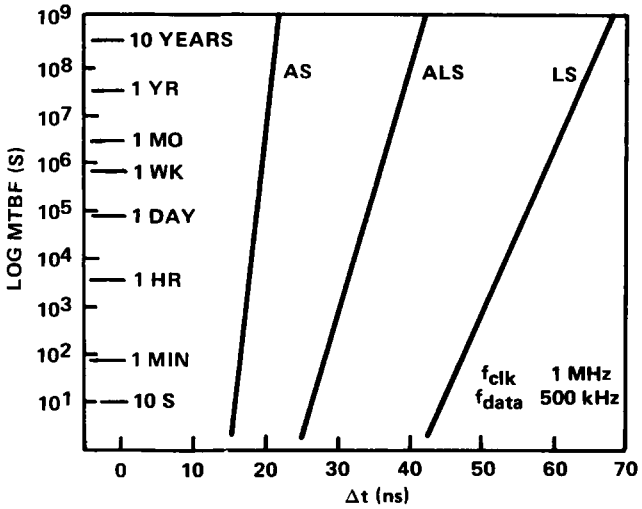

Figure 4. AS/ALS/LS Metastable Characteristics

Other Clock Frequencies

Clock frequencies other than 1 MHz will either increase or decrease the probability of the device entering the metastable state. The faster the frequency, the higher the probability of entering the metastable state. Likewise, the slower the frequency, the lower the probability of entering the metastable state. From the data taken in the above experiment, an equation can be derived for the metastable characteristics at other clock frequencies. Equation (1) relates input clock and data frequency, to metastable characteristics.

Metastable Equation

$$\frac{1}{\text{MTBF}} = f_{cp} \times f_{data} \times C1\, e^{(-C2\ \Delta t)} \qquad (1)$$

As stated earlier, the worst case situation for the test circuit shown in Figure 2, is when the data setup and hold time is always violated. Based on this assumption, the equation is reduced to the following.

$$\frac{1}{\text{MTBF}} = \frac{1}{2} f_{cp}^2 \times C1\, e^{(-C2\ \Delta t)} \qquad (2)$$

The constants C1 and C2 describe the metastable characteristics of the device. From the experimental data graphed in Figure 4, these constants can be solved for each device family. As an example, the constants are solved below for the ALS device family.

C2 is defined by the slope of the line. Picking two data points off the graph yields the following.

$$C2 = \frac{10^8 - 10^2}{40.2 - 28.2}(2.302) = \frac{6}{12}(2.302) = 1.151$$

By plugging C2 into equation 2, along with using one of the data points off the graph, C1 can be solved for.

$$\frac{1}{MTBF} = \frac{1}{2} f_{cp}^2 \times C1\, e^{(-1.51\ \Delta t)}$$

$$\frac{1}{10^8} = \frac{1}{2} (10^6)^2 \times C1\, e^{(-1.151 \times 40.2)}$$

$$C1 = 2.49$$

Inserting C1 and C2 into equation 2, yields the metastable equation for ALS.

$$\frac{1}{MTBF} = \frac{1}{2} f_{cp}^2 \times 2.49\, e^{(-1.151\ \Delta t)}$$

Given this worst-case equation, the system designer can determine the metastable characteristics for ALS when using other input clock frequencies.

The equations for AS and LS can be derived using the same procedure. They are as follows.

AS:

$$\frac{1}{MTBF} = \frac{1}{2} f_{cp}^2 \times 1.53 \times 10^7\, e^{(-2.92\ \Delta t)}$$

LS:

$$\frac{1}{MTBF} = \frac{1}{2} f_{cp}^2 \times 306\, e^{-0.783\ \Delta t)}$$

To get a feel for the effect of changing the input clock frequency, Figure 5 shows the change in the metastable characteristics from 1 MHz to 10 MHz.

METASTABLE CHARACTERISTICS OF PROGRAMMABLE LOGIC

The PAL16R4A and TIBPAL16R4-15 from the programmable logic family were also evaluated. They exhibited very similar characteristics to the ALS curve. This was expected because they utilize the same technology. One important consideration when evaluating programmable logic in the test circuit described, is positioning the jittery data a few nanoseconds before CP1. This compensates for the delay of the AND/OR array which is usually positioned in front of the flip-flop. Remember that the jittery data must be violating the setup and hold time at the input to the flip-flop, not just at the device input. Some experimentation is usually required to find the worst-case condition.

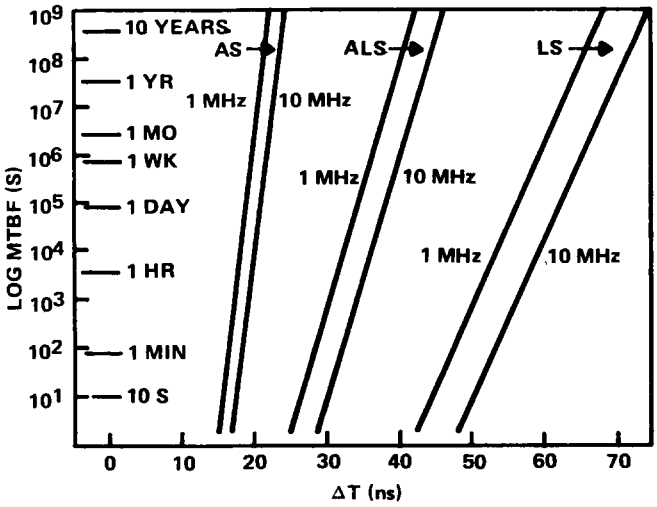

Figure 5. AS/ALS/LS Metastable Characteristics Variation with Frequency

As a general rule, a system designer can usually get a feel for the metastable characteristics of a device by simply looking at the setup and hold time specifications. Usually, the smaller the setup and hold time numbers, the better its metastable characteristics will be. However, in the case of programmable logic, the setup and hold time numbers are not reflective of metastable characteristics. This is because the setup and hold time numbers also reflect the propagation delay time of the AND/OR logic in front of the flip-flops.

SUMMARY

The metastable characteristics of a flip-flop used for data synchronization can greatly affect system reliability. Based on the information presented in this application report, the system designer can make a rational decision about what type of flip-flop to use, and what its metastable characteristics will be.

It is easy to see from the experimental data shown in Figure 4, that AS offers the best metastable characteristics. It has a much narrower setup and hold time window, and is quicker to recover once it gets into the metastable region. However, with adequate sampling time, ALS and LS will also perform well. The selection of what type of flip-flop to use must be based on the speed of the application. As a general rule, the faster the flip-flop, the better its metastable characteristics.

We at Texas Instruments believe that the graphs shown and equations derived, represent a reasonable assumption about the metastable characteristics for the device families discussed. However, we strongly recommend that when using flip-flops as data synchronizers, an adequate amount of guardband is allowed between the characteristics shown, and when the output of the flip-flop is actually sampled.