

Product Brief SCARABAEUS SDA 9400

Scanrate Converter Using
Embedded Dram Technology Units

Potential Application

The SDA9400 is a new component of the Siemens MEGAVISION® IC set for building high end TV sets

- 100/120 Hz interlaced TV sets
- 50/60 Hz Progressive Scan TV sets

Features

■ Two Input Data Formats

- 4:2:2 luminance and chrominance parallel (2 x 8 wires)
- ITU-R 656 data format (8 wires)

■ Flexible Compression of the Input Signal

- Digital vertical compression of the input signal (1.0, 1.25, 1.5, 1.75, 2.0, 3.0, 4.0)
- Digital horizontal compression of the input signal (1.0, 2.0, 4.0)

■ Noise Reduction

- Motion adaptive spatial and temporal noise reduction (3D-NR)
- Flexible programming of the temporal noise reduction parameters
- Automatic measurement of the noise level (5 bit value, readable by I²C Bus)

■ 3-D Motion Detection

- High performance motion detector for scan rate conversion
- Global motion detection flag (readable by I²C Bus)
- Movie mode and phase detector (readable by I²C Bus)

■ Embedded Memory 5 Mbit Embedded DRAM Core for Field Memories, 192 kbit Embedded DRAM Core for Line Memories

■ Flexible Clock and Synchronization Concept

■ Scan Rate Conversion

- Motion adaptive 100/120 Hz interlaced scan conversion
- Motion adaptive 50/60 Hz progressive scan conversion
- Simple static interlaced and progressive conversion modes for 100/120 Hz interlaced or 50/60 Hz progressive scan conversion: e.g. ABAB, AABB, AA*B*B,

AAAA, BBBB, AB, AA*

- Large area and line flicker reduction

■ Flexible Digital Vertical Expansion of the Output Signal (1.0, ... [1/32]..., 2.0)

■ Flexible Output Sync Controller

■ Signal Manipulations

- Insertion of coloured background
- Vertical and/or horizontal windowing with four different speed factors
- Flash generation (for supervising applications, motion flag readable by I²C Bus)
- Still frame or field
- Support for split screen applications (PIP processor necessary)
- Still-in-moving picture, Moving-in-still picture (PIP processor)

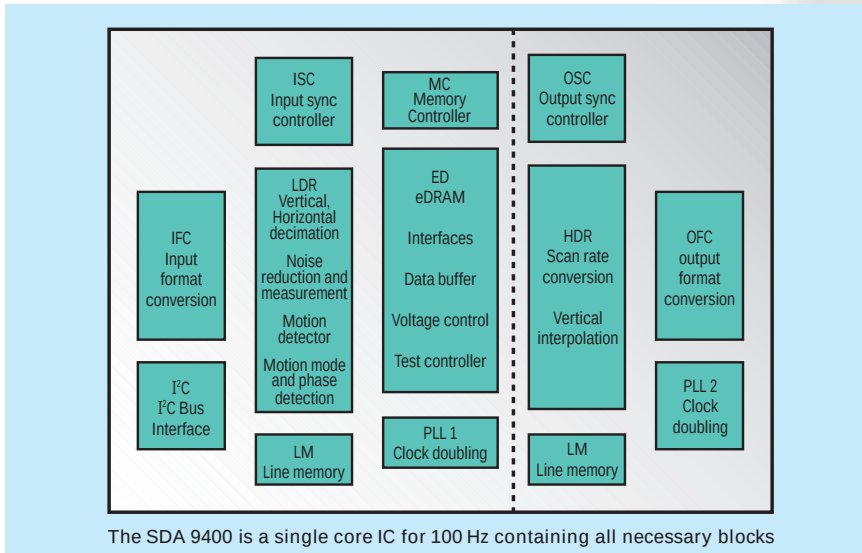


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Technical Data

- I²C Bus control (400 kHz)
- P-MQFP-64 package
- 3.3 V $\pm$ 5% supply voltage
- 0.35 μ m CMOS technology
- 4:2:2 processing
- Embedded memory
 - 5 Mbit embedded DRAM core for field memories
 - 192 kbit embedded DRAM core for line memories

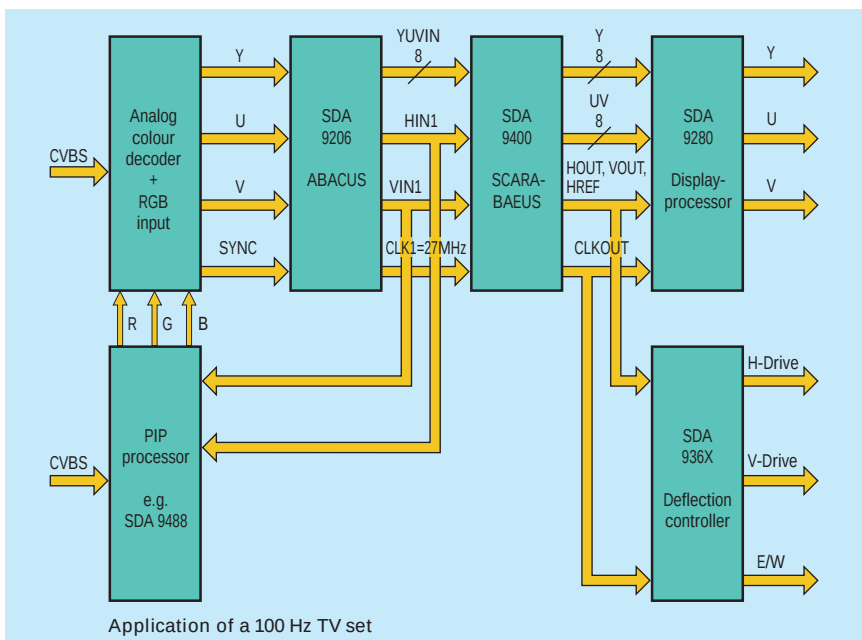
Block Diagram SDA 9400



The SDA 9400 contains all necessary functional blocks on a single chip:

- Flexible input sync controller
 - Input format conversion
 - Low data rate processing
 - Memory controller
 - Flexible output sync controller
 - Output format conversion
 - High data rate processing
 - I²C Bus interface
 - PLL for frequency doubling
- and in a leading edge technology 5.2 Mbit embedded DRAM for line and field memories.

Application Example



Availability

The SDA 9400 and a complete documentation is available in samples 1998. Mass production is scheduled for 1999. A dedicated engineering support team is there to assist you. Also an application board is available. Please contact your local Siemens office for further

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