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Introduction

SDA 9288X – The One-Chip Picture-In-Picture System

With SDA 9288X the semiconductor department for the first time presents a highly integrated one-chip solution for pictures insertion. The whole PIP circuitry consisting of analog-to-digital converter (ADC), picture memory, image processing, matrix and digital-to-analog converter (DAC) was packaged into a 32-pin P-DSO case. Compared to PIPplus the improved signal quality and various important features such as POP (picture outside picture) or multi-PIP extend the range of application considerably. Less space requirements on the PCB as well as reduced peripheral circuit complexity lower costs whereby the picture quality is increased at the same time.

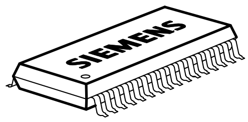
SIEMENS

Picture-In-Picture Processor
1-Chip

SDA 9288X

Preliminary Data

1 Features



P-DSO-32-2

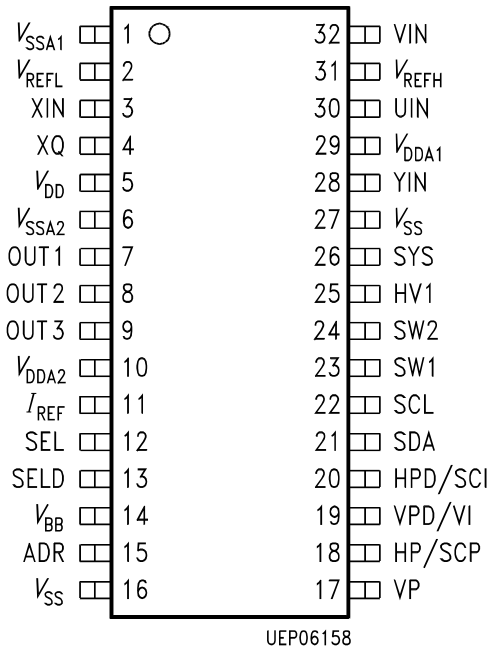
- **Multistandard Applications**
  625 lines / 50 Hz; 525 lines / 60 Hz standard
  (inset and parent channel)
  Scan conversion systems as flickerfree display systems (parent channel)
  HDTV (parent channel)
- **Single Chip Solution**
  Clamping, AD-conversion, filtering, field memory, RGB-matrix, DA-conversion and clock generation integrated on one chip
- **2 Picture Sizes**
  1/9 or 1/16 of normal size
- **High Resolution Display**
  13.5 MHz / 27 MHz display clock frequency
  212 luminance and 53 chrominance pixels per inset line for picture size 1/9
  6 Bit amplitude resolution for each incoming signal component
  Field and frame mode display
  Horizontal and vertical filtering
  Special antialias filtering for the luminance signal
- **16:9 Compatibility**
  Operation in 4:3 and 16:9 sets
  4:3 inset-signals on 16:9-displays or v.v. with picture size 1/9 and 1/16, respectively
- **Analog Inputs**
  Y, +(B-Y), +(R-Y) or Y, –(B-Y), –(R-Y)
- **Analog Outputs**
  Y, +(B-Y), +(R-Y) or Y, –(B-Y), –(R-Y) or RGB
  3 RGB-matrices: EBU, NTSC (Japan); NTSC (USA)

Type	Ordering Code	Package
SDA 9288X	Q67101-H5083	P-DSO-32-2 (SMD)

- **Free Programmable Position of Inset Picture**
  Steps of 1 pixel and 1 line
  All PIP and POP positions are possible
- **Programmable Framing**
  4096 frame colors
  Variable frame width
- **Freeze picture**
- **I^2C Bus Control**
- **Threefold PIP / POP Facility**
  Three different I^2C-addresses (pin-programmable)
  Tri-state outputs
- **Numerical PLL Circuit for High Stability Clock Generation**
- **No Necessity of PAL / SECAM Delay Lines**
  (using suitable color decoders i.e. TDA 8310)
- **P-DSO-32-2 Package / 350 mil (SMD)**
- **5 V Supply Voltage**

Pin Configuration
(top view)

P-DSO-32-2



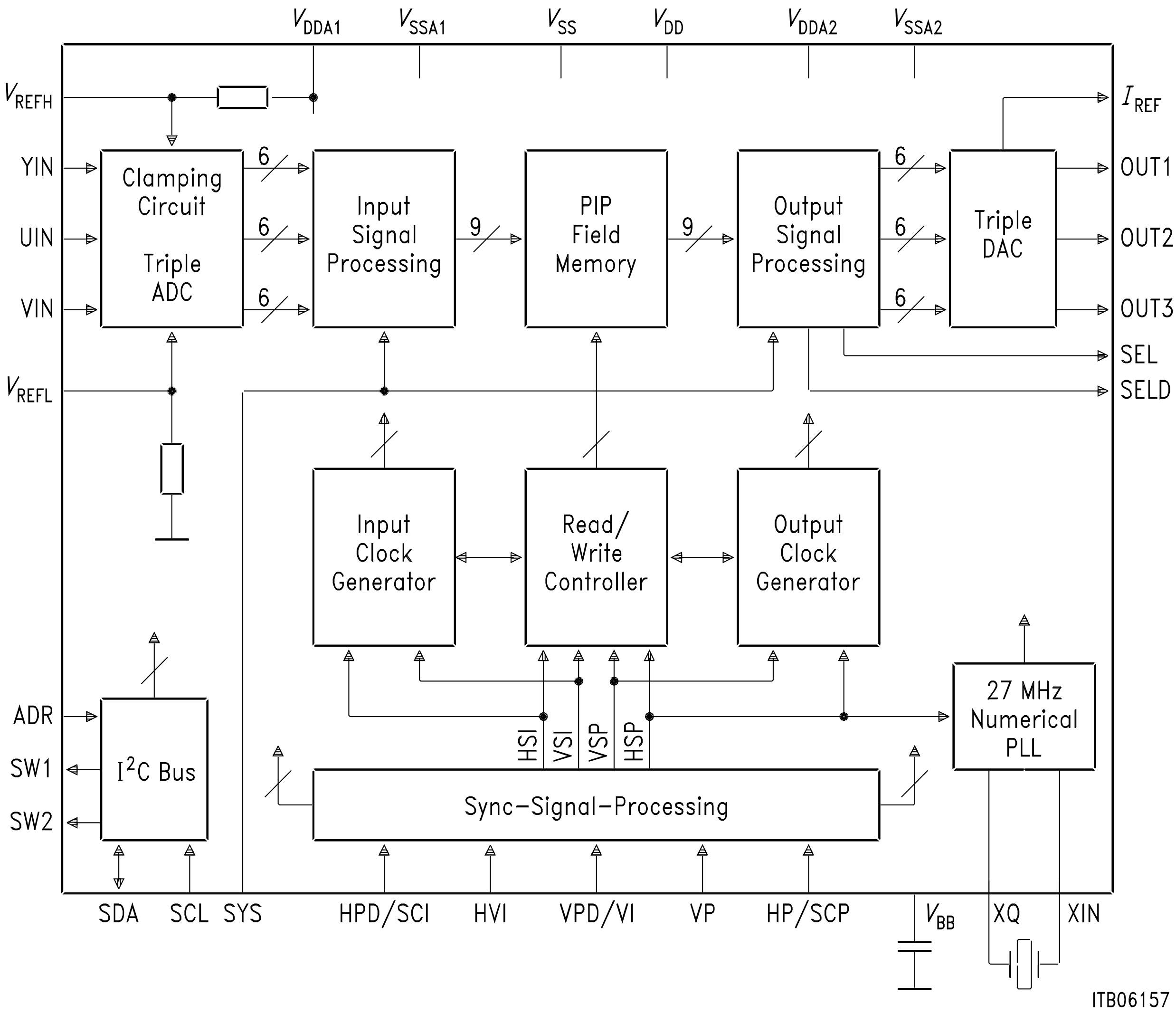
Pin Definitions and Function

Pin No.	Symbol	Function	Description
1	V_{SSA1}	S	Analog voltage supply (V_{SS}) for ADC
2	V_{REFL}	I	Lower reference voltage for AD-converters
3	XIN	I	Quartz oscillator (input) or quartz clock (from another PIP IC) or line locked clock (27 MHz, from a digital parent channel)
4	XQ	Q	Quartz oscillator (output)
5	V_{DD}	S	Digital voltage supply (V_{DD})
6	V_{SSA2}	S	Analog voltage supply (V_{SS}) for DAC and PLL
7	OUT1	Q A	Analog output: chrominance signal +(R-Y) or –(R-Y) or R
8	OUT2	Q A	Analog output: luminance signal Y or G
9	OUT3	Q A	Analog output: chrominance signal +(B-Y) or –(B-Y) or B
10	V_{DDA2}	S	Analog voltage supply (V_{DD}) for DAL and PLL
11	I_{REF}	Q A	Reference current for DA-converters
12	SEL	Q	Single frequency fast PIP switching output (Tristate)
13	SELD	Q	Double frequency fast PIP switching output (Tristate)
14	V_{BB}	S	Capacitor connection for smoothing internally generated substrate bias
15	ADR	I^3L	I^2C Bus address control
16, 27	V_{SS}	S	Digital voltage supply (V_{SS})
17	VP	I	Multifrequency vertical sync for parent channel
18	HP/SCP	I	Multifrequency horizontal sync for parent channel
19	VPD/VI	I	Double frequency vertical sync for parent channel or vertical sync input for inset channel

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Function	Description
20	HPD/SCI	I	Double frequency horizontal sync for parent channel or horizontal input for inset channel
21	SDA	I/Q	I^2C Bus data
22	SCL	I	I^2C Bus clock
23	SW1	Q^3L	I^2C Bus controlled output 1
24	SW2	Q^3L	I^2C Bus controlled output 2
25	HVI	I^3L	Special 3 level horizontal and vertical sync signal for inset channel
26	SYS	I^3L	Input for standard depending internal switching (Low (L) = PAL, Mid (M) = NTSC, High (H) = SECAM)
28	YIN	I A	Analog input: luminance signal Y
29	V_{DDA1}	S	Analog voltage supply (V_{DD}) for ADC
30	UIN	I A	Analog input: chrominance signal +(B-Y) or –(B-Y)
31	V_{REFH}	I	Upper reference voltage for AD-converters
32	VIN	I A	Analog input: chrominance signal +(R-Y) or –(R-Y)

I = Input
A = Analog
^3L = 3 level
Q = Output
TTL = Digital (TTL)
S = Supply voltage



Block Diagram

2 System Description

2.1 AD-Conversion, Inset Synchronization

The inset video signal is fed to the SDA 9288X as analog luminance and chrominance components. The polarity of the chrominance signals is programmable. After clamping the video components are AD-converted with an amplitude resolution of 6 bit. The conversion is done using a 13.5 MHz clock for the luminance signal and a 3.375 MHz clock for the chrominance signals.

For inset synchronization it is possible to feed either a special 3 level signal via pin HVI (detection of horizontal and vertical pulses) or separate signals via pins SCI for horizontal and Vl for vertical synchronization. SCI is the horizontal synchron signal of the inset channel. lf the burst gate pulse of the sandcastle is used it must be adapted to TTL compatible levels by a simple external circuit. Centering of the displayed picture area is possible by a programmable delay for the horizontal synchronization signal (HSIDEL).

The inset horizontal synchronization signals are sampled with 27 MHz. This 27 MHz clock and the AD-converter clocks are derived from the parent horizontal synchronization pulse (see PLL description) or from the quartz frequency converted by a factor of 4/3.

Delay differences between luminance and chrominance signals at the input of the IC caused by chroma decoding are compensated by a programmable luminance delay line (YDEL) of about – 290 ns … 740 ns (at decimation input; see application information).

By analyzing the synchronization pulses the line standard of the inset signal source is detected and interference noise on the vertical sync signal is removed. For applications with fixed line standard (only 625 lines or 525 lines) the automatic detection can be switched off.

The phase of the vertical sync pulse is programmable (VSIDEL; VSPDEL). By this way a correct detection of the field number is possible, an important condition for frame mode display. Remark: The adjustment of VSIDEL is influenced by HSIDEL (see waveform), vertical synchronization via pin HVI causes an additional internal delay for the vertical sync pulse of about 16 µs.

2.2 Input Signal Processing

This stage performs the decimation of the inset signal by horizontal and vertical filtering and subsampling. A special antialias filter improves the frequency response of the luminance channel. lt is optimized for the use of the horizontal decimation factor 3:1.

A window signal, derived from the sync pulses and the detected line standard, defines the part of the active video area used for decimation. For HSIDEL = 0 the decimation window is opened about 104 clock periods (13.5 MHz) after the horizontal synchronization pulse. For the 625 lines standard the 36^{th} video line is the first decimated line, for the 525 lines standard decimation starts in the 26^{th} video line.

The following decimation filters are implemented:

Horizontal Decimation	Component	Filter
3:1	luminance	$1 + z^{-1} + z^{-2}$
3:1	chrominance	$1 + 2 \times z^{-1} + z^{-2}$
4:1	luminance	$1 + z^{-1} + z^{-2} + z^{-3}$
4:1	chrominance	$1 + z^{-1} + z^{-2} + z^{-3}$

Vertical Decimation	Component	Filter
3:1	luminance	$1 + z^{-L} + z^{-2L}$
3:1	chrominance	$1 + 2 \times z^{-L} + z^{-2L}$
4:1	luminance	$1 + z^{-L} + z^{-2L} + z^{-3L}$
4:1	chrominance	$1 + z^{-L} + z^{-2L} + z^{-3L}$

$z = e^{j\omega T}$, T = 1/13.5 MHz for luminance
T = 1/3.375 MHz for chrominance

L = samples per line for luminance respectively chrominance

The realized chrominance filtering allows omitting the color decoder delay line for PAL and SECAM demodulation if the color decoder supplies the same output voltages independent of the kind of operation. In case of SECAM signals an amplification of the chrominance signals by a factor of 2 is necessary because just every second line a signal is present. This chrominance amplification is programmable via pin SYS or I^2C Bus (AMSEC).

The horizontal and vertical decimation factors are free programmable (DECHOR, DECVER). Using different decimations horizontal and vertical 16:9 applications become realizable:

DECHOR = 1, DECVER = 0: picture size 1/9 for 4:3 inset signals on 16:9 displays.

DECHOR = 0, DECVER = 1: picture size 1/16 for 16:9 inset signals on 4:3 displays.

2.3 PIP Field Memory

The onchip memory stores one decimated field of the inset picture. Its capacity is 169812 bits. The picture size depends on the horizontal and vertical decimation factors.

Horizontal Decimation	PIP Pixels per Line		
	Y	(B-Y)	(R-Y)
3:1	212	53	53
4:1	160	40	40

Vertical Decimation	Line Standard	PIP Lines
3:1	625	88
3:1	525	76
4:1	625	66
4:1	525	57

In field mode display just every second inset field is written into the memory, in frame mode display the memory is continuously written. Data are written with the lower inset clock frequency depending on the horizontal decimation factor (4.5 MHz or 3.375 MHz). Normally the read frequency is 13.5 MHz and 27 MHz for scan conversion systems. For progressive scan conversion systems and HDTV displays a mode is available (LINEDBL). Every line of the inset picture is read twice.

Memory writing can be stopped by program (FREEZE), a freeze picture display results (one field).

Having no scan conversion and the same line numbers in inset and parent channel (625 lines or 525 lines both) frame mode display is possible. The result is a higher vertical and time resolution because of displaying every incoming field. For this purpose the standards are internally analyzed and activating of frame mode display is blocked automatically when the described restrictions are not fulfilled.

As in the inset channel a field number detection is carried out for the parent channel. Depending on the phase between inset and parent signals a correction of the display raster for the read out data is performed by omitting or inserting lines when the read address counter outruns the write address counter.

The display position of the inset picture is free programmable (POSHOR, POSVER). The first possible picture position (without frame) is 54 clock periods (13.5 MHz or 27 MHz) after the horizontal and 4 lines after the vertical synchronization pulses. Starting at this position the picture can be moved over the whole display area. Even POP-positions (Picture Outside Picture) at 16:9 applications are possible.

Having different line standards in inset and parent channels we have a so called mixed mode display. It causes deformations in the aspect ratio of the inset picture. A special mixed mode display is available for the picture size 1/9 (MIXDIS):

– parent channel 625 lines, inset channel 525 lines: The inset picture is shifted down by 6 lines. By performing this shifting the centers of the inset pictures have the same position for both line standards.
– parent channel 525 lines, inset channel 625 lines: The inset picture gets a reduced line number of 76. The first 6 and the last 6 lines are omitted. This way the inset picture size is the same as for 525 lines inset signals. The display shows the center part of the original picture.

Synchronization of memory reading with the parent channel is achieved by processing the parent horizontal and vertical synchronization signals in the same way as described for the inset channel. The synchronization signals are fed to the IC at pin HP/SCP for horizontal synchronization and pin VP for vertical synchronization. In the same way as described for the inset channel the burst gate of the sandcastle signal can be used for horizontal synchronization. In scan conversion systems also the inputs HPD/SCI and VPDNI are available if the input HVI is activated for inset synchronization.

2.4 Output Signal Processing

At the memory output the chrominance components are demultiplexed and linearly interpolated to the luminance sample rate.

Different output formats are available: luminance signal Y with inverted or non inverted chrominance signals (B-Y), (R-Y) or RGB. For the RGB-conversion 3 matrices are integrated:

Standard	**B-Y**	**R-Y**	**G-Y**	**B-Y**	**R-Y**	**G-Y**
EBU	1	0.588	0.345	0°	90°	237°
NTSC (Japan)	1	0.783	0.31	0°	95°	240°
NTSC (USA)	1	1.013	0.305	0°	104°	252°

Matrix selection is done by pin SYS or I^2C Bus. The matrices are designed for the following input voltages (100 % white, 75 % color saturation):

Component	Input Voltage (without sync) in % of Full Scale Input Range of ADC
Y	75
B-Y	100
R-Y	100

Matrix-Equations

EBU

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 \\ 0 & 0.78125 & 1 \\ -0.1875 & -0.40625 & 1 \end{bmatrix} \begin{bmatrix} B-Y \\ R-Y \\ Y \end{bmatrix}$$

NTSC (Japan)

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 \\ -0.0625 & 1.09375 & 1 \\ -0.15625 & -0.375 & 1 \end{bmatrix} \begin{bmatrix} B-Y \\ R-Y \\ Y \end{bmatrix}$$

NTSC (USA1)

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 \\ -0.25 & 1.375 & 1 \\ -0.09375 & -0.40625 & 1 \end{bmatrix} \begin{bmatrix} B-Y \\ R-Y \\ Y \end{bmatrix}$$

A colored frame is added to the inset picture. 4096 frame colors are programmable, 4 bits for each component Y, (B-Y), (R-Y). The horizontal and vertical width of the frame are independently programmable. Width = 0 means display without frame.

For controlling an external switch (for example a RGB processor) a select signal is supplied. Pin SEL is active in normal 13.5 MHz reading mode, pin SELD is active using 27 MHz. The phases of these signals are programmable for adaption to different external output signal processing.

2.5 DA-Conversion

The SDA 9288X includes three 6 bit DA-converters. Each converter supplies a current through an external resistor that is connected between VSSA and OUT1, OUT2, OUT3 respectively. The current is controlled by a digital control circuit. Each command DACONST or PIPON starts the adjustment cycle.

2.6 PLL

A numerical PLL circuit supplies a clock of about 27 MHz with high stability. The generated clock is locked to the parent horizontal synchronization pulse. Its frequency depends linearly on the frequency of the sync signal and the quartz frequency. The recommended quartz frequencies are listed under “Recommended Operation Conditions”. Using up to three SDA 9288X ICs in one application only a single quartz is necessary. Four time constants are programmable via I^2C Bus. lf the PLL is switched off an external 27 MHz parent line locked clock can be fed to the IC.

The inset clock generation is possible in two ways:

1. Synchron with the parent horizontal synchronization pulse (Bit CLISW = 0)
2. Synchron with the quartz frequency (Bit CLISW = 1; $f_{cli} = 4/3 \times f_{quartz}$). In this mode the aspect ratio is independent on the parent sync frequency but depends on the used resonator type. lt is only possible to use one of the two modes.

Note: Before setting bit D3 of Subaddress 00 (READ27) noise reduction of the VSP pulse must be switched off (D5 of subaddress 08 = 1).

2.7 I²C Bus

2.7.1 I²C-Bus Addresses

Three different I²C addresses are programmable via pin ADR.

Pin ADR	Address (bin.)	Address (hex.)
Low level (V_{SS} or V_{SSA})	11010110	D6
Mid level (open)	11011100	DC
High level (V_{DD} or V_{DDA})	11011110	DE

2.7.2 I²C-Bus Receiver Format

S	Address	A	Subaddress	A	Data byte	A	****	A	P

S: Start condition A: Acknowledge P: Stop condition

Only write operation is possible. An automatically address increment function is implemented.

2.7.3 I²C-Bus Commands

Sub-Addr	Data Bytes							
Hex.	D7	D6	D5	D4	D3	D2	D1	D0
00	0	SYSACT	FREEZE	PLLOFF	READ27	LINEDBL	FRAME	PIPON
01	0	SELDEL3	SELDEL2	SELDEL1	SELDEL0	MIXDIS	POSHOR9	POSHOR8
02	POSHOR7	POSHOR6	POSHOR5	POSHOR4	POSHOR3	POSHOR2	POSHOR1	POSHOR0
03	POSVER7	POSVER6	POSVER5	POSVER4	POSVER3	POSVER2	POSVER1	POSVER0
04	0	SW21	SW20	SW11	SW10	YDEL2	YDEL1	YDEL0
05	DECVER	DECHOR	INSVHI	CHRINS	PMOD1	PMOD0	IMOD1	IMOD0
06	0	0	0	CLISW	HSIDEL3	HSIDEL2	HSIDEL1	HSIDEL0
07	AMSEC	0	VSIISQ	VSIDEL4	VSIDEL3	VSIDEL2	VSIDEL1	VSIDEL0
08	PARSYND	0	VSPISQ	VSPDEL4	VSPDEL3	VSPDEL2	VSPDEL1	VSPDEL0
09	CON3	CON2	CON1	CON0	FRY5	FRY4	FRY3	FRY2
0A	FRV5	FRV4	FRV3	FRV2	FRU5	FRU4	FRU3	FRU2
0B	0	0	SELDOWN	FRWIDV1	FRWIDV0	FRWIDH2	FRWIDH1	FRWIDH0
0C	0	0	0	MAT2	MAT1	MAT0	CHRPIP	OUTFOR
0D	DACONST	PLLTC1	PLLTC2	0	0	0	0	DACONDE

After switching on the IC the data bytes of all registers are set to “0”, the bit PLLOFF is set to “1”.

Bit	Name	Function
Subaddress 00		
D0	PIPON	0: PIP insertion off 1: PIP insertion on
D1	FRAME	0: field display 1: frame display (under special restrictions)
D2	LINEDBL	0: each line of the PIP memory is read once (normal operation) 1: each line of the PIP memory is read twice (line doubling for progressive scan conversion systems in parent channel)
D3	READ27	0: PIP display with single read frequency (13.5 MHz) 1: PIP display with double read frequency (27 MHz) (**see note page 18**)
D4	PLLOFF	0: internal PLL on 1: internal PLL off (external clock generation)
D5	FREEZE	0: live picture 1: freeze picture
D6	SYSACT	0: pin SYS inactive: selection of decimation amplification and RGB-matrix is done via I^2C Bus 1: pin SYS active: selection of decimation amplification and RGB-matrix is done via pin SYS
Subaddress 01		
D1 … D0	POSHOR	2 MSBs of POSHOR (see also subaddress 02).
D2	MIXDIS	0: PIP picture height depends just upon inset line standard, position upon POSHOR 1: modified PIP picture height and position for different inset and parent line standards (mixed display mode)
D6 … D3	SELDEL	Delay of output signal SELECT at pins SEL respectively SELD (– 8 … + 7 periods of read frequency clock, programmable in 2’s complement code). SELDEL = 0: SELECT signal has the same phase as the PIP picture signal referenced to the IC output.

Bit	Name	Function
Subaddress 02		
D7 … D0	POSHOR	Horizontal position of PIP picture (raster: 1 pixel). **Remark:** the 2 MSBs of POSHOR are located at subaddress 01. **Warning: It is not allowed to adjust positions < 2 and > 740!**
Subaddress 03		
D7 … D0	POSVER	Vertical position of PIP picture (raster: 1 line). **Warning: It is not allowed to adjust positions > 220 (50 Hz) or > 182 (60 Hz)!**
Subaddress 04		
D2 … D0	YDEL	Delay of luminance input signal: 000: minimum delay 111: maximum delay; see application informations
D4 … D3	SW1	Direct control of output pin SW1 (3 levels): 00: low level 01: mid level 10: high level 11: high level
D6 … D5	SW2	Direct control of output pin SW2 (3 levels): 00: low level 01: mid level 10: high level 11: high level

Bit	Name	Function
Subaddress 05		
D1 … D0	IMOD	00: automatic detection of line standard (inset signal) 01: fixed adjustment: 625 lines* 10: fixed adjustment: 525 lines* 11: freeze last automatically detected line standard
D3 … D2	PMOD	00: automatic detection of line standard (parent signal) 01: fixed adjustment: 625 lines* 10: fixed adjustment: 525 lines* 11: freeze last automatically detected line standard
D4	CHRINS	0: chrominance input signals +(B-Y), +(R-Y) 1: inverted chrominance input signals –(B-Y), –(R-Y)
D5	INSHVI	0: inset synchronization signals via pins HPD/SCI and VPD/VI 1: inset synchronization signals via pin HVI (3-l. sand-castle signal)
D6	DECHOR	0: horizontal decimation 3 to 1 1: horizontal decimation 4 to 1
D7	DECVER	0: vertical decimation 3 to 1 1: vertical decimation 4 to 1

* Fixed adjustments for IMOD and PMOD result in undefined working conditions when signal standards are used which are different from the programmed values.

Bit	Name	Function
Subaddress 06		
D3 … D0	HSIDEL	Delay of horizontal synchronization pulse (inset signal). Raster: 6 clock periods (13.5 MHz). **Warning: Adjustment of HSIDEL will influence the adjustment of VSIDEL (subaddr. 07); see waveforms!**
D4	CLISW	0: inset clock synchronized with parent clock 1: inset clock synchronized with quartz frequency **Note: Only one of the two modes can be used. Switching back from 1 to 0 is not possible!**

Bit	Name	Function
Subaddress 07		
D4 … D0	VSIDEL	Delay of vertical synchronization pulse (inset signal) in steps of 2.37 µs. **Warning: Correct adjustment value is influenced by the adjustment of HSIDEL (subaddr. 06); see waveforms!**
D5	VSIISQ	Noise reduction of the VSI pulse (set to “0” under normal conditions).
D7	AMSEC	0: unity amplification of decimation filters (normal mode) 1: amplification by a factor of 2 (SECAM signals without delay line in the chroma decoder)
Subaddress 08		
D4 … D0	VSPDEL	Delay of vertical synchronization pulse (parent signal) in steps of 2.37 µs / 1.68 µs (50/100 Hz).
D5	VSPISQ	Noise reduction of the VSP pulse (should be set to “0” under normal conditions).
D7	PARSYND	0: parent synchronization signals for double frequency read via pins HP/SCP and VP 1: parent synchronization signals for double frequency read via pins HPD/SCI and VPD/VI (INSHVI = 1 required)
Subaddress 09		
D3 … D0	FRY	Luminance component of frame color (4 MSBs of 6 bit).
D7 … D4	CON	contrast adjustment of PIP picture; steps and adjustment range depending on the external output resistors. Proposed value see at Characteristics.
Subaddress 0A		
D3 … D0	FRU	Chrominance component (B-Y) of frame color (4 MSBs of 6 bit).
D7 … D4	FRV	Chrominance component (R-Y) of frame color (4 MSBs of 6 bit).

Bit	Name	Function
Subaddress 0B		
D2 … D0	FRWIDH	Horizontal width of PIP frame (0 … 7 pixels).
D4 … D3	FRWIDV	Vertical width of PIP frame (0 … 3 lines).
D5	SELDOWN	0: open source output at pins SEL, SELD 1: TTL output at pins SEL, SELD
Subaddress 0C		
D0	OUTFOR	0: format of output signals: Y, (B-Y), (R-Y) 1: format of output signals: R G B
D1	CHRPIP	0: chrominance output signals: +(B-Y), +(R-Y) 1: inverted chrominance output signals: –(B-Y), –(R-Y)
D2	MAT0	0: EBU RGB-matrix 1: NTSC RGB-matrix
D3	MAT1	0: preselection of NTSC RGB-matrix (USA) 1: preselection of NTSC RGB-matrix (Japan)
D4	MAT2	0: matrix section by bit MAT0 1: automatic matrix selection depending on inset line standard
Subaddress 0D		
D0	DACONDE	Set to “0”.
D5 D6	PLLTC2 PLLTC1	Time constant of internal PLL: 00: medium damping, low resonance frequency 01: medium damping, high resonance frequency 10: high damping, low resonance frequency 11: high damping, high resonance frequency
D7	DACONST	Changing from 0 to 1 starts automatic adjustment of OUT1 … 3 output current if D0 = 0.

3 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remark
		min.	max.		
Ambient temperature		0	70	˚C	
Storage temperature		– 55	125	˚C	
Junction temperature			125	˚C	
Soldering temperature			260	˚C	duration < 10 s
Input voltage		– 0.5	V_{DD} + 0.5	V	analog inputs (YIN, UIN, VIN, IREF)
		– 1	7	V	all other pins
Output voltage		– 0.5	V_{DD} + 0.5	V	pins OUT1, OUT2, OUT3, XQ, SW1, SW2
		– 1	7	V	all other pins
Supply voltages		– 1	7	V	
Supply voltage differentials		– 0.25	0.25	V	
Total power dissipation			900	mW	
Latch-up protection		– 100	100	mA	except pins OUT1, OUT2, OUT3, IREF, XQ, YIN, UIN, VIN

All voltages listed are referenced to ground (0 V, V_{SS}) except where noted.

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions or at any other condition beyond those indicated in the operational sections of this specification is not implied.

4 Recommended Operating Conditions

Parameter	Symbol	Limit Values			Unit	Remark
		min.	typ.	max.		
Supply voltages	V_{DDxx}	4.75	5	5.5	V	
Ambient temperature	T_A	0	25	70	˚C	
All TTL Inputs						
Low-level input voltage	V_{IL}	– 1		0.8	V	
High-level input voltage	V_{IH}	2.0		6	V	
All Three Level Inputs (3-L) see Figure						
High-level input voltage	V_{IH}	3.5		6	V	
Low-level input voltage	V_{IL}	– 1		0.8	V	
Medium-level voltage	V_{IM}	open input, **see Characteristics**				
All 3-L Outputs see Figure						
High-level output current	I_{OH}	– 500		0	µA	
Low-level output current	I_{OL}	0		1.6	mA	
Inset Horizontal Sync TTL and 3-L Inputs: HPD/SCI, HVI (All values are referred to the corresponding min(V_{IH}), max(V_{IM}) and max(V_{IL}))						
Horizontal frequency		14.53		16.72	kHz	
Signal rise time				100	ns	noisefree L/M to H transition
Signal high time		100			ns	
Signal medium or low time		900			ns	

Recommended Operating Conditions (cont'd)

Parameter	Symbol	Limit Values			Unit	Remark
		min.	typ.	max.		
Inset Vertical Sync TTL and 3-L Inputs: VPD/VI, HVI (All values are referred to the corresponding min(V_{IH}), max(V_{IM}) and max(V_{IL}).						
Signal medium or high time		17			µs	necessary for vertical sync detection
Signal low time		200			ns	
Parent Horizontal Sync TTL Inputs: HP/SCP, HPD/SCI (All values are referred to the corresponding min(V_{IH}) and max(V_{IL}))						
Sync frequency in single frequency display mode		14.53		16.72	kHz	quartz frequency 20.480 MHz
		15		17.19	kHz	quartz frequency 21.090 MHz
Sync frequency in double frequency display mode		29.06		33.44	kHz	quartz frequency 20.480 MHz
		30		34.375		quartz frequency 21.090 MHz
Signal rise time				100	ns	noisefree transition
Signal high time		100			ns	
Signal low time		900			ns	

Recommended Operating Conditions (cont'd)

Parameter	Symbol	Limit Values			Unit	Remark
		min.	typ.	max.		
Parent Vertical Sync TTL Input VPD/VI (All values are referred to the corresponding min(V_{IH}) and max(V_{IL}))						
Signal high time		200			ns	
Signal low time		200			ns	
Quartz / Ceramic Resonator						
Recommended frequency		20.25	20.48	21.3	MHz	21.09 MHz for MUSE
Series resistance				10	Ω	C_1, $C_2 \leq$ 33 pF
				20	Ω	C_1, $C_2 \leq$ 22 pF
				30	Ω	C_1, $C_2 \leq$ 15 pF
				40	Ω	C_1, $C_2 \leq$ 10 pF
Optional TTL Clock Input: XIN (All values are referred to min(V_{IH}) and max(V_{IL}))						
Clock input cycle time		35		40	ns	external line locked 27 MHz clock (I^2C: internal PLL off)
Clock input rise time				5	ns	
Clock input fall time				5	ns	
Clock input low time		10			ns	
Clock input high time		10			ns	

Recommended Operating Conditions (cont'd)

Parameter	Symbol	Limit Values			Unit	Remark
		min.	typ.	max.		
Fast I²C Bus (All values are referred to min(V_{IH}) and max(V_{IL})) This specification of the bus lines need not to be identical with the I/O stages specification because of optional series resistors between bus lines and I/O pins.						
SCL clock frequency	f_{SCL}	0		400	kHz	
Inactive time before start of transmission	t_{BUF}	1.3			µs	
Set-up time start condition	$t_{SU;\ STA}$	0.6			µs	
Hold time start condition	$t_{HD;\ STA}$	0.6			µs	
SCL low time	t_{LOW}	1.3			µs	
SCL high time	t_{HIGH}	0.6			µs	
Set-up time DATA	$t_{SU;\ DAT}$	100			µs	
Hold time DATA	$t_{HD;\ DAT}$	0		0.9	µs	
SDA/SCL rise/fall times	t_R, t_F	20 + $		300	ns	$ = 0.1 C_b / pF
Set-up time stop condition	$t_{SU;\ STO}$	0.6			µs	
Capacitive load/bus line	C_b			400	pF	
I²C Bus Inputs/Output: SDA, SCL						
High-level input voltage	V_{IH}	3		V_{DD} + 0.5	V	also for SDA/ SCL input stages
Low-level input voltage	V_{IL}	– 0.5		1.5	V	
Spike duration at inputs		0	0	50	ns	
Low-level output current	I_{OL}			6	mA	

Recommended Operating Conditions (cont'd)

Parameter	Symbol	Limit Values			Unit	Remark
		min.	typ.	max.		
Analog To Digital Converters (6 bit)						
Input coupling capacitors		10	100		nF	necessary for proper clamping
Y, U, V source resistance				1	kΩ	
Reference voltage low	V_{REFL}	0.5	1.0	1.5	V	min and max values only with optional external resistors, see also Characteristics
Reference voltage high	V_{REFH}	1.5	2.0	2.5	V	
Reference voltage difference	$V_{REFH} - V_{REFL}$	0.5	1.0	2.0	V	
Digital To Analog Converters (6 bit)						
Full range output voltage	V_{OFR}		1	2	V	peak-to-peak
Reference resistance	R_{REF1}	4.2	5.1	6.3	kΩ	bits CON = 0000 no contrast adjustment used
	R_{REF2}	6.0	6.8	7.5	kΩ	contrast adjustment via I^2C Bus

5 Characteristics

(Assuming Recommended Operating Conditions)

Note: The listed characteristics are ensured over the operating range of the integrated circuit unless restricted to nominal operating conditions. (All voltages refer to V_{SS}).

Parameter	Symbol	Limit Values		Unit	Remark
		min.	max.		
Average total supply current	I_{DDtot}		160	mA	$I_{DDtot} = I_{DD} + I_{DDA1} + I_{DDA2}$ **Note:** The maxima do not necessarily coincide
Average digital supply current	I_{DD}		120	mA	
Average analog supply current	I_{DDA1}		40	mA	
Average analog supply current	I_{DDA2}		20	mA	
All Digital Inputs (TTL, I^2C)					
Input capacitance	C_I		7	pF	not tested
Input leakage current		– 10	10	µA	including leakage current of SDA output stage
All Three Level Inputs (3-L) see Figure					
Input capacitance	C_I		7	pF	not tested
Medium-level open input voltage	V_{IM}	2.1	2.5	V	$\|I_{IN}\| \leq 1$ µA, $V_{DD} = 5$ V
Differential input resistance	R_{IN}	8	14	kΩ	not tested

Characteristics (cont'd)

Parameter	Symbol	Limit Values		Unit	Remark
		min.	max.		
SEL, SELD					
High-level output voltage	V_{QH}	2.4	V_{DD}	V	I_{QH} = – 200 µA
High-level output voltage	V_{QH}	1.5	V_{DD}	V	I_{QH} = – 4.5 mA
Low-level output voltage	V_{QL}		0.4	V	I_{QL} = 1.6 mA, only valid if bit SELDOWN = 1
Leakage current		– 10		µA	V_Q = 0 V … V_{DD}
Output capacitance			7	pF	not tested
All 3-L Outputs					
High-level output voltage	V_{QH}		4 3.9	V V	I_{QH} = – 100 µA I_{QH} = – 500 µA
Low-level output voltage	V_{QL}		0.4	V	I_{QL} = max
Medium-level output leakage current	I_{QM}	– 1	1	µA	tristate
Output capacitance			7	pF	not tested
I²C Inputs: SDA/SCL					
Schmitt trigger hysteresis	V_{hys}	0.2		V	not tested
I²C Input / Output: SDA (referenced to SCL; open drain output)					
Low-level output voltage	V_{QL}		0.4	V	I_{QL} = 3 mA
Low-level output voltage	V_{QL}		0.6	V	I_{QL} = max
Output fall time from min(V_{IH}) to max(V_{IL})	t_{QF}	20 + 0.1 × C_b/pF	250	ns	10 pF ≤ C_b ≤ 400 pF

Characteristics (cont'd)

Parameter	Symbol	Limit Values		Unit	Remark
		min.	max.		
Analog To Digital Converters (6 bit)					
Y, U, V input leakage current		– 100	100	nA	
Y, U, V input capacitance			7	pF	not tested
Input clamping error		– 1	1	LSB	settled state
Input clamping current	$\|I_{CLP}\|$	50	150	µA	for large devitations
Reference voltage difference	$V_{REFH} - V_{REFL}$	0.98	1.02	V	V_{DDA} = 5 V, ($V_{REFH} - V_{REFL} \cong V_{DDA1}/5$)
D.C. differential nonlinearity		– 0.5	0.5	LSB	$V_{REFH} - V_{REFL}$ = nom
Digital To Analog Converters (6 bit): Current Source Outputs OUT1, OUT2, OUT3 I²C: Contrast bits set to zero unless otherwise noted					
D.C. differential nonlinearity	DNLE	– 0.5	0.5	LSB	R_{REF} = 5.1 kΩ
Full range output current	I_Q	tbf	tbf	mA	V_{DDA} = nom, T_A = nom, R_{REF} = 5.1 kΩ, R_L = 560 Ω, after adjustment
Output voltage ($U_Q \sim 1.6 \times V_{DDA} \times R_L/R_{REF}$)	U_Q	tbf	tbf	V	V_{DDA} = nom, T_A = nom, R_{REF} = 5.1 kΩ, R_L = 560 Ω after adjustment
Tracking		– 3	3	%	V_{DDA} = nom, T_A = nom, R_{REF} = 5.1 kΩ, R_L = 560 Ω

Characteristics (cont'd)

Parameter	Symbol	Limit Values		Unit	Remark
		min.	max.		
Contrast increase		30		%	V_{DDA} = nom, T_A = nom, R_{REF} = 6.8 kΩ, R_L = 560 Ω contrast bits change from 0000 to 1111 for typical values see diagram
Supply voltage dependence of DAC output current					for typical values see diagram
Temperature dependence of DAC output current					for typical values see diagram
Dependence of DAC output current on external reference resistor					for typical values see diagram

6 Diagrams

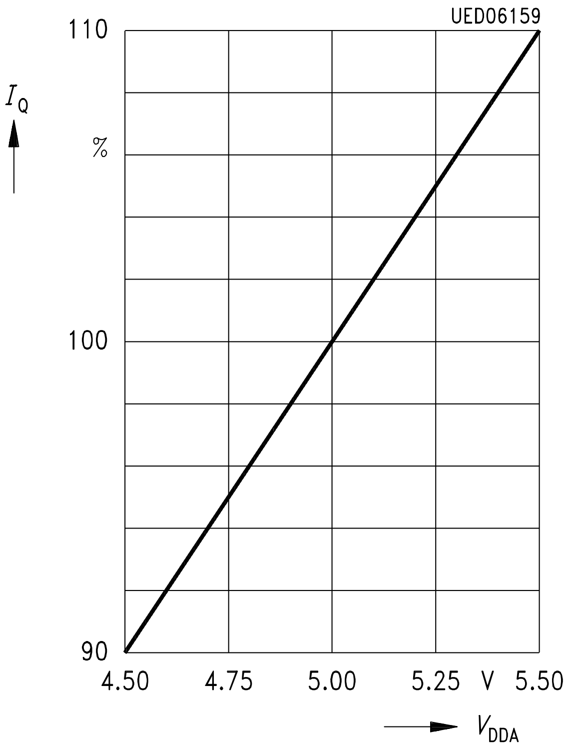
6.1 Output Current of DA Converters

Nominal values: V_{DDA} = 5 V; R_{REF} = 5.1 kΩ; T = 25 °C

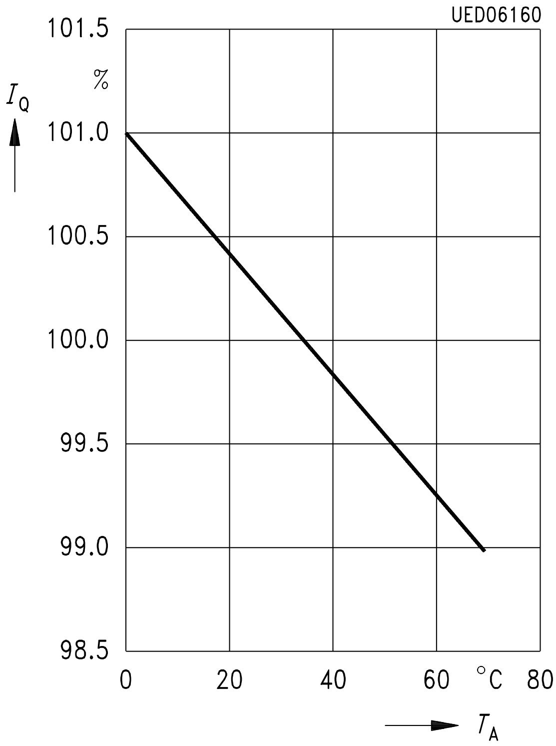
Measurements after adjustment via bit d7 of I²C Bus address 0D for each step.

Remark: The output currents are controlled in digital way, so inaccuracy of 1LSB (ca. 2 %) is always possible.

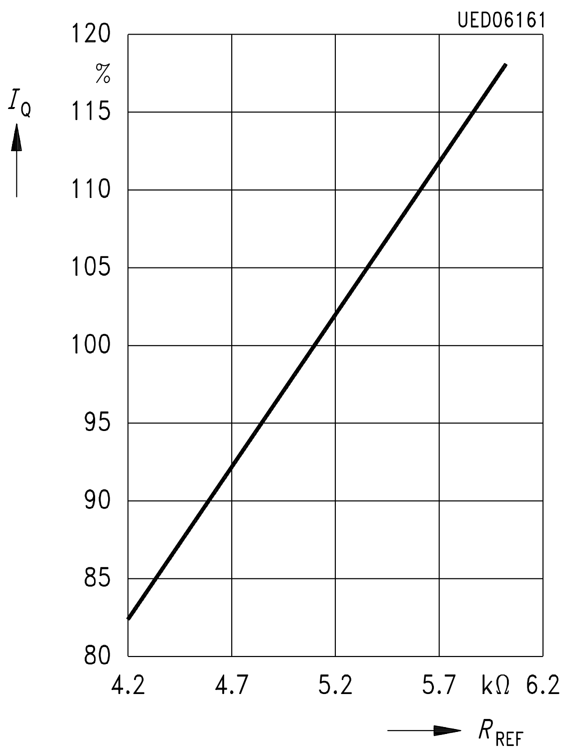
Output current = $f\,(V_{DDA})$



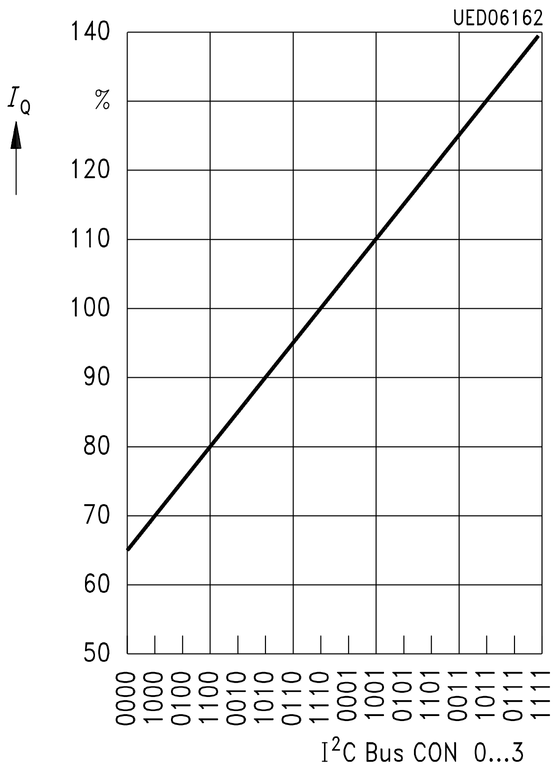
Output current = $f\,(T_A)$



Output current = $f\,(R_{REF})$

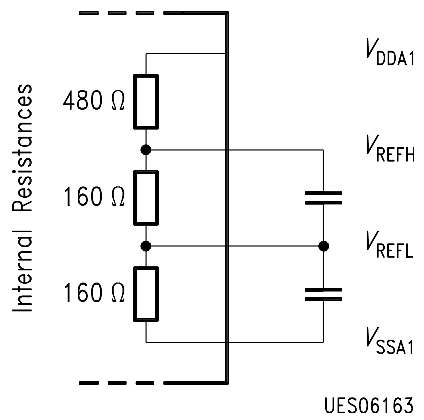


Current = f (CON 0 … 3), R_{REF} = 6.8 kΩ

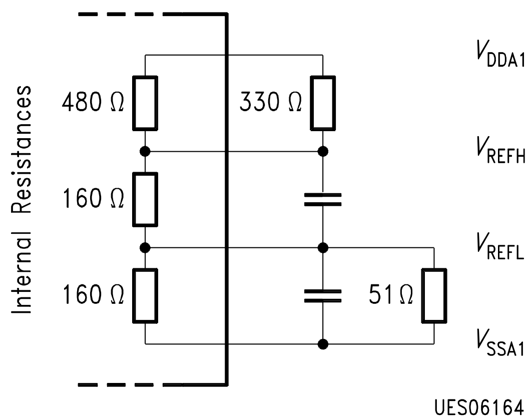


7 Application Information

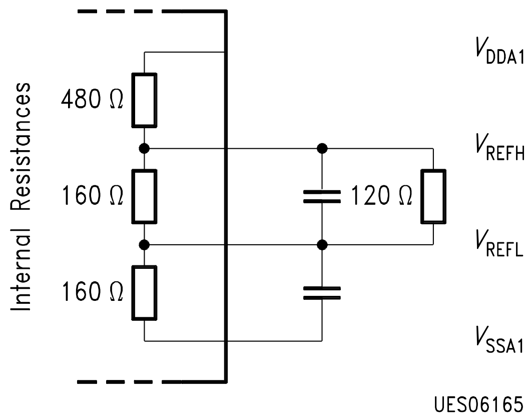
7.1 Reference Voltage Generation for ADC



Signal Input Range 1 Vpp at Y, U, V

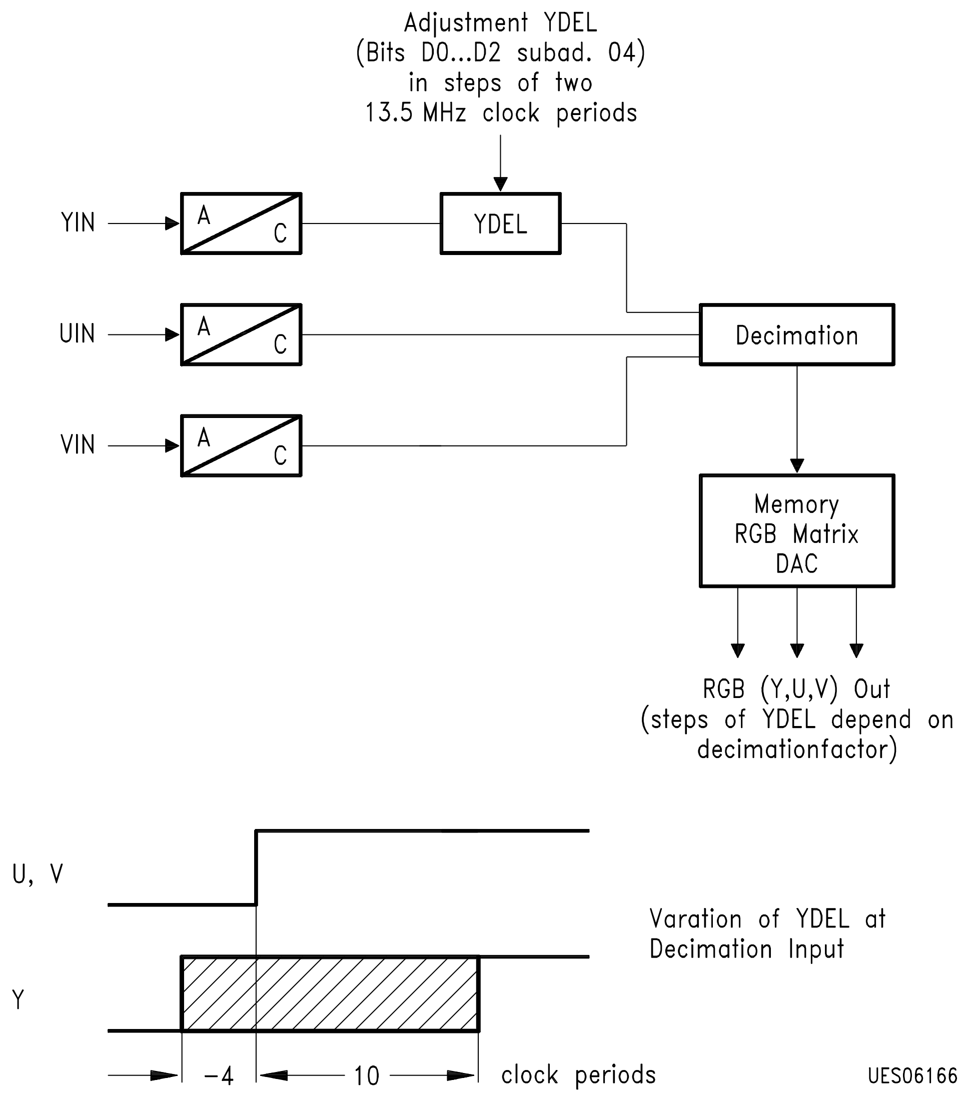


Signal Input Range 2 Vpp at Y, U, V

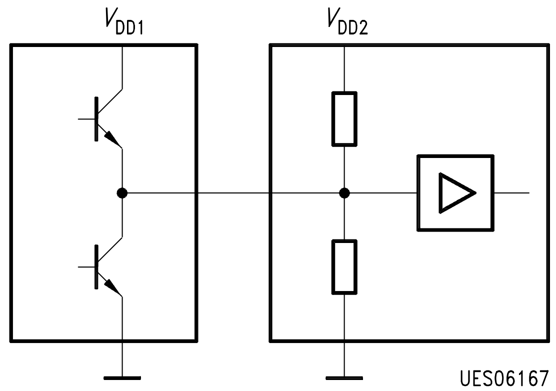


Signal Input Range 0.5 Vpp at Y, U, V

7.2 Adjustment of YDEL

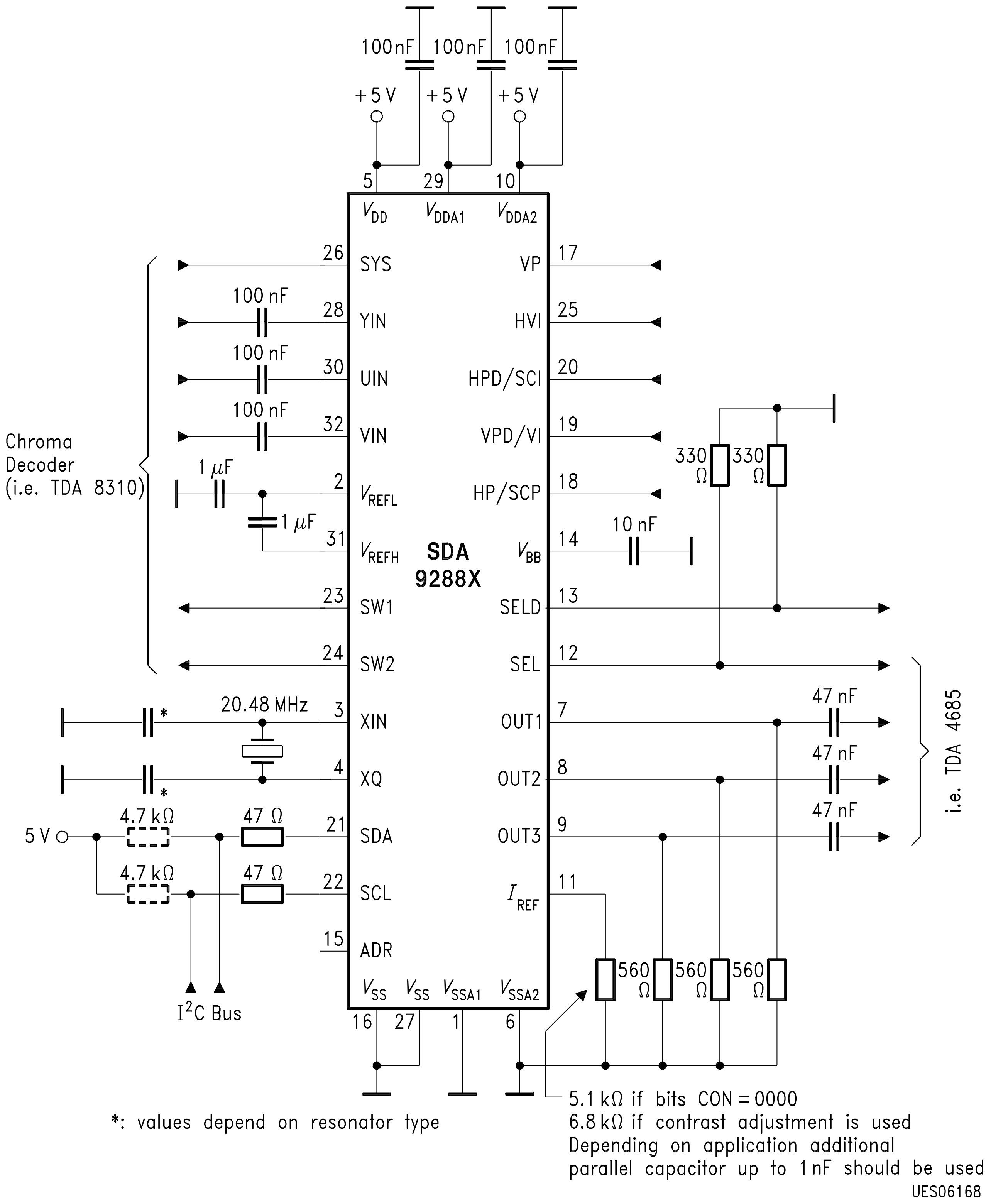


7.3 Three Level Interface (3-L)



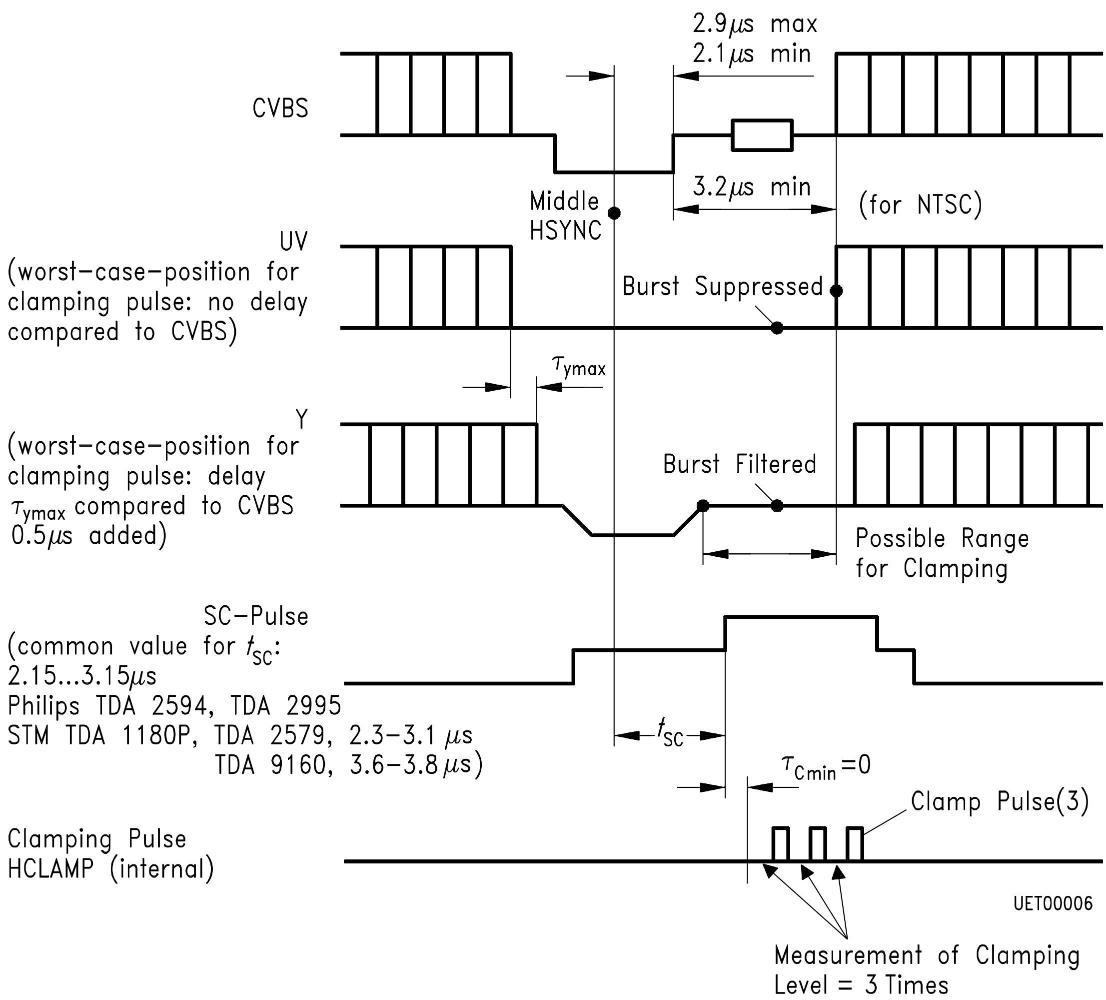
High Level (H):	upper transistor on, lower transistor off
Medium Level (M):	both transistors off (interface voltage determined by input stage)
Low Level (L):	upper transistor off, lower transistor on

7.4 Application Circuit (R, G, B-Mode)



8 Waveforms

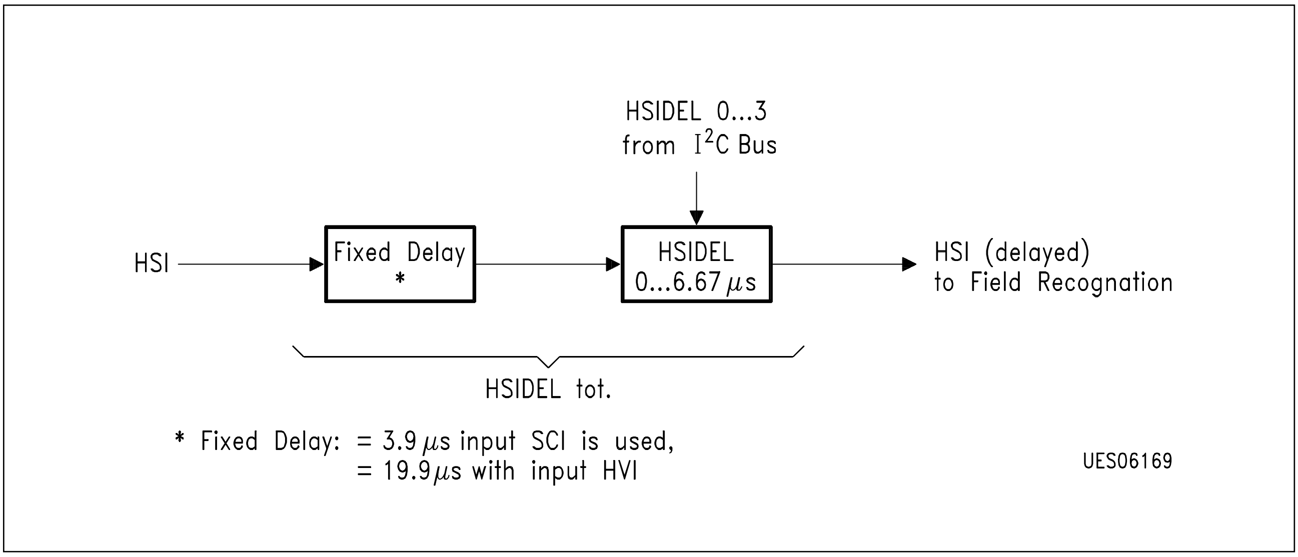
8.1 Timing of ADC Clamping



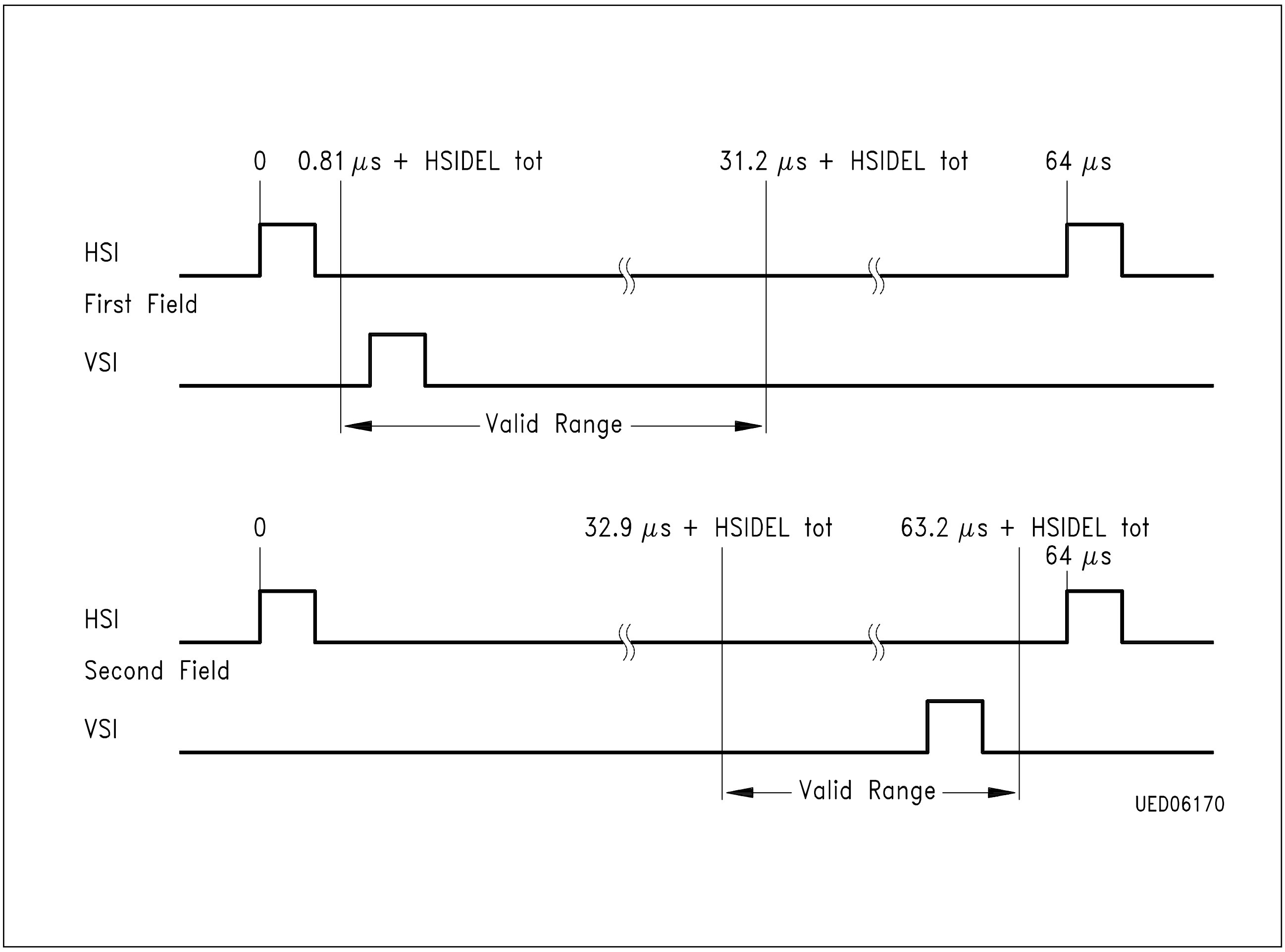
The values of t_m and t_c depend on the value of subaddress 06 (HSIDEL, CLISW).
If it is 00:
t_m(min) = 166 ns ± 6 % for the Y output and 240 ns ± 6 % for U, V;
t_c(min) = 296 ns ± 6 % for the Y output and 444 ns ± 6 % for U, V;

To get the maximum values 444 ns for each step of HSIDEL adjustment must be added.

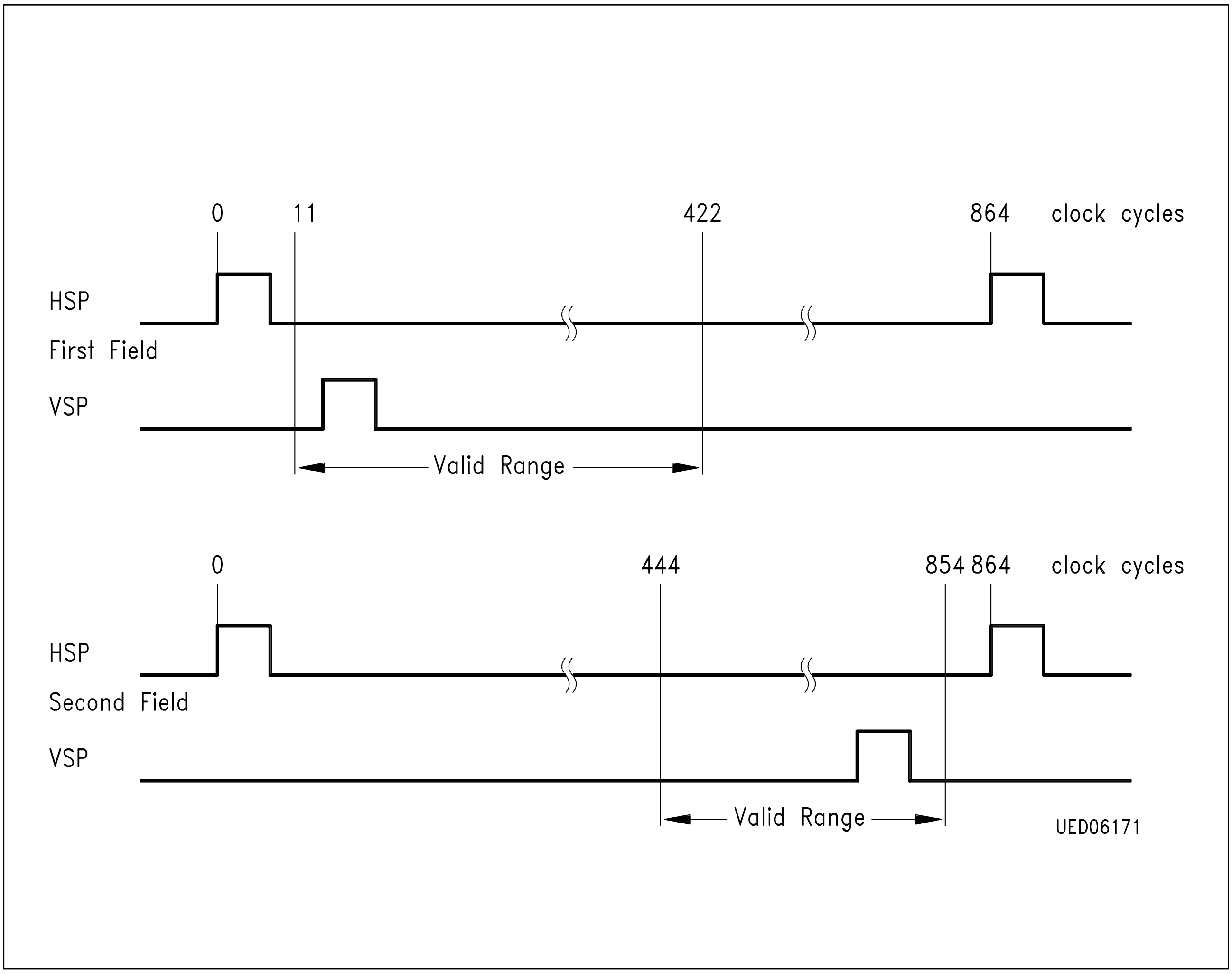
8.2 Phase Relation of Sync Pulses at Frame Mode



Signal Flow of the Horizontal Synchronization (Insert Part)



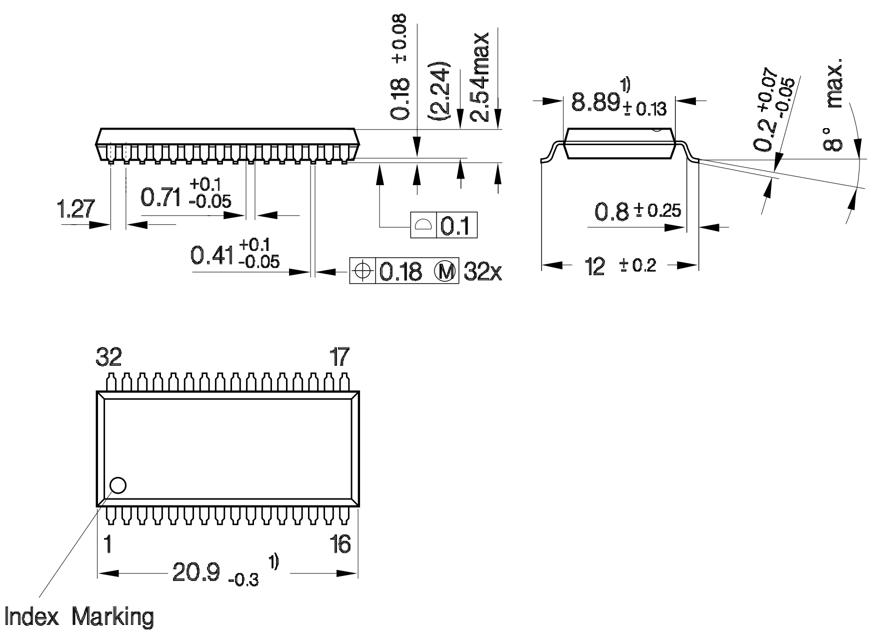
Allowed Phase Relation of the Horizontal/Vertical Sync Pulses (Insert Channel) if VSIDEL 0:4 = 0000



Allowed Phase Relation of the Horizontal/Vertical Sync Pulses (parent channel) if VSPDEL 0:4 = 0000

9 Package Outlines

Plastic Package, P-DSO-32-2 (SMD)
(Plastic Dual Small Outline Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”

SMD = Surface Mounted Device

Dimensions in mm