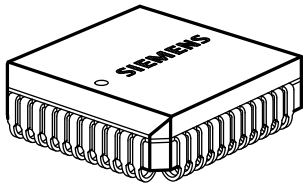
SIEMENS

Memory Sync Controller III — SDA 9220-5

Preliminary Data — **MOS IC**

Features

- Large area flicker elimination through field doubling
- Additional elimination of interline flicker in field mode
- Field switching and selection in field mode
- Noise and cross-color reduction
- Stills
- 9-image display, still-in-picture, picture-in-still with different frame versions
- Zoom with selection of enlarged picture segment (8 x 12 positions)
- Pin-programmable operation without standard conversion



P-LCC-44-1

Type	Ordering Code	Package
SDA 9220-5	Q67100-H5087	P-LCC-44-1 (SMD)

Functional Description

The MSC III is a component of the TV-SAM Featurebox and is responsible for driving the picture memory devices (TV-SAMs) and generating sync signals (**figure 6**). Together with the other devices of the Featurebox it enhances picture quality and offers a number of special operating modes.

The MSC III is set via the I^2C Bus, it being possible to switch the I^2C Bus address by hardware so that implementation of a simple frame Featurebox is possible in conjunction with the signal MUX supplied by the MSC III.

Other major output signals of the SDA 9220-5, in addition to the clocks LL3X (13.5 MHz) and LL1.5X (27 MHz), are the memory-driving signals ($\overline{RA}$, $\overline{RB}$, $\overline{WT}$, $\overline{RE}$, SCAD, SCA) and the sync signal CSY for the teletext device. The horizontal sync signals (HS2, BLN2) and the vertical sync signals (VS1, VS2) are also generated.

Circuit Description

The MSC III can be divided into the following function blocks (**figure 6**):

- Sync-signal generator
- Memory controller
- Clock generator
- I^2C Bus receiver

The sync-signal generator uses signals VS and BLN to produce the horizontal and vertical sync signals BLN2, HS2, VS1 and VS2. It supplies the composite sync signal CSY for the 100-Hz teletext, the control signal MUX for implementing a simple frame Featurebox and the frame signal FRM for inserting a colored frame in multi-picture, still-in-picture and picture-in-still modes. Signal CFH is output to prevent the bottom flutter effect in the video cassette recorder mode.

In operation without standard conversion (pin-programmable) signals BLN2, VS2 and FRM are switched from double to single line/field frequency. Outputs CSY and HS2 are not required in this case.

The memory controller produces the driving signals ($\overline{RA}$, $\overline{RB}$, $\overline{WT}$, $\overline{RE}$) and the addresses (SAR, SAC) for the memory devices (TV-SAMs). In addition, it produces the DREQ pulses used for requesting data from the picture processor during operation with reduced pictures. Two refresh operations are performed in the memory for each TV line.

The clock generator consists essentially of a PLL which generates the internal and exported system clocks from input clock LL3 or LL1.5 and synchronizes them with the horizontal blanking signal. The MSC can be set to one of the two input frequencies via input LLSEL. For the possible use of the Featurebox as a channel scanner, the PLL incorporates a crystal-controlled reference clock to ensure an undisturbed clock supply for memory output (stills sequence) during channel-switching phases.

All modes (except switching off the standard conversion) are set by appropriate programming of the I^2C Bus data bytes. When the operating voltage is switched on, all bits of the associated control registers are set to 0. The address of the I^2C Bus is set with signal ADR (24_H or 26_H).

Detailed Circuit Description

Picture Formats

The MSC forms part of a digital television system with line-locked scanning frequency. The nominal word rate is 13.5 MHz for luminance and 3.375 MHz for each of the U and V color components. The active region of a TV line is identified by the high time interval of BLN. It comprises 720 pixels for luminance and 180 pixels each for U and V and is stored in its entirety. In the 50-Hz standard a field consists of 287.5 lines and in the 60-Hz standard of 243.5 lines.

288 lines are stored in the 50-Hz standard (lines 23-310 of the first field, lines 336-623 of the second field) and 243 lines in the 60-Hz standard (lines 17-259 of the first field, lines 280-522 of the second field), (**figure 1**). In the 9-image mode a field without a frame consists of 208 pixels per line for luminance and 2 x 52 pixels per line for chrominance, with four pixels being lost for luminance and 2 x 1 for chrominance with memory or display frames. The number of lines without a frame is 84 for the 50-Hz standard and 71 for the 60-Hz standard. Two lines less are displayed with a frame (**figures 2 and 3**).

In the picture-in-still (PIS) and still-in-picture (SIP) modes a field without a frame or having a display frame is of the same size as a 9-image window. With the memory frame, however, eight pixels are lost for luminance and 2 x 2 for chrominance (**figure 4**).

For generating the windows in the modes 9-image display, PIS and SIP the picture data are filtered horizontally and vertically in the picture processor and reduced by a factor of three.

In the zoom mode a segment of the stored picture is enlarged by a factor of two by displaying each pixel twice as long and each line twice. The position of this picture segment is selectable.

Eight vertical and twelve horizontal positions can be set by the I^2C Bus (**figure 5**).

Random Interlace

The phase of VS relative to HS and the active picture content is measured at the input. At the output VS2 is generated in the same phase relation to HS2 and the picture content. Despite the random interlacing this means that standard picture conversion is possible without any visible interference.

Display Raster

There are three ways of displaying the field sequence: one is without interlace and two are with interlace, i.e. with a 50-Hz or 60-Hz interlace frequency or a 100-Hz or 120-Hz interlace frequency respectively. In what follows these are referred to symbolically as $\alpha\alpha\alpha\alpha$, $\alpha\alpha\beta\beta$ or $\beta\alpha\beta\alpha$. They are produced by a suitable sequence of the vertical sync pulses VS2 for the standard-converted video signal. The symbols α_n, β_n denote the vertical sync phases of the pulses (VS, VS2) referred to the horizontal blanking signals (BLN, BLN2), i.e. αn when the positive vertical sync edge falls within one blanking half cycle and β_n when it falls within the complementary blanking half cycle.

Normally the input signal will be as follows: (α_{n-1}, β_{n-1}) (α_n, β_n) (α_{n+1}, β_{n+1}) with α_n and β_n virtually constant. **Figures 15, 16, 17, 18 and 19** show the sequence obtained for output signal VS2 when using one of the three operating modes.

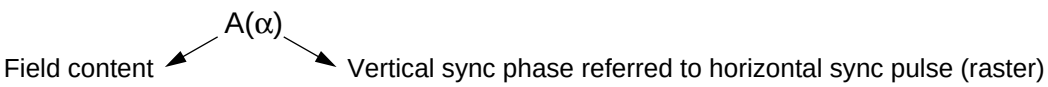
The standard conversion (SC) function can be activated via pin NW

- The following correlation exists:
  Low level at pin NW: Mode without standard conversion
  High level at pin NW: Mode with standard conversion
  If the standard conversion is switched on, there is a 100-(120-) Hz field frequency in the 50-(60)-Hz standard.
  Field sequence with SC: A(α) A(α) B(β) B(β) [1)]
  Field sequence without SC: A(α) B(β)

The following functions can be set on the I²C Bus [2)] interface:

- Still
  Field sequence with SC and interlace: A(β) A(α) A(β) A(α)
  or B(α) B(β) B(α) B(β)
  Field sequence with SC and without interlace: A(α) A(α) A(α) A(α)
  or B(β) B(β) B(β) B(β)
  Field sequence without SC and without interlace: A(α) A(α)
  or B(β) B(β)
- Teletext text mode: $A_{VT}(\alpha)$ $A_{VT}(\alpha)$ $A_{VT}(\alpha)$ $A_{VT}(\alpha)$
  or: $A_{VT}(\beta)$ $A_{VT}(\alpha)$ $A_{VT}(\beta)$ $A_{VT}(\alpha)$
  Teletext mixed mode:
  with SC $A_{VT}(\alpha)$ $A_{VT}(\alpha)$ $A_{VT}(\beta)$ $A_{VT}(\beta)$
  without SC $A_{VT}(\alpha)$ $A_{VT}(\beta)$
- Teletext field mode: In this mode every second field is written to the field memory. The display raster is freely selectable. Although the vertical resolution of the TV picture is slightly less in this mode, the lack of background edge flicker improves the visual effect in teletext mixed mode. An improvement in the picture can also be achieved with VCR signals in the special modes. It is also possible to select a particular field; this is useful for specific requests.
- HS2 phase: Programmable between 0 and 32 µs in increments of approx. 300 ns (for delay equalization between picture generation and deflection).
- Write operation delay owing to delay in the picture processor for noise reduction can be set between 0 and 14 or 16 and 30 LL3X clocks.
- When the color frame is used, the picture-in-picture and multi-picture modes have to be activated without the software frame because the two are not identical.
- The picture-in-picture and multi-picture modes cannot be switched on in the field mode; there may otherwise be no gray backing for the frame function, depending on the field. The field mode can only be activated one field after the picture-in-picture or multi-picture mode.

1)



2) I²C Bus: Bus system patented by Philips

- When switching from free running to line-locked mode, the following maximum synchronization times can occur for standard signals:
  a) Vertical synchronization at
     50 (60) Hz and 100 (120) Hz: 220 (183) ms
  a) Horizontal synchronization at
     50 (60) Hz: 100 (83) ms
     100 (120) Hz: 100 (75) ms

Device Interfaces

The interfaces of this device are designed to work with the CSG SDA 9257 and triple ADC SDA 9205-2, or DMSD/CGC, the TV-SAMs SDA 9251-2X and Picture Processor SDA 9290-5. The standard conversion function can be enabled and disabled on one pin. All other functions are set on an I^2C Bus interface.

I^2C Bus Interface

1. Functional Overview

The following control signals are received on the I^2C Bus:

- Synchronization (EXSYN)
- Blanking (BLK)
- Control for frame mode (MUXI, MUXS)
- VS noise reduction (VNR)
- 50/60-Hz standard (VERT)
- Deflection raster (VDM 1-0)
- Field mode with field changeover (FLDM, FLDC, FLDF)
- Delay compensation for write channel (WDEL 4-0)
- Still (STB)
- Frame (FR)
- Write mode (WM 1-0)
- Picture position for 9-image, picture-in-picture (VPOS 1-0, HPOS 1-0)
- Zoom mode (ZM)
- Position of zoom detail (ZV 2-0, ZH 3-0)
- NTSC mode with 864 pixels per line (N864)
- HS2 phase relation (HP 6-0)
- Disabling of frame display signal (FRDIS)
- Delay of frame display signal (FRD 6-0)
- Duration of CFH signal (CFHW 3-0)
- Position of CFH signal (CFHP 3-0)

2. Description

Slave Address:

0	0	1	0	0	1	ADR

Receiver Format:

S	Slave Address	0	A	Sub Address	A	Data Byte	A	P

S: Start condition
A: Acknowledge
P: Stop condition

Data Byte Formats:

Function	**Sub-address**	**Data Byte**							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Control 1	00	EXSYN	BLK	MUXI	MUXS	VNR	VERT	VDM1	VDM0
Control 2	01	FLDM	FLDC	FLDF	WDEL4	WDEL3	WDEL2	WDEL1	WDEL0
Control 3	02	STB	FR	WM1	WM0	VPOS1	VPOS0	HPOS1	HPOS0
Zoom control	03	ZM	ZV2	ZV1	ZV0	ZH3	ZH2	ZH1	ZH0
HS2 phase	04	N864	HP6	HP5	HP4	HP3	HP2	HP1	HP0
FRM delay	05	FRDIS	FRD6	FRD5	FRD4	FRD3	FRD2	FRD1	FRD0
CFH control	06	CFHW3	CFHW2	CFHW1	CFHW0	CFHP3	CFHP2	CFHP1	CFHP0

The subaddress is incremented automatically.
When the operating voltage is applied (power-up reset), all registers are set to 0.

3. Detailed Tables

Control 1 (subaddress 00)

Synchronization	**Control Bit EXSYN (D7)**
External synchronization (line-locked)	0
Internal synchronization (free-running)	1

Blanking	**Control Bit BLK (D6)**
Picture enabled	0
Picture blanked	1

MUX Invert, MUX Strobe (**Figure 9b** shows the functional diagram of MUX)	**Control Bit**	
	MUXI (D5)	**MUXS (D4)**
MUX = L	0	0
MUX toggles with VS2 (for VS1 = H change to L)	0	1
MUX = H	1	0
MUX toggles with VS2 (for VS1 = H change to H)	1	1

VS Noise Reduction	**Control Bit VNR (D3)**
Mode 1 (window)	0
Mode 2 (flywheel)	1

50/60-Hz-Standard	**Control Bit Vert (D2)**
50-Hz standard	0
60-Hz standard	1

Deflection Raster	**Control Bit**	
	VDM 1 (D1)	**VDM 0 (D0)**
$\alpha\alpha\beta\beta$ (with standard conversion) $\alpha\beta$ (w/o standard conversion)	0	0
$\alpha\alpha\alpha\alpha$ (with standard conversion) $\alpha\alpha$ (w/o standard conversion)	0	1
$\beta\alpha\beta\alpha$ (with standard conversion) not defined (w/o standard conversion)	1	0
Not defined	1	1

Control 2 (subaddress 01)

Field Mode	**Control Bit FLDM (D7)**
Normal mode (both fields)	0
Field mode (only one field)	1

Field Switching in Field Mode	**Control Bit FLDC (D6)**
For FLDF = L: Change of field; (no reference to a specific field)	$0 \rightarrow 1$ $1 \rightarrow 0$
For FLDF = H: Field 1 displayed Field 2 displayed	0 1

Field Mode Feature Selection	**Control Bit FLDF (D5)**
Free-running field mode without field reference	0
Field mode with field reference	1

Write Operation Delay in LL3 Periods (from rising edge of BLN)	**Control Bit**				
	WDEL4 (D4)	**WDEL3 (D3)**	**WDEL2 (D2)**	**WDEL1 (D1)**	**WDEL0 (D0)**
Delay 0	0	0	0	0	0
to					
Delay 14	0	1	1	1	0
Delay 16	1	0	0	0	0
to					
Delay 30	1	1	1	1	0
Not defined	×	1	1	1	1

Control 3 (subaddress 02)

Still	**Control Bit STB (D7)**
Moving image	0
Still	1

Frame	**Control Bit FR (D6)**
9-image picture, picture-in-picture without frame	0
9-image picture, picture-in-picture with frame	1

Write Mode	**Control Bit**	
	WM 1 (D5)	**WM 0 (D4)**
Normal mode (NM)	0	0
9-image picture mode (MP)	0	1
Picture-in-still (PIS)	1	0
Still-in-picture (SIP)	1	1

Vertical Picture Position for 9th Image	**Control Bit**	
	VPOS 1 (D3)	**VPOS 0 (D2)**
Vertical position 0	0	0
Vertical position 1 (not allowed for PIS and SIP)	0	1
Vertical position 2	1	0
Not defined	1	1

Horizontal Picture Position for 9th Image	**Control Bit**	
	HPOS 1 (D1)	**HPOS 0 (D0)**
Horizontal position 0	0	0
Horizontal position 1 (not allowed for PIS and SIP)	0	1
Horizontal position 2	1	0
Not defined	1	1

Zoom Control (subaddress 03)

Zoom	Control Bit ZM (D7)
Normal	0
Zoom	1

Vertical Position of Zoomed Detail	Control Bit		
	ZV 2 (D6)	ZV 1 (D5)	ZV 0 (D4)
Vertical position 0	0	0	0
to			
Vertical position 7	1	1	1

Horizontal Position of Zoomed Detail	Control Bit			
	ZH 3 (D3)	ZH 2 (D2)	ZH 1 (D1)	ZH 0 (D0)
Horizontal position 0	0	0	0	0
to				
Horizontal position 11	1	0	1	1
Not defined	1	1	×	×

x: don’t care

HS2 Phase (subaddress 04)

Switching in 60-Hz Mode (VERT = 1)	Control Bit N864 (D7)
858 pixels per line	0
864 pixels per line	1

HS2 Phase	Control Bit						
	HP 6 (D6)	HP 5 (D5)	HP 4 (D4)	HP 3 (D3)	HP 2 (D2)	HP 1 (D1)	HP 0 (D0)
0 steps	0	0	0	0	0	0	0
to							
108 steps	1	1	0	1	1	0	0

One step corresponds to eight LL1.5 cycles (approx. 300 ns).

FRM Delay (subaddress 05)

FRM Disable	Control Bit FRDIS (D7)
Frame display signal FRM enable	0
Frame display signal FRM disable (FRM = L)	1

Delay for Frame Display Signal	Control Bit						
	FRD 6 (D6)	FRD 5 (D5)	FRD 4 (D4)	FRD 3 (D3)	FRD 2 (D2)	FRD 1 (D1)	FRD 0 (D0)
0 LL1.5 cycles	0	0	0	0	0	0	0
to							
127 LL1.5 cycles	1	1	1	1	1	1	1

CFH Control (subaddress 06)

CFH Width (H level)	Control Bit			
	CFHW3 (D7)	CFHW2 (D6)	CFHW1 (D5)	CFHW0 (D4)
0 halfline	0	0	0	0
to				
15 halflines	1	1	1	1

CFH Position Before VS	Control Bit			
	CFHP3 (D3)	CFHP2 (D2)	CFHP1 (D1)	CFHP0 (D0)
3 halflines	0	0	0	0
to				
18 halflines	1	1	1	1

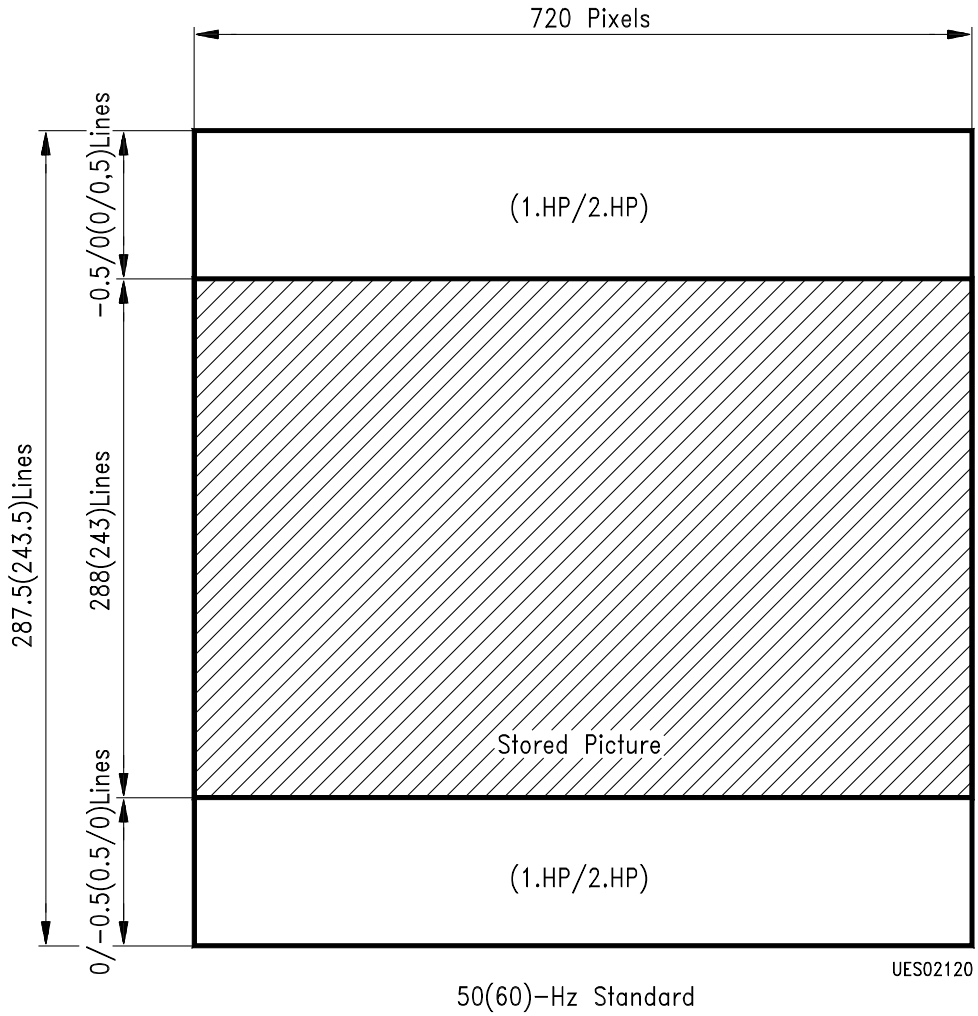


Figure 1
Picture Format, Normal Mode

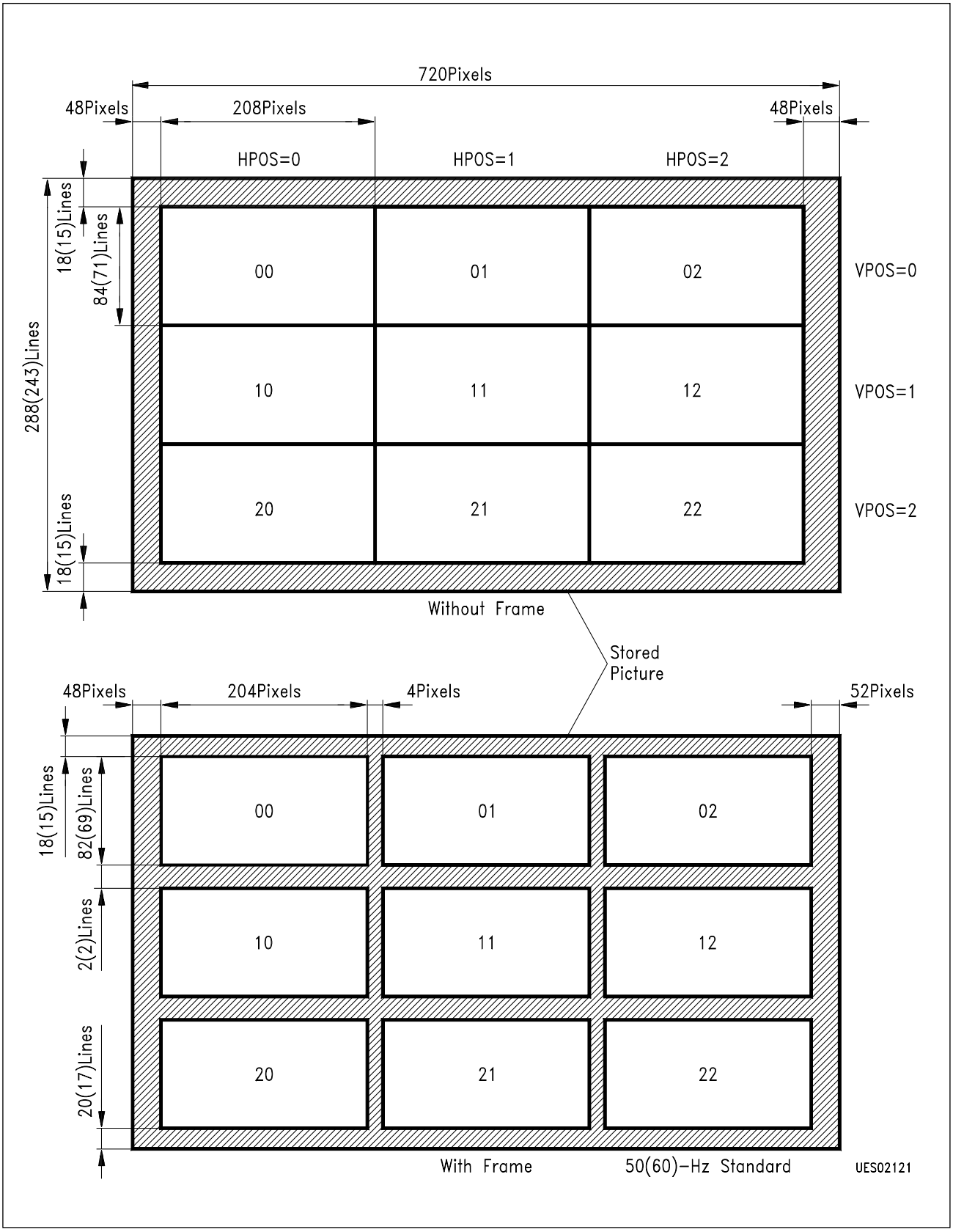


Figure 2
Picture Formats for 9-Image Mode

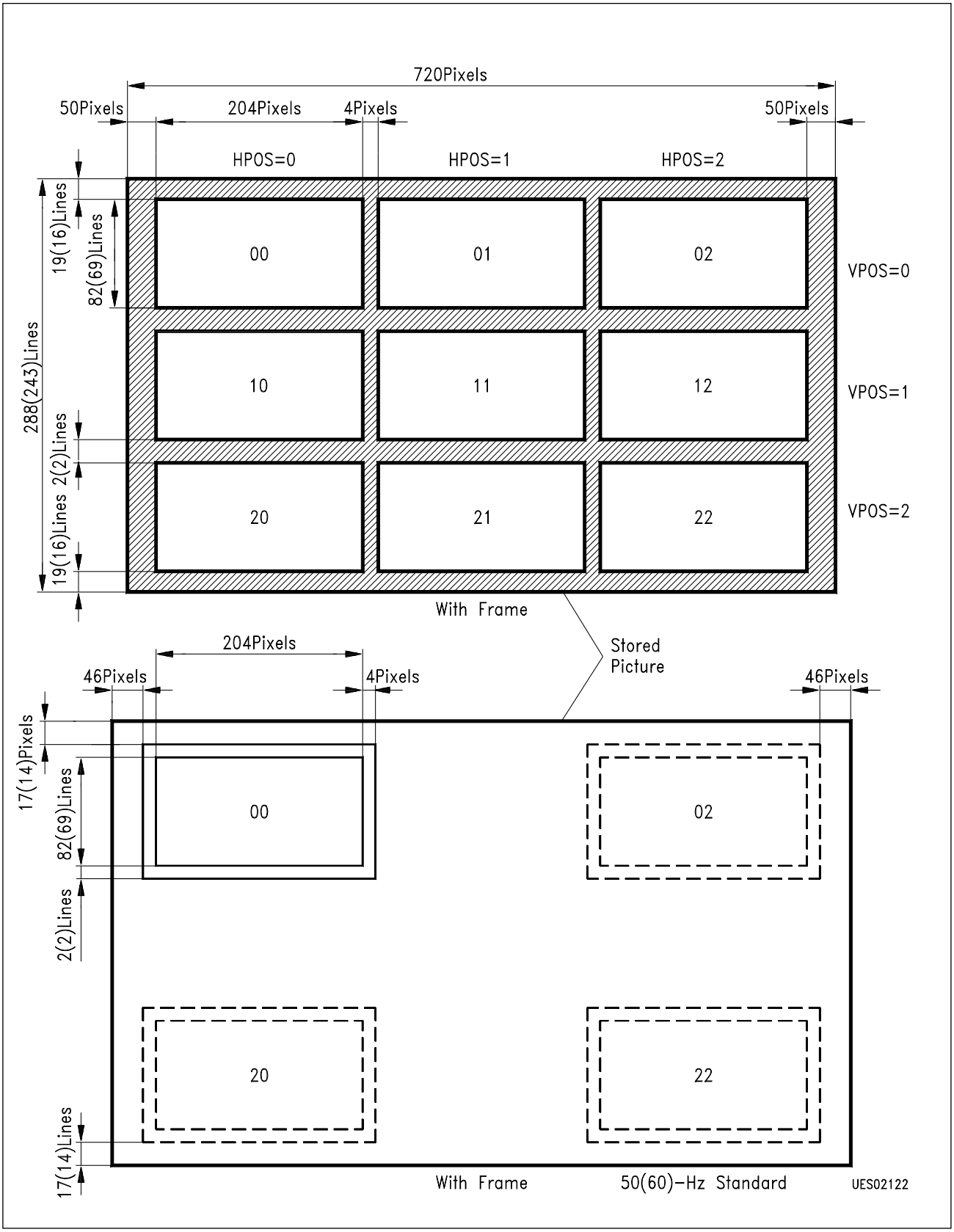


Figure 3
Picture Formats for 9-Image Mode, PIS and SIP with Display Frame

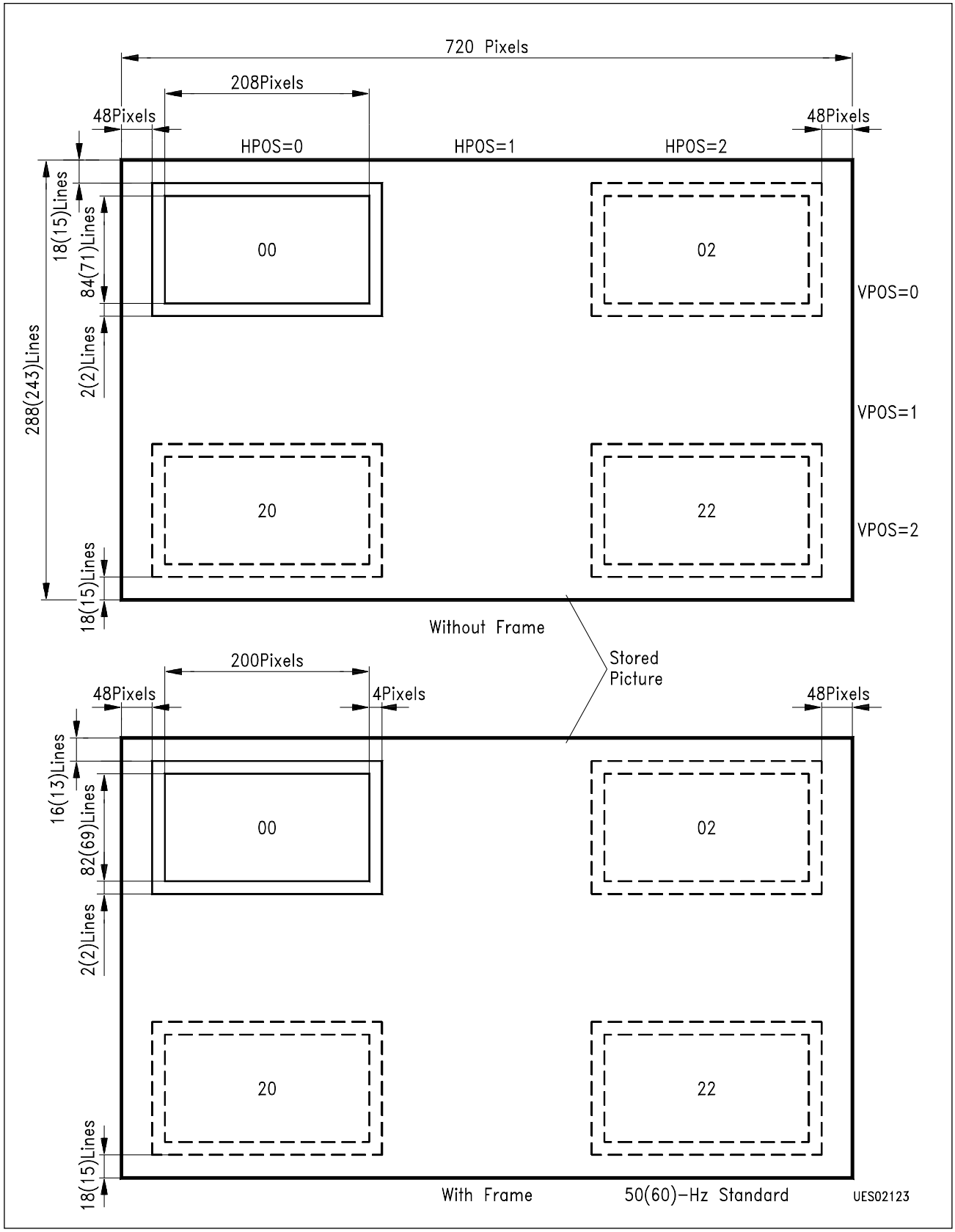


Figure 4
Picture Formats for Picture-in-Still, Still-in-Picture

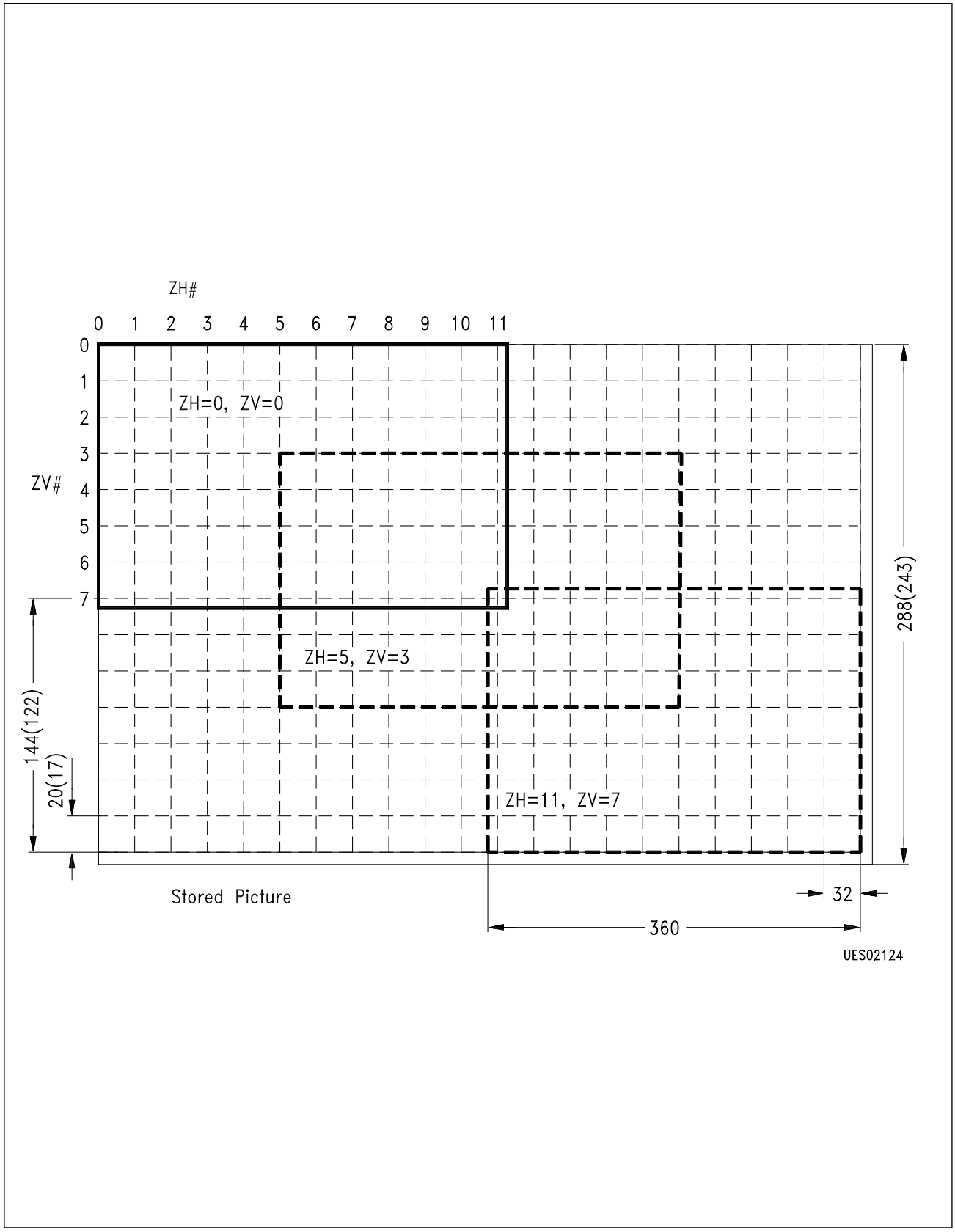


Figure 5
Zoomed Picture Segments

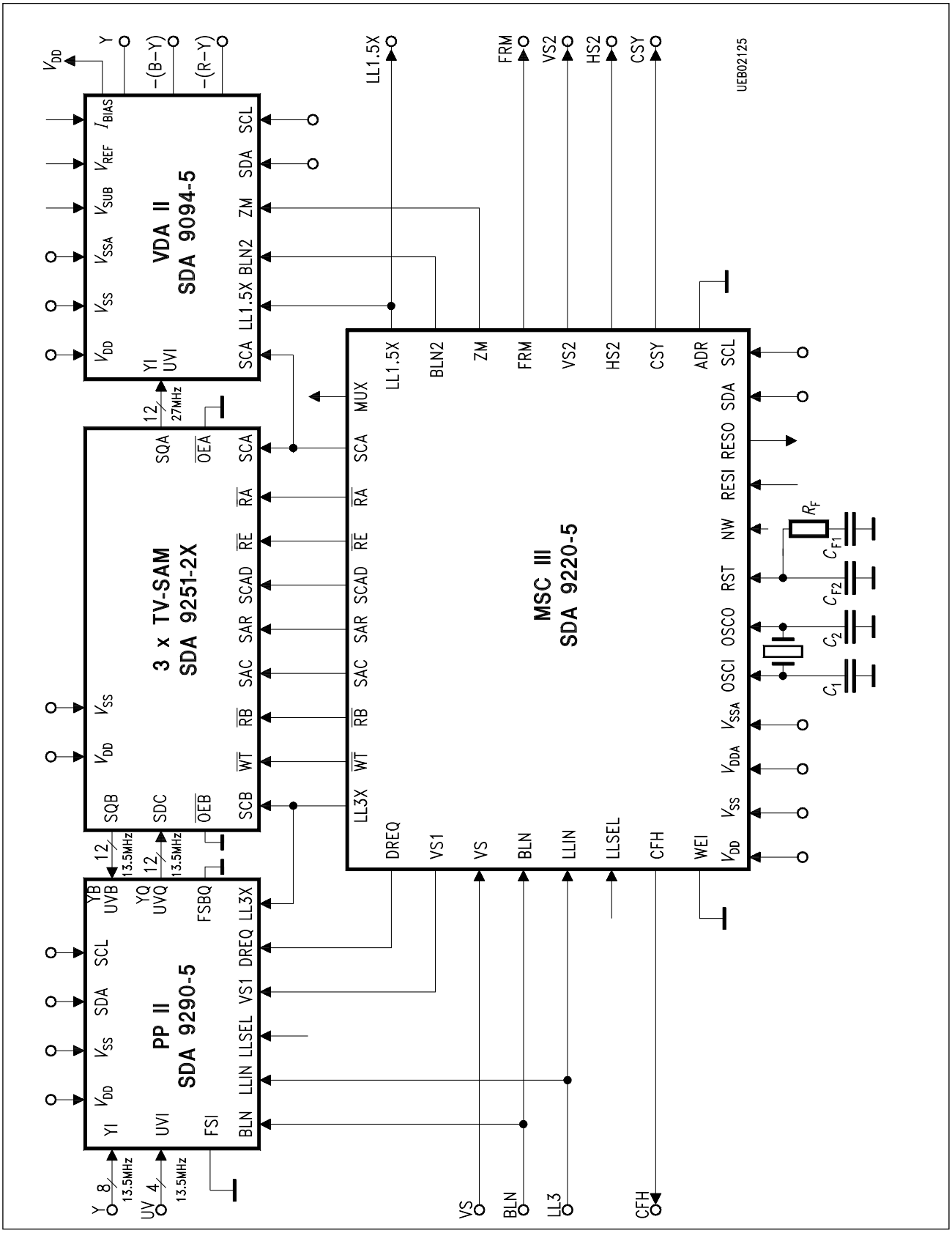


Figure 6
Block Diagram 1, Featurebox with Standard Conversion

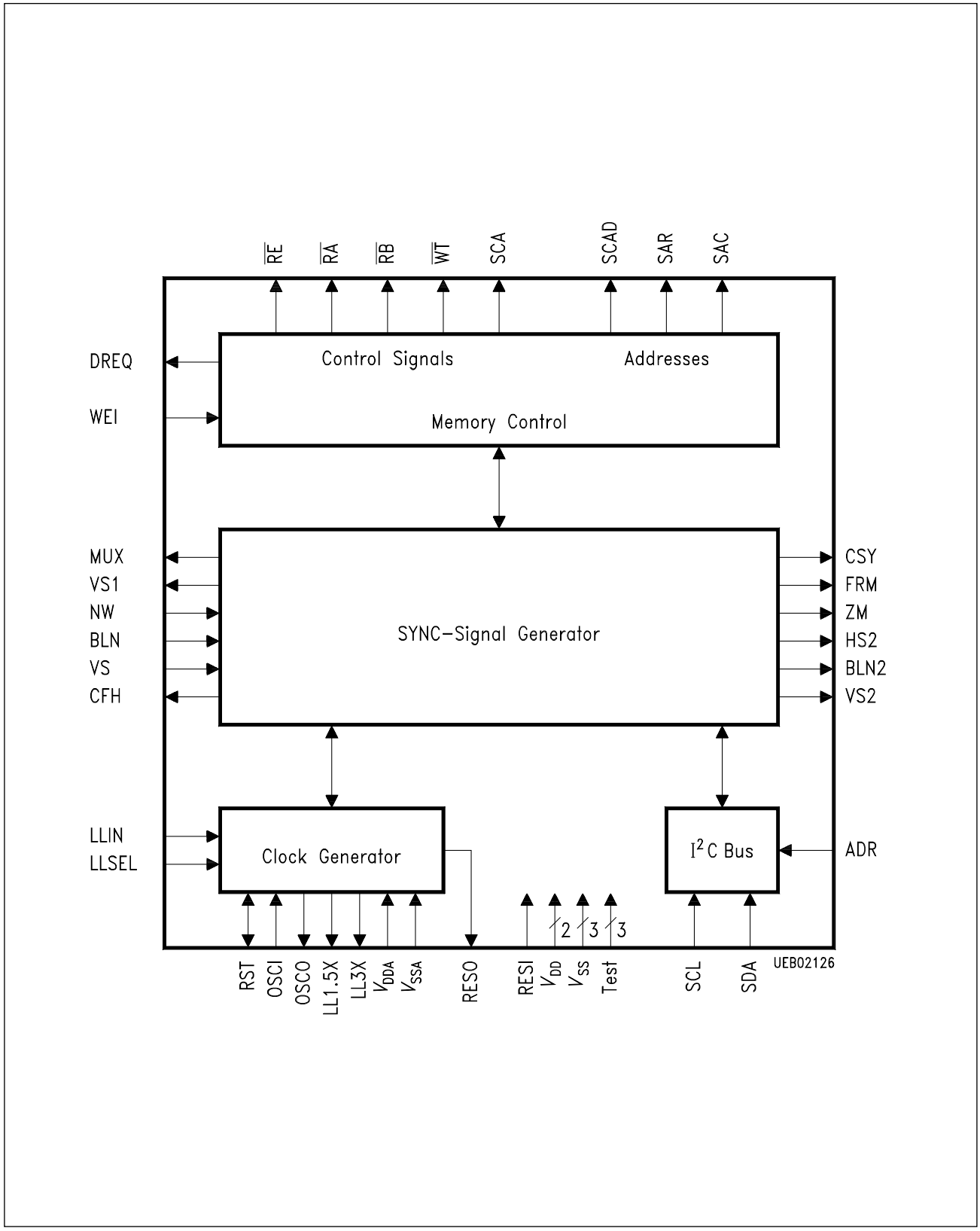
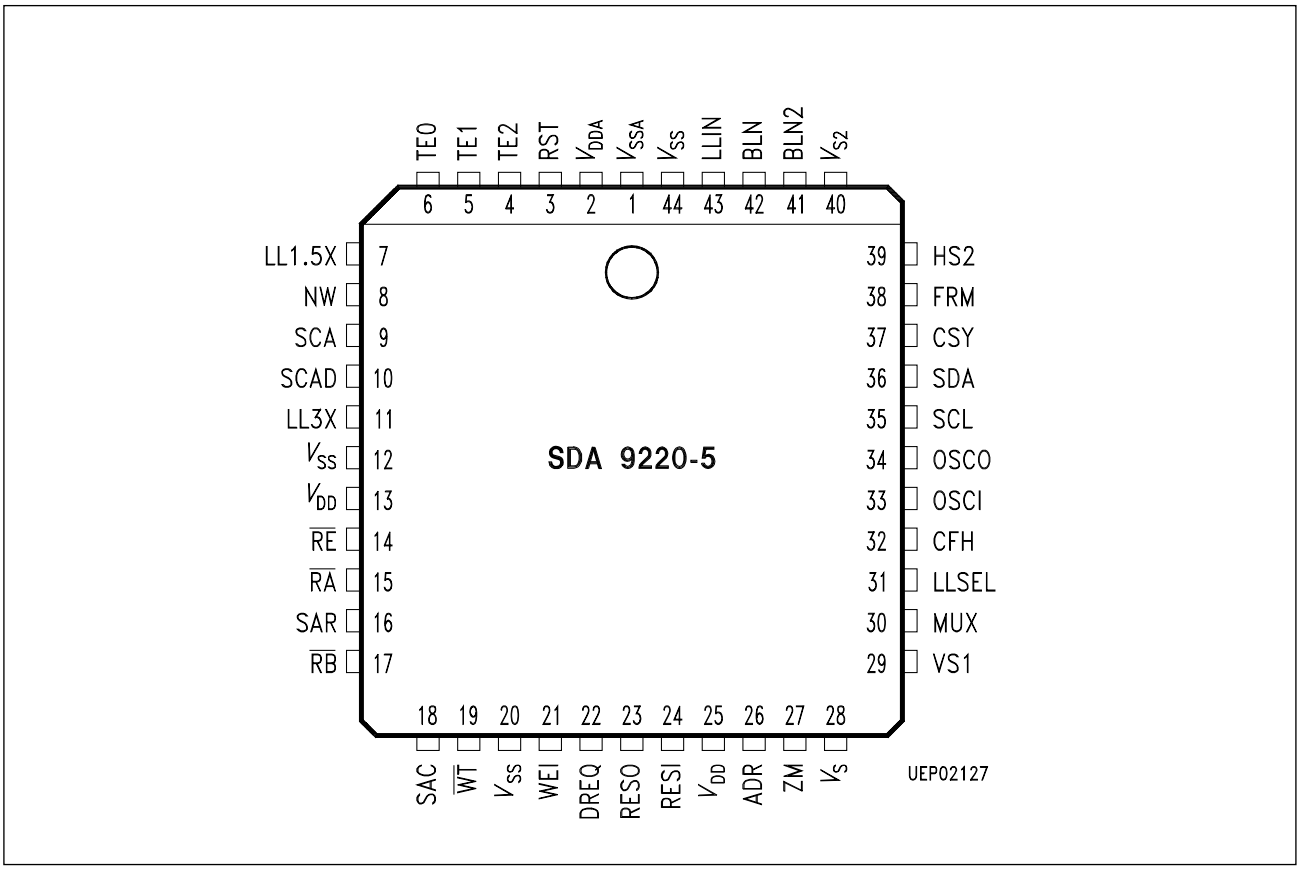


Figure 7
Block Diagram 2
Memory Sync Controller

Figure 8
Pin Configuration
(top view)



Pin Definitions and Functions

Pin No.	Symbol	Function	Description
1	V_{SSA}	Analog ground	
2	V_{DDA}	Analog supply voltage	Positive supply voltage (+ 5 V) for analog part
3	RST	PLL filter	Connecting pin for PLL filter
4	TE2	Test pin	Test pin; must be connected to V_{SS} for normal mode
5	TE1	Test pin	Test pin; must be connected to V_{SS} for normal mode
6	TE0	Test pin	Test pin; must be connected to V_{SS} for normal mode
7	LL1.5X	27-MHz clock	27-MHz clock for devices of Featurebox generated by PLL
8	NW	Select standard conversion	Standard-conversion switching; high level on this pin means that standard conversion is activated
9	SCA	Serial clock	Serial clock for port A of TV-SAM
10	SCAD	Serial address clock	Serial address clock for TV-SAM
11	LL3X	Clock	13.5-MHz clock for the devices of the Featurebox generated by PLL
12	V_{SS}	Digital ground	
13	V_{DD}	Digital supply voltage	Positive supply voltage
14	$\overline{RE}$	Row enable	Control signal for TV-SAM
15	$\overline{RA}$	Read transfer	Via port A of TV-SAM
16	SAR	Serial row address	For TV-SAM
17	$\overline{RB}$	Read transfer	Via port B of TV-SAM
18	SAC	Serial column address and mode	For TV-SAM
19	$\overline{WT}$	Write transfer	Via port C of TV-SAM
20	V_{SS}	Digital ground	
21	WEI	Write inhibit	Write-enable input for direct disabling of write operation for field memory
22	DREQ	Data request	Data-request signal in 9-image mode for reduced picture data; at same time I^2C Bus sync signal for picture processor
23	RESQ	Reset output	
24	RESI	Reset input	Normally on V_{DD} (active low)
25	V_{DD}	Digital supply voltage	Position supply voltage (+ 5 V) for digital part

Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Function	Description
26	ADR	Address select	24_H for ADR = 0 or 26_H for ADR = 1
27	ZM	Zoom signal	Control signal for Featurebox output interface IC: supplies high level in zoom mode
28	VS	Vertical sync	Input determines vertical position of TV picture for 50-or 60-Hz field frequency
29	VS1	Vertical sync	Output; noise suppressed
30	MUX	MUX switching	Switching signal for implementing simple frame Featurebox
31	LLSEL	Select clock input	A 27-MHz clock selected for LLSEL = low
32	CFH	Clock frequency hold	For elimination of bottom flutter effect in VCR mode
33	OSCI	Crystal oscillator input	
34	OSCQ	Crystal oscillator output	Crystal clock as reference for recovery in tuner scanning mode
35	SCL	Serial clock I^2C Bus	
36	SDA	Serial data I^2C Bus	
37	CSY	Composite sync	Horizontal and vertical sync pulses for Teletext device in standard-conversion mode
38	FRM	Display frame signal	Control signal output for possible insertion of colored frame in multi-picture, picture-in still and still-in-picture modes
39	HS2	Horizontal sync display	Horizontal pulse for standard-converted picture (31.25 / 31.47 kHz)
40	VS2	Vertical sync display	Vertical sync pulse for data readout
41	BLN2	Horizontal blank display	Blanking signal for identifying active picture line for data readout
42	BLN	Horizontal blank	Blanking signal input; high phase identifies active picture line
43	LLIN	Input clock	13.5 or 27 MHz
44	V_{SS}	Digital ground	

Absolute Maximum Ratings

(all voltages are referred to V_{SS})

Parameter	Symbol	Limit Values			Unit	Remarks
		min.	typ.	max.		
Ambient temperature	T_A	0		70	°C	
Storage temperature	T_{stg}	– 55		125	°C	
Thermal resistance	$R_{th\ SA}$			50	K/W	
Supply voltage	V_{DD}	– 0.3		6	V	
Input voltage	V_I	– 0.3		6	V	
Total power dissipation	P_{tot}			1.25	W	

Operating Range

Supply voltage	V_{DD}	4.5	5	5.5	V	
Supply current digital	I_{DDD}		200	240	mA	Sum pins 13, 27
Supply current analog	I_{DDA}		2	2.3	mA	Pin 2
Ambient temperature	T_A	0		70	°C	

Characteristics

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Input Clock LLIN = 13.5 MHz/LLSEL = High or Open (refer to figure 9 c)						
Period	T_{LLIN}	68	74	80	ns	
H-pulse width	t_{WH}	25			ns	
L-pulse width	t_{WL}	25			ns	
H-input voltage	V_{IH}	2			V	
L-input voltage	V_{IL}			0.8	V	
Input Clock LLIN = 27 MHz/LLSEL = Low (refer to figure 9 c)						
Period	T_{LLIN}	34	37	40	ns	
H-pulse width	t_{WH}	10			ns	
L-pulse width	t_{WL}	10			ns	
H-input voltage	V_{IH}	2			V	
L-input voltage	V_{IL}			0.8	V	
Input Signal BLN, VS, WEI/Reference Clock: LLIN = 13.5 MHz (refer to figure 9c)						
Setup time	t_{SU}	14			ns	
Hold time	t_{IH}	5			ns	
H-input voltage	V_{IH}	2			V	
L-input voltage	V_{IH}			0.8	V	
H-input current	I_{IH}	– 80		– 500	µA	
L-input current	I_{IL}	– 100		– 500	µA	
Input Signal BLN, VS, WEI/Reference Clock: LLIN = 27 MHz (refer to figure 9c)						
Setup time	t_{SU}	7			ns	
Hold time	t_{IH}	6			ns	
H-input voltage	V_{IH}	2			V	
L-input voltage	V_{IL}			0.8	V	
H-input current	I_{IH}	– 80		– 500	µA	
L-input current	I_{IL}	– 100		– 500	µA	

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output Clock LL1.5X/Reference Clock: LLIN (refer to figure 9a)						
Period	$T_{LL1.5X}$	34	37	40	ns	
H-pulse width	t_{WH}	12			ns	
L-pulse width	t_{WL}	12			ns	
Clock skew *)	t_{SK}	0		15	ns	
Load capacitance	C_L			50	pF	
H-output voltage	V_{QH}	2.4			V	I_{QH} = – 2.5 mA
L-output voltage	V_{QL}			0.4	V	I_{QL} = 5 mA
Output Clock LL3X/Reference Clock: LLIN (refer to figure 9a)						
Period	T_{LL3X}	68	74	80	ns	
H-pulse width	t_{WH}	25			ns	
L-pulse width	t_{WL}	25			ns	
Clock skew *)	t_{SK}	0		15	ns	
Load capacitance	C_L			50	pF	
H-output voltage	V_{QH}	2.4			V	I_{QH} = – 2.5 mA
L-output voltage	V_{QL}			0.4	V	I_{QL} = 5 mA

*) With steady-state PLL.

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output Clock SCA/Reference Clock: LL1.5X (refer to figure 9a)						
H-pulse width	t_{WH}	10		25	ns	
L-pulse width	t_{WL}	10			ns	
Clock skew **)	t_{SK}	0		15	ns	
Load capacitance	C_L			50	pF	
H-output voltage	V_{QH}	2.4			V	I_{QH} = – 2.5 mA
L-output voltage	V_{QL}			0.4	V	I_{QL} = 5 mA
Period	T_{SCA1}	34	37	40	ns	Normal mode with standard conversion
	T_{SCA2} ***)	68	74	80	ns	Normal mode without standard conversion or zoom mode with standard conversion
	T_{SCA3} ***)	136	148	160	ns	Zoom mode without standard conversion
Output Clock SCAD/Reference Clock: LL3X (refer to figure 9a)						
Period	T_{SCAD}	34	37	40	ns	
H-pulse width	t_{WH}	12			ns	
L-pulse width	t_{WL}	12			ns	
Clock skew *)	t_{SK}	– 15		0	ns	
Load capacitance	C_L			50	pF	
H-output voltage	V_{QH}	2.4			V	I_{QH} = – 2.5 mA
L-output voltage	V_{QL}			0.4	V	I_{QL} = 5 mA

*) With steady-state PLL and provided that the capacitive load of the reference clock is identical or more.

**) With steady-state PLL and provided that the capacitive load of the reference clock is identical or less.

***) $T_{SCA2/3}$ are generated from T_{SCA1} (by blanking the high phases).

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output Signals: BLN2, FRM, ZM, HS2, VS2/Reference Clock: LL1.5X (refer to figure 9b)						
Delay time (for HS2, VS2)	t_{QD}			20	ns	
Delay time (for BLN2, FRM, ZM)	t_{QD}			25	ns	
Hold time	t_{QH}	6			ns	
Load capacitance	C_L			30	pF	
H-output voltage	V_{QH}	2.4			V	I_{QH} = – 2.5 mA
L-output voltage	V_{QL}			0.4	V	I_{QL} = 5 mA
Output Signals: $\overline{\text{WT}}$, $\overline{\text{RB}}$, CSY, VS1, MUX, DREQ, CFH/Reference Clock: LL3X (refer to figure 9b)						
Delay time	t_{QD}			25	ns	
Hold time	t_{QH}	6			ns	
Load capacitance for $\overline{\text{WT}}$, $\overline{\text{RB}}$	C_L			50	pF	
Load capacitance for CSY, VS1, DREQ, CFH	C_L			30	pF	
H-output voltage	V_{QH}	2.4			V	I_{QH} = – 2.5 mA
L-output voltage	V_{QL}			0.4	V	I_{QL} = 5 mA
Output Signals: $\overline{\text{RA}}$/Reference Clock: SCA (refer to figure 9b)						
Delay time	t_{QD}			15	ns	
Hold time	t_{QH}	0			ns	
Load capacitance	C_L			50	pF	
H-output voltage	V_{QH}	2.4			V	I_{QH} = – 2.5 mA
L-output voltage	V_{QL}			0.4	V	I_{QL} = 5 mA

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output Signals: SAR, SAC, $\overline{RE}$/Reference Clock: SCAD (refer to figure 9b)						
Delay time for SAR, SAC	t_{QD}			25	ns	
Delay time for $\overline{RE}$	t_{QD}			20	ns	
Hold time	t_{QH}	6			ns	
Load capacitance	C_L			50	pF	
H-output voltage	V_{QH}	2.4			V	I_{QH} = – 2.5 mA
L-output voltage	V_{QL}			0.4	V	I_{QL} = 5 mA
PLL-Filter Currents						
Charge current	I_{CH}	80		250	µA	V_{QL} = 1.9 V
Charge current	I_{CH}	70		250	µA	V_{QL} = 2.9 V
Discharge current	I_{DCH}	– 80		– 300	µA	V_{QL} = 1.9 V
Discharge current	I_{DCH}	– 70		– 300	µA	V_{QL} = 2.9 V
Filter Elements (see figure 10a) $C_{F1} \approx$ 1.5 nF, $R_F \approx$ 1.8 kΩ, $C_{F2} \approx$ 100 pF						
Crystal (see figure 10b)						
Nominal frequency	f_Q		6.7500		MHz	
Effect of temperature and accuracy of adjustment	$\Delta f/f_Q$					
Temperature range	T_A	0		70	°C	
Load capacitance	C_L		33 ± 0.5		pF	
Resonant impedance	Z_R		60		Ω	
Equivalent parallel C	C_O			7 ± 20 %	pF	
Crystal load				0.1	mW	

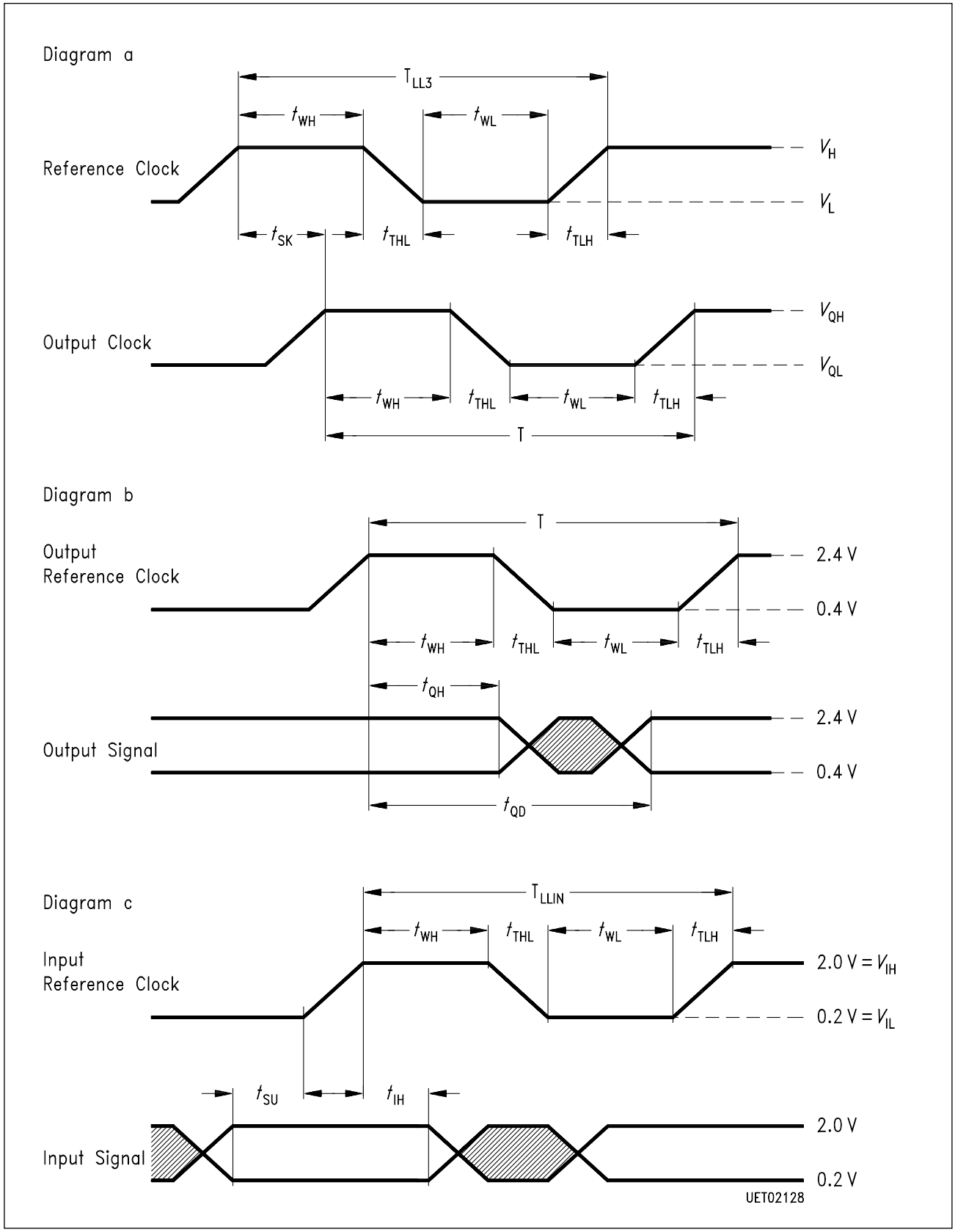


Figure 9
Timing Diagram (for characteristics of SDA 9220-5)

a) Filter Circuitry **b) Crystal Circuitry**

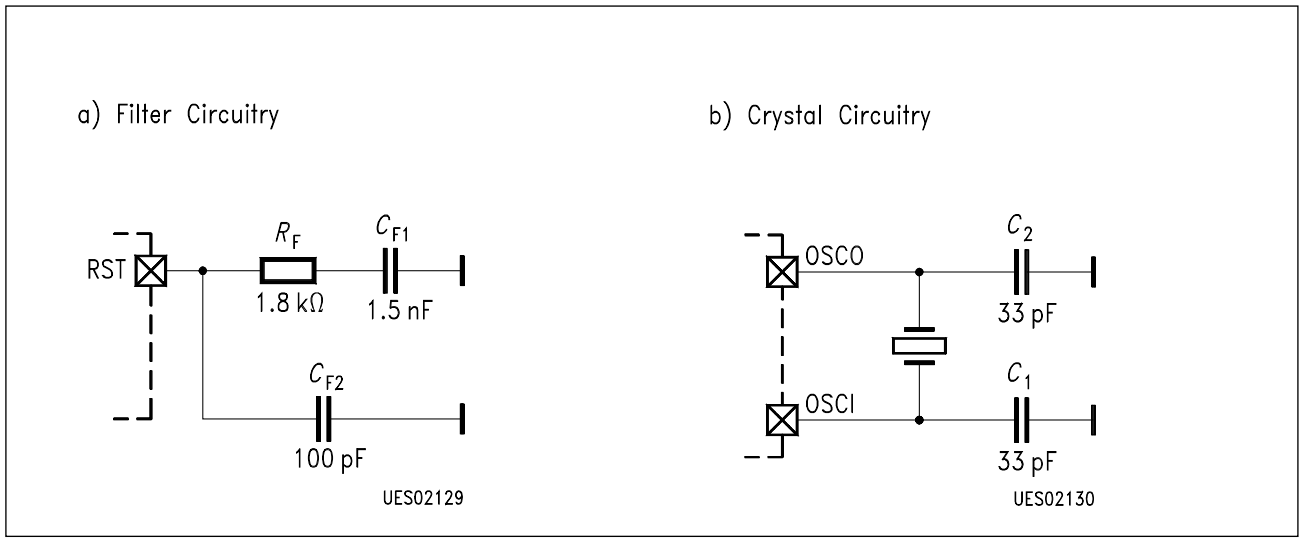


Figure 10
Circuit Configuration for Filter and Crystal

Reset Behavior of SDA 9220-5

The circuitry has sensor logic for separately detecting values below the minimum supply level on the V_{DDA} and the two V_{DD} pins. A reset cycle is initiated whenever such values are detected; the reset time is preset by charging and discharging the pin capacitance of the reset input pin which is not normally connected. This time can be extended by connecting RESI with an external capacitance. The RESI pin can also be connected directly with a signal; a RES low level enables reset, a RES high level terminates the reset. The internal circuit reset status is output via reset RESQ and can then be used as an active low signal (low level = reset status). During the reset phase all the output clocks generated by MSC (LL1.5X, LL3X, SCA and SCAD) are kept at low level. Upon completion of the reset the SDA 9220-5 is in its basic (line-locked) mode. If no clock is applied to LLIN at this point of time, the VCO in the PLL oscillates at its free-running frequency (5–20 MHz) and enables all the output clocks derived from it.

– Typical Control Values for the Reset System

Initiation level for reset on V_{DD}	V_{DDR}	< 3.9 V
Low level on RESI	V_{RIL}	< 1.5 V
High level on RESI	V_{RIH}	> 2.3 V
Output low level on RESQ	V_{QL}	≤ 0.4 V (I_{QL} = 5 mA)
Output high level on RESQ	V_{QH}	≥ 2.4 V (I_{QH} = – 2.5 mA)

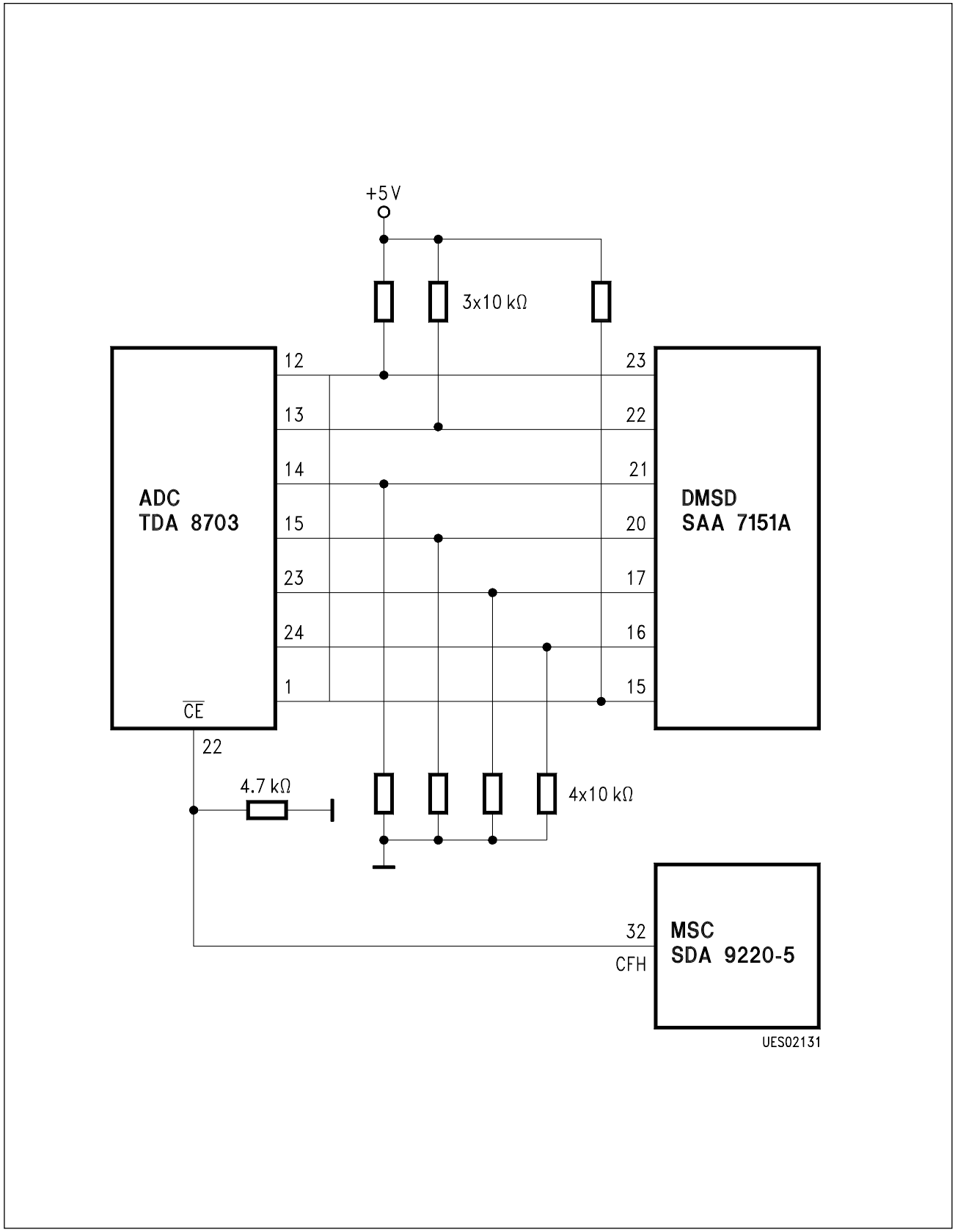


Figure 11
Application Circuit for Eliminating Bottom Flutter

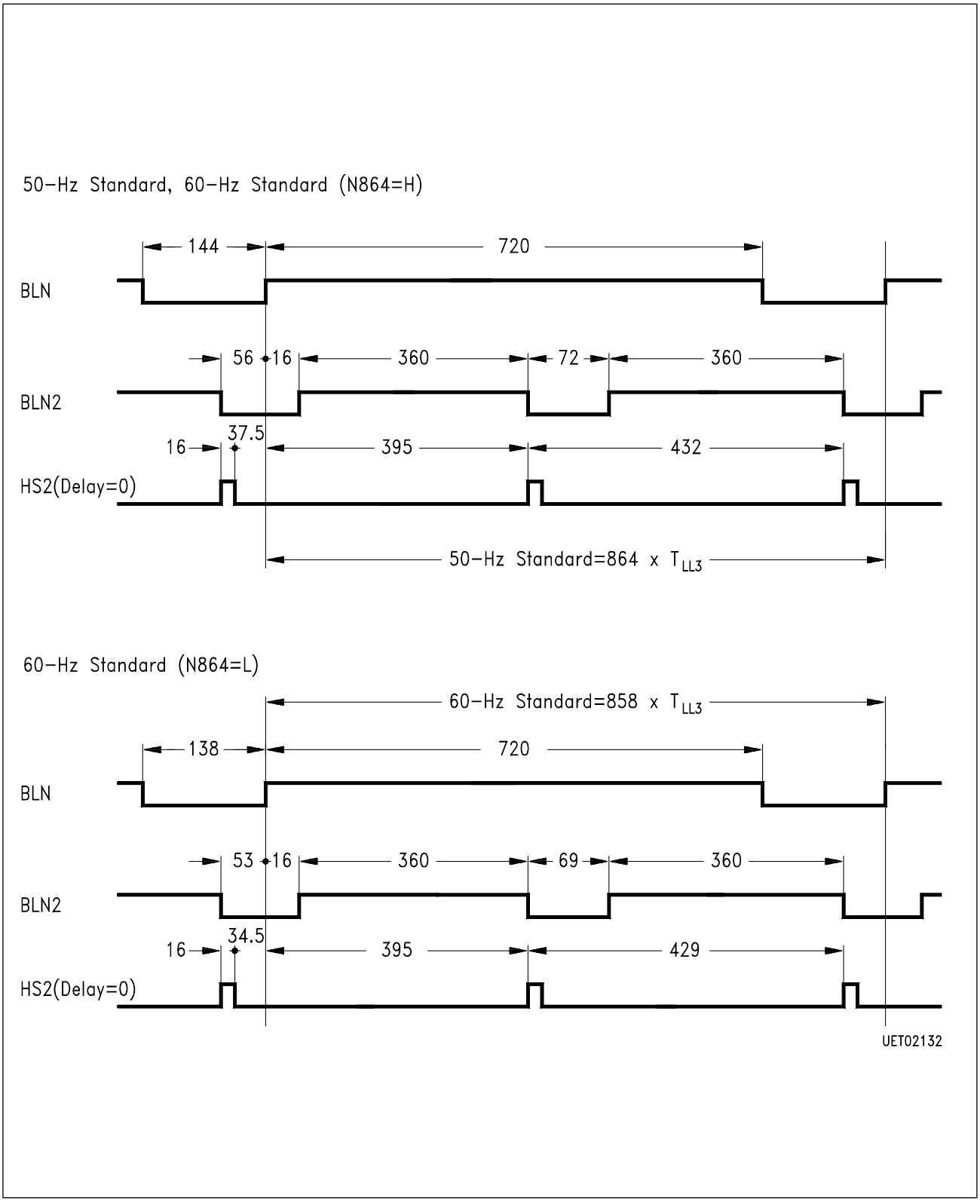


Figure 12
Timing Diagrams, Horizontal Sync Signals for Standard Conversion

Note: The figures indicate the number of LL3-clock periods

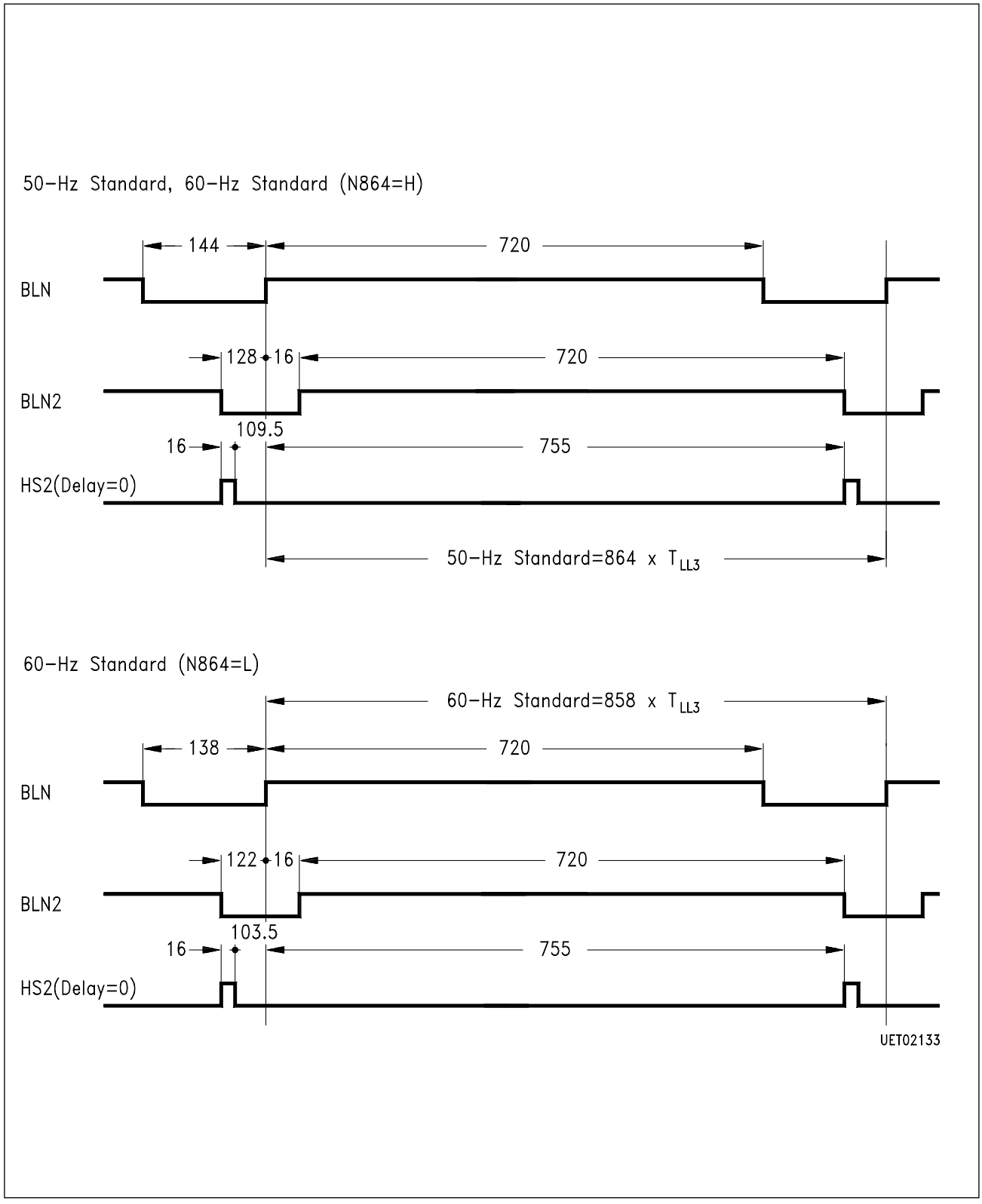


Figure 13
Timing Diagrams, Horizontal Sync Signals without Standard Conversion

Note: The figures indicate the number of LL3-clock periods

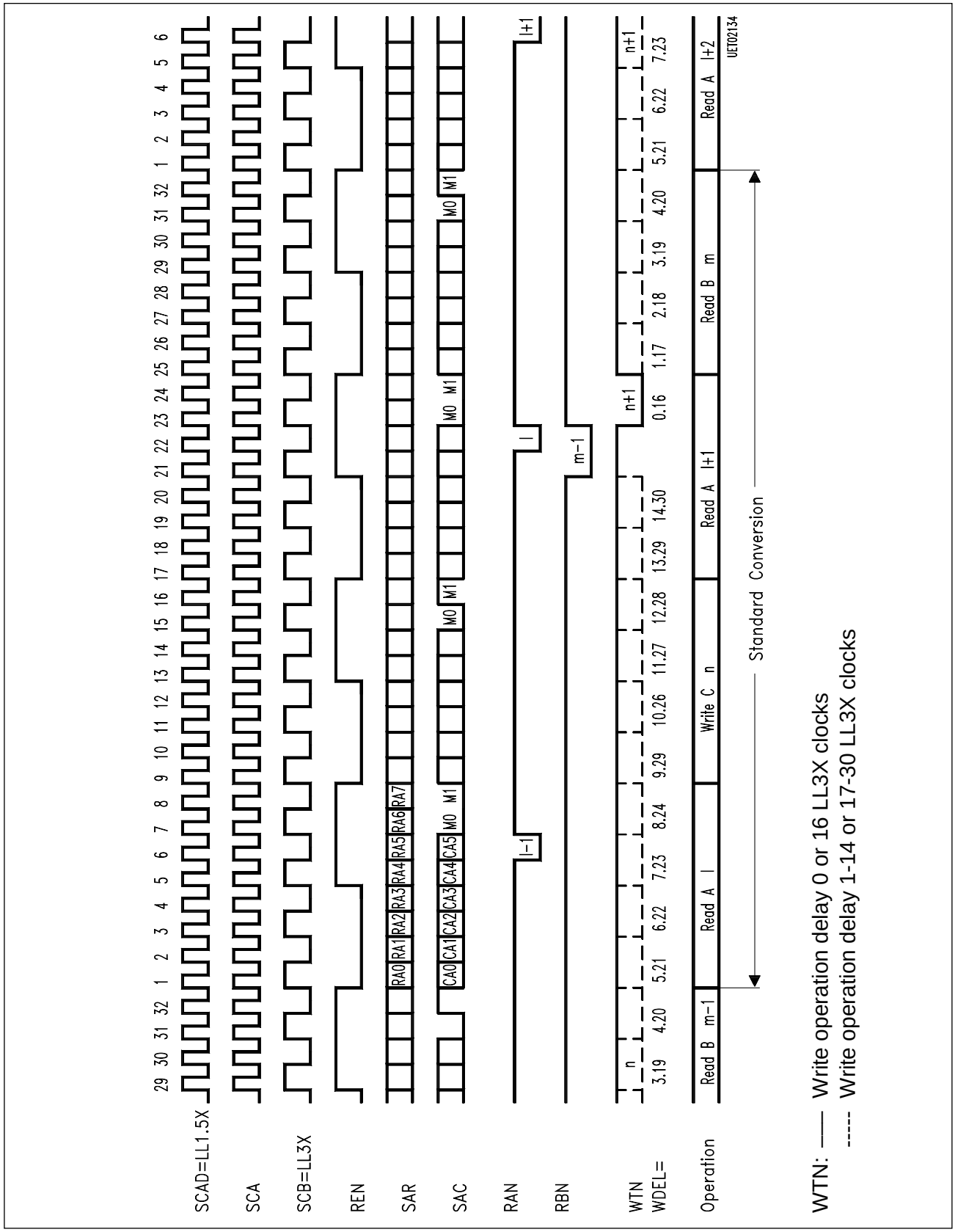


Figure 14
Memory Basic Cycle for Normal Mode with Standard Conversion and 864 Pixels per Line

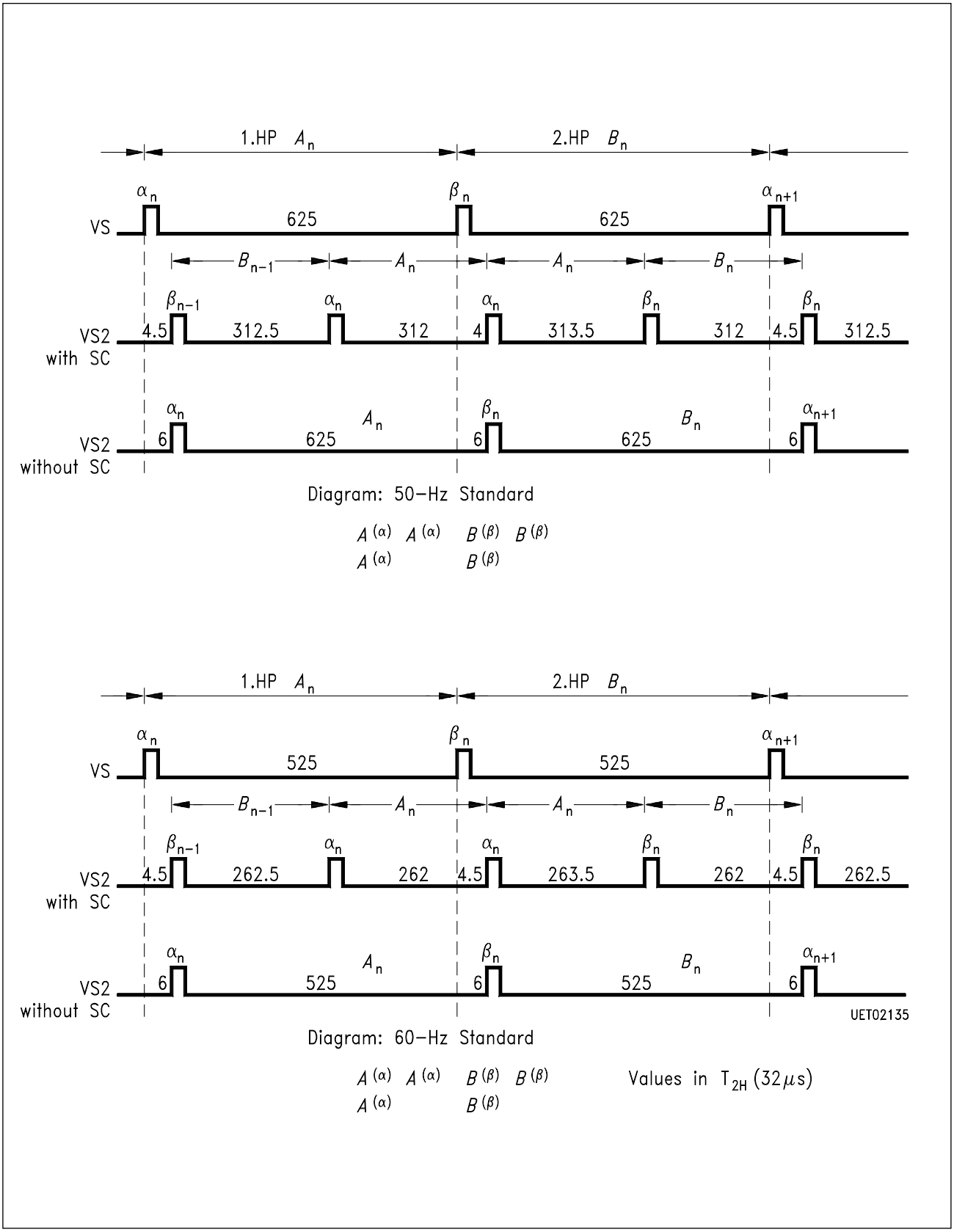

1.HP A_n
2.HP B_n
α_n
β_n
α_{n+1}
VS
625
625
B_{n-1}
A_n
A_n
B_n
β_{n-1}
α_n
α_n
β_n
β_n
VS2 with SC
4.5
312.5
312
4
313.5
312
4.5
312.5
α_n
A_n
β_n
B_n
α_{n+1}
VS2 without SC
6
625
6
625
6
Diagram: 50–Hz Standard
$A^{(\alpha)}$ $A^{(\alpha)}$ $B^{(\beta)}$ $B^{(\beta)}$
$A^{(\alpha)}$ $B^{(\beta)}$
1.HP A_n
2.HP B_n
α_n
β_n
α_{n+1}
VS
525
525
B_{n-1}
A_n
A_n
B_n
β_{n-1}
α_n
α_n
β_n
β_n
VS2 with SC
4.5
262.5
262
4.5
263.5
262
4.5
262.5
α_n
A_n
β_n
B_n
α_{n+1}
VS2 without SC
6
525
6
525
6
UET02135
Diagram: 60–Hz Standard
$A^{(\alpha)}$ $A^{(\alpha)}$ $B^{(\beta)}$ $B^{(\beta)}$
$A^{(\alpha)}$ $B^{(\beta)}$
Values in T_{2H} (32 µs)

Figure 15

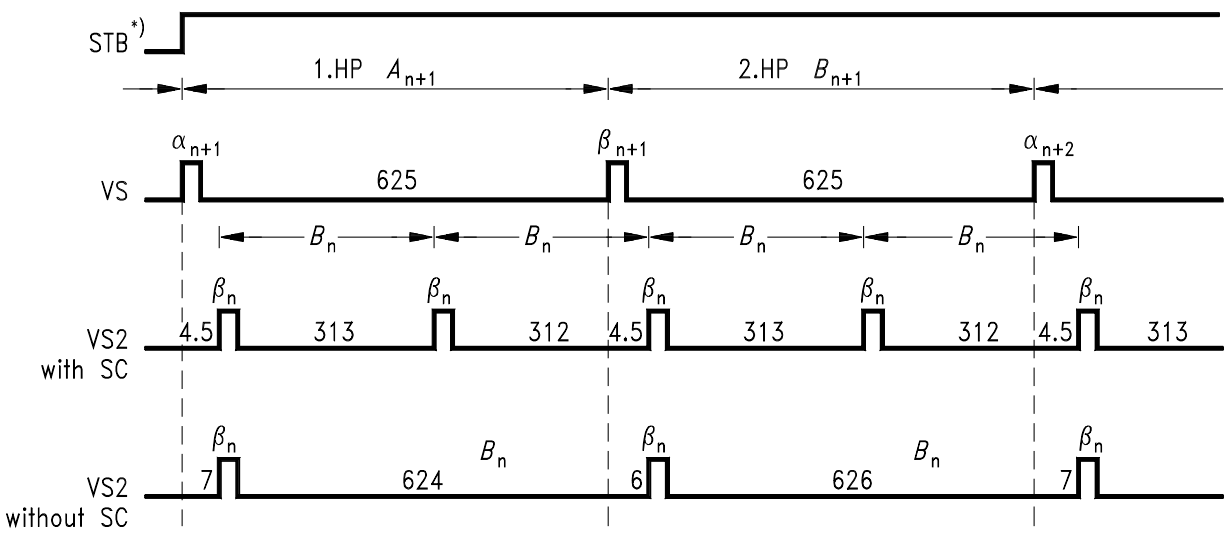


Diagram: 50–Hz Standard

$B^{(\beta)}$ $B^{(\beta)}$ $B^{(\beta)}$ $B^{(\beta)}$
$B^{(\beta)}$ $B^{(\beta)}$

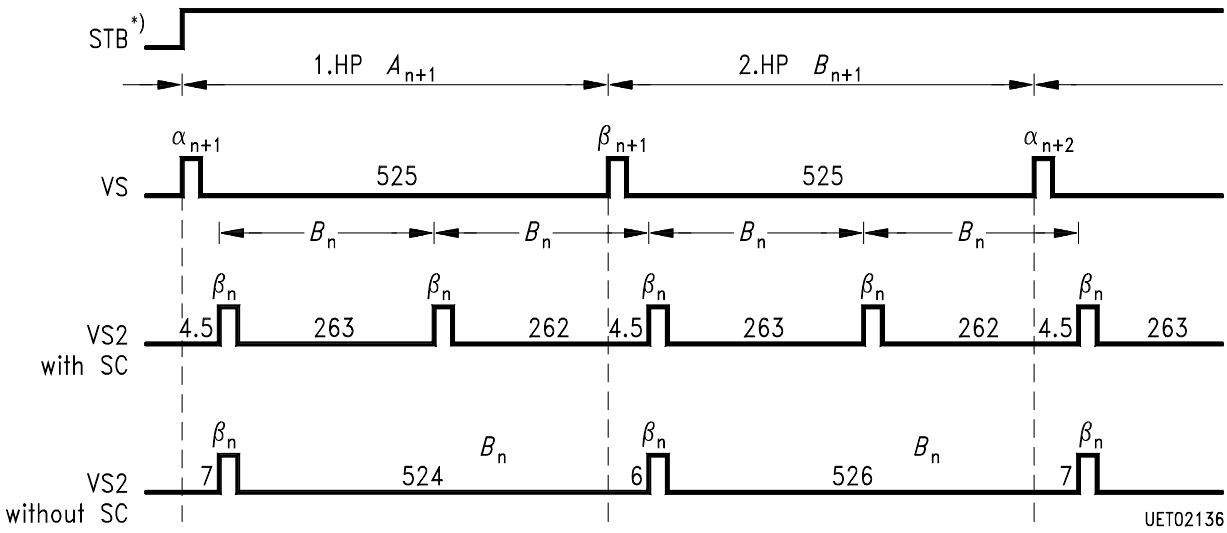


Diagram: 60–Hz Standard

$B^{(\beta)}$ $B^{(\beta)}$ $B^{(\beta)}$ $B^{(\beta)}$
$B^{(\beta)}$ $B^{(\beta)}$

Values in T_{2H} (32 μs)

*) Symbolized Interruption of Write Operation

Figure 16

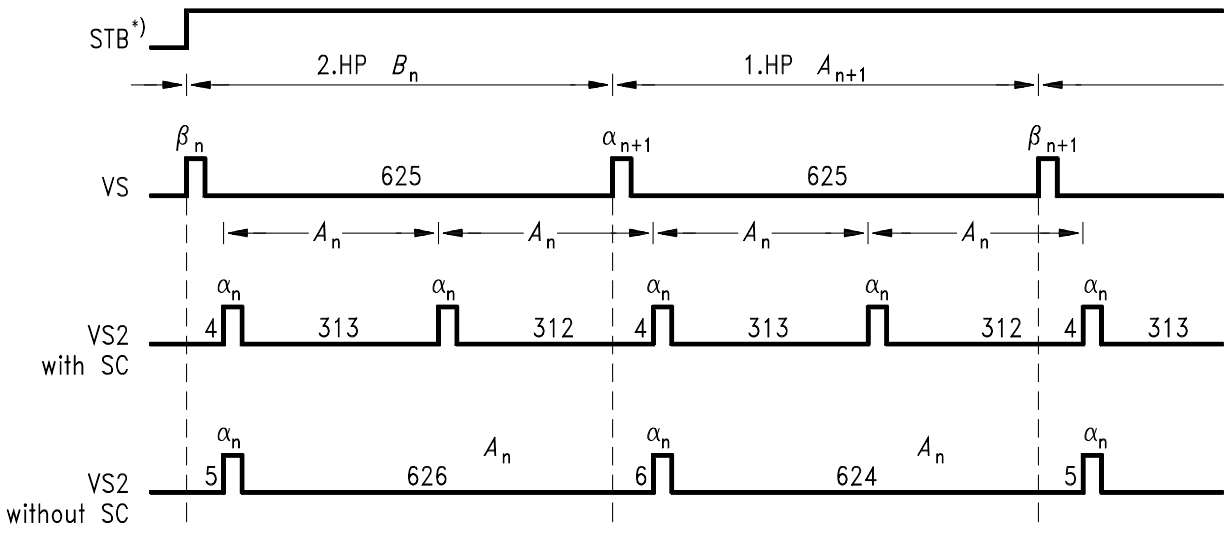


Diagram: 50–Hz Standard

$A^{(\alpha)}$ $A^{(\alpha)}$ $A^{(\alpha)}$ $A^{(\alpha)}$
$A^{(\alpha)}$ $A^{(\alpha)}$

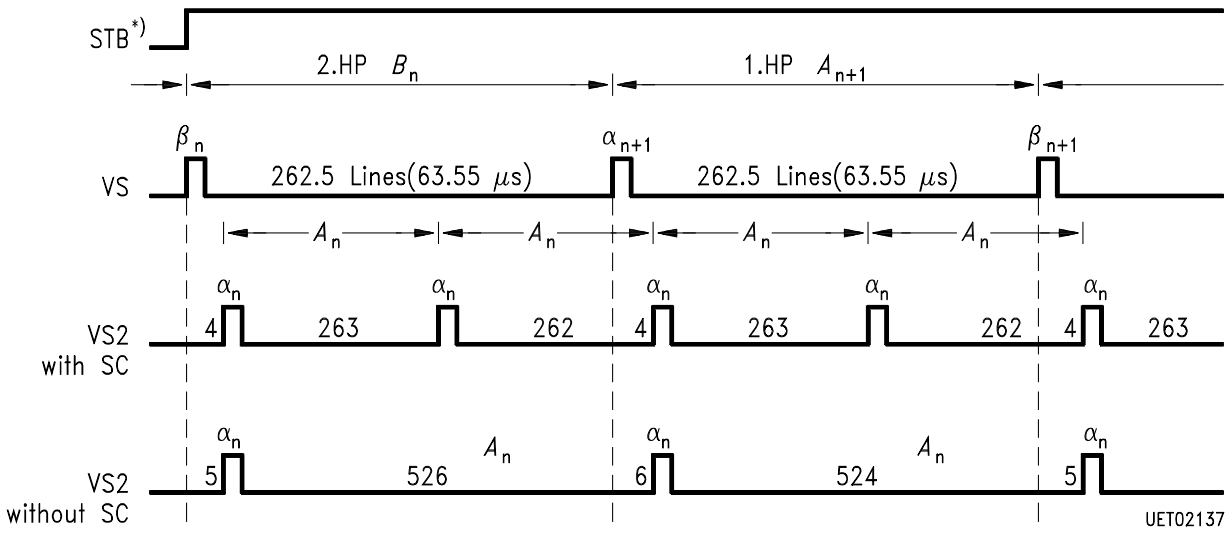


Diagram: 60–Hz Standard

$A^{(\alpha)}$ $A^{(\alpha)}$ $A^{(\alpha)}$ $A^{(\alpha)}$ Values in T_{2H} (32μs)
$A^{(\alpha)}$ $A^{(\alpha)}$

*) Symbolized Interruption of Write Operation

Figure 17

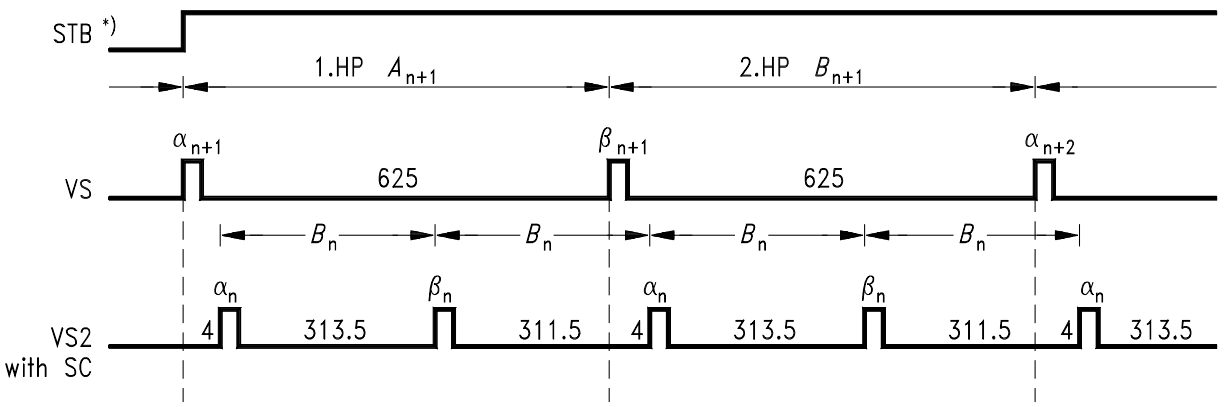


Diagram: 50–Hz Standard

$B^{(\alpha)}$ $B^{(\beta)}$ $B^{(\alpha)}$ $B^{(\beta)}$

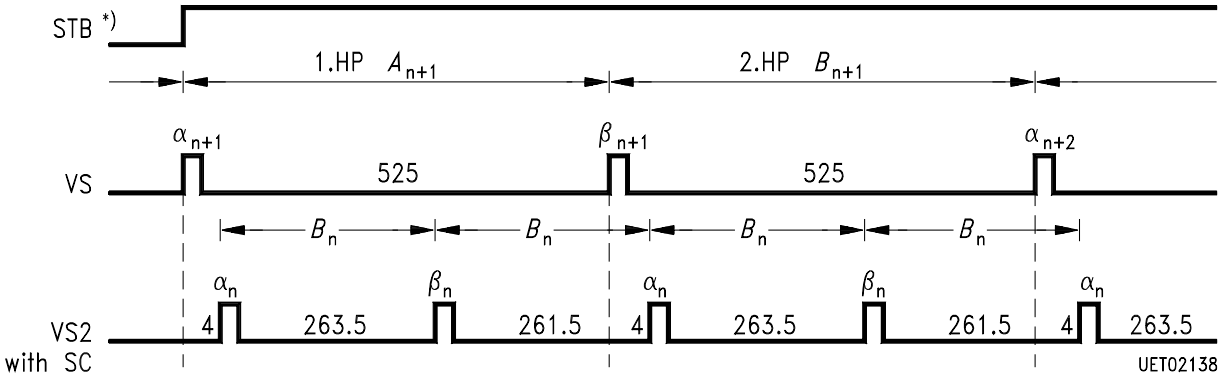


Diagram: 60–Hz Standard

$B^{(\alpha)}$ $B^{(\beta)}$ $B^{(\alpha)}$ $B^{(\beta)}$ Values in T_{2H} (32 μs)

*) Symbolized Interruption of Write Operation

Figure 18

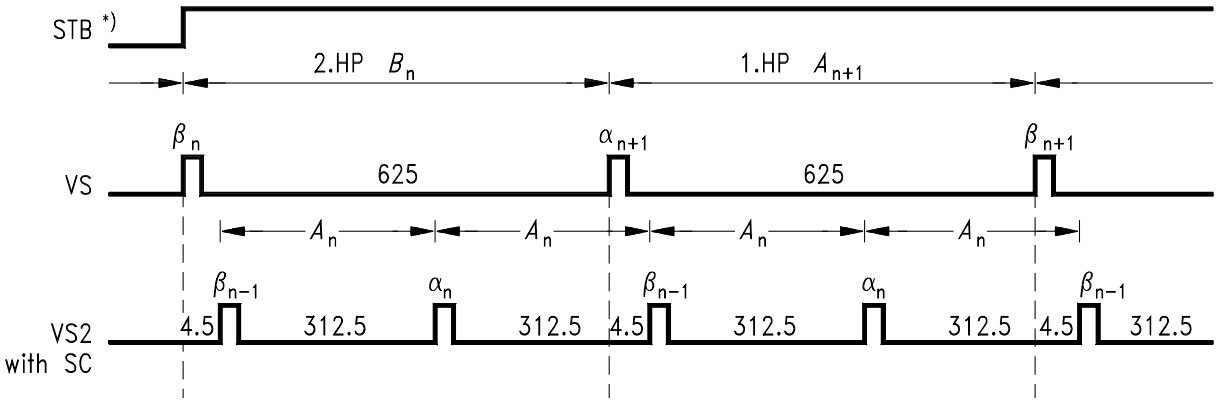


Diagram: 50–Hz Standard

$A^{(\alpha)}$ $A^{(\beta)}$ $A^{(\alpha)}$ $A^{(\beta)}$

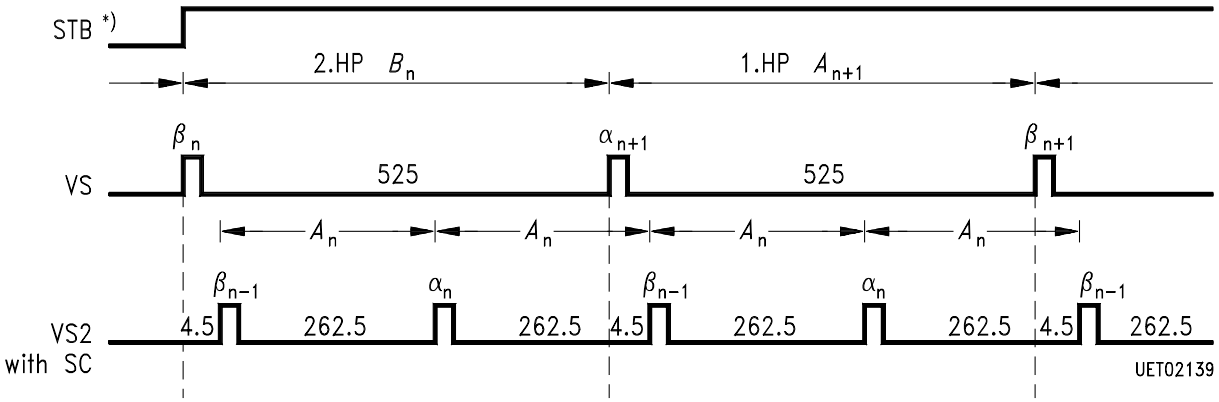


Diagram: 60–Hz Standard

$A^{(\alpha)}$ $A^{(\beta)}$ $A^{(\alpha)}$ $A^{(\beta)}$ Values in T_{2H} (32 μs)

*) Symbolized Interruption of Write Operation

Figure 19

Operation with Standard Conversion

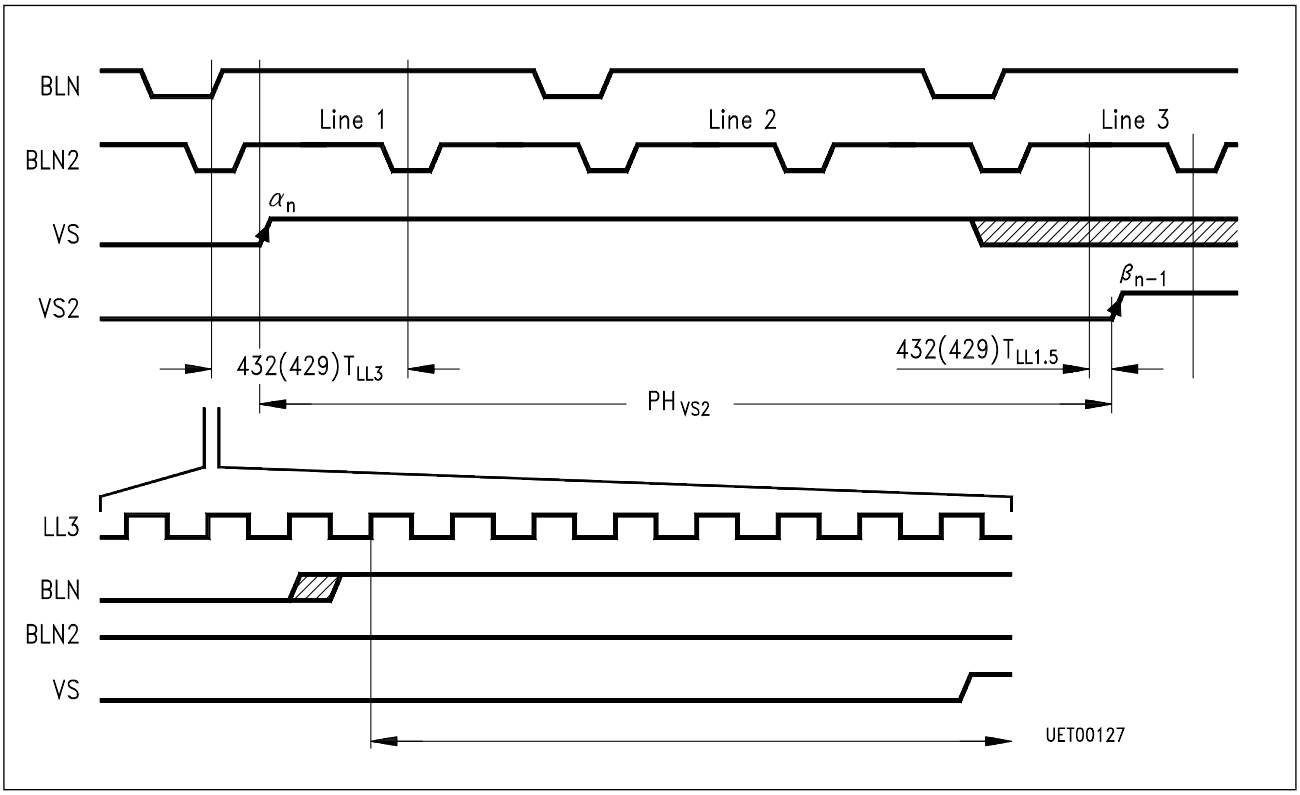


Figure 20a
VS/VS2 Phase Relation for Mode A(α) A(α) B(β) B(β) and VS Edge in First BLN-Half Cycle (VNR Bit = 1)

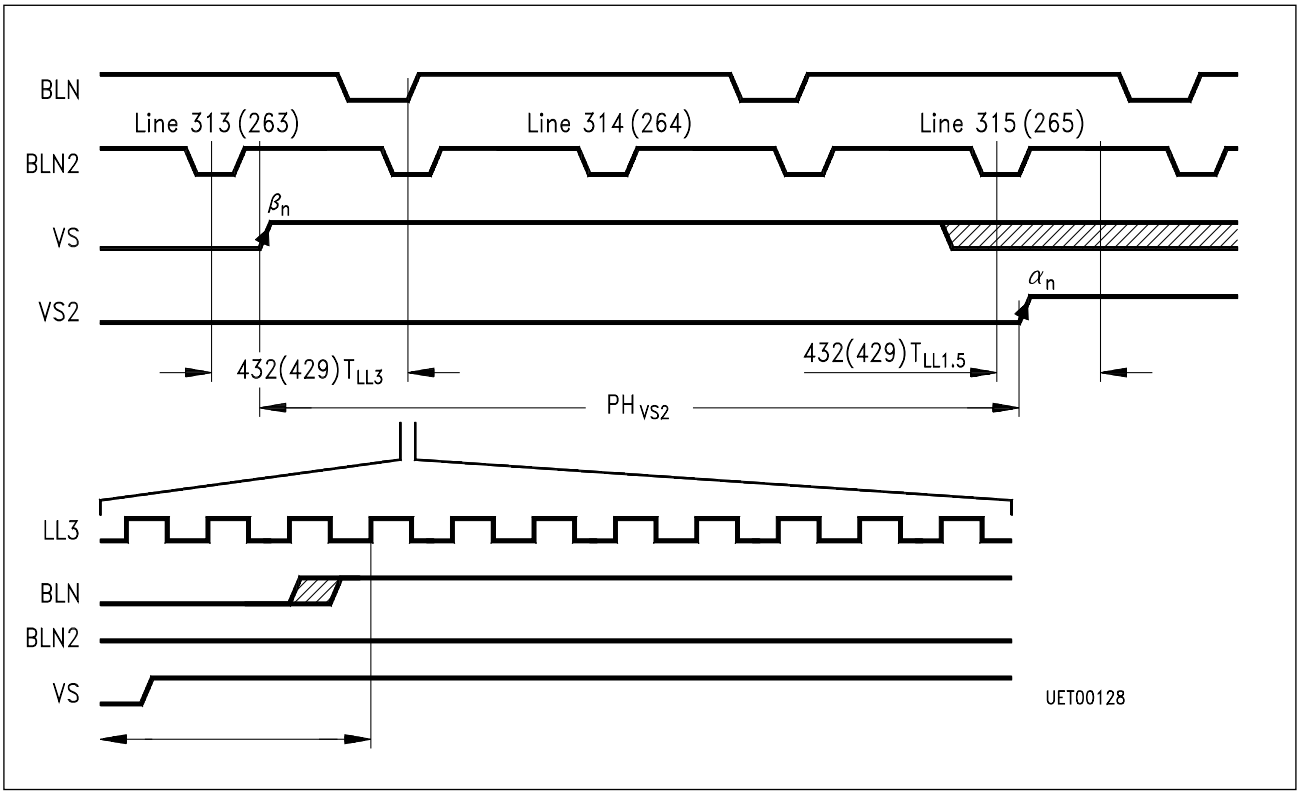


Figure 20b
VS/VS2 Phase Relation for Mode A(α) A(α) B(β) B(β) and VS Edge in Second BLN-Half Cycle (VNR Bit = 1)

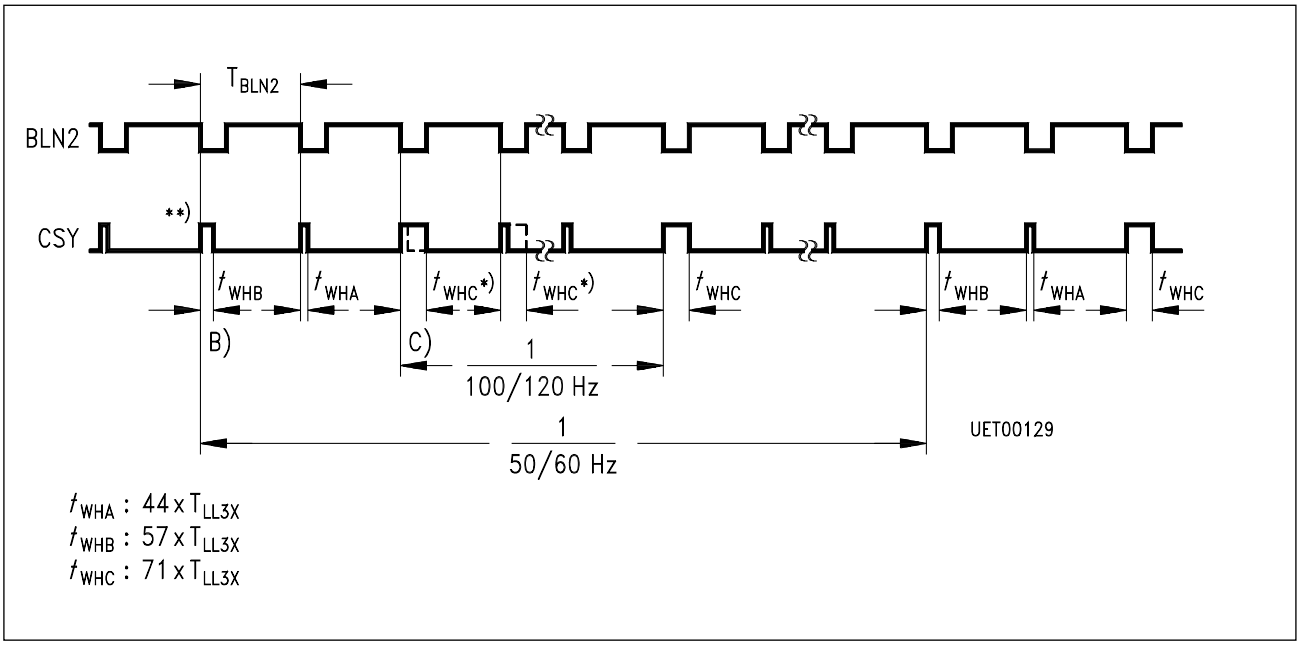


Figure 21
Timing Diagram, CSY-Pulse Sequency

B) Start of TV line 3 (1st field) or 316/266 (2nd field) before standard conversion (50/60 Hz)
C) Start of TV line 3 of each field after standard conversion (100/120 Hz)
*) Alternative
**) Rising edge of CSY comes four LL3X cycles before falling edge of BLN2

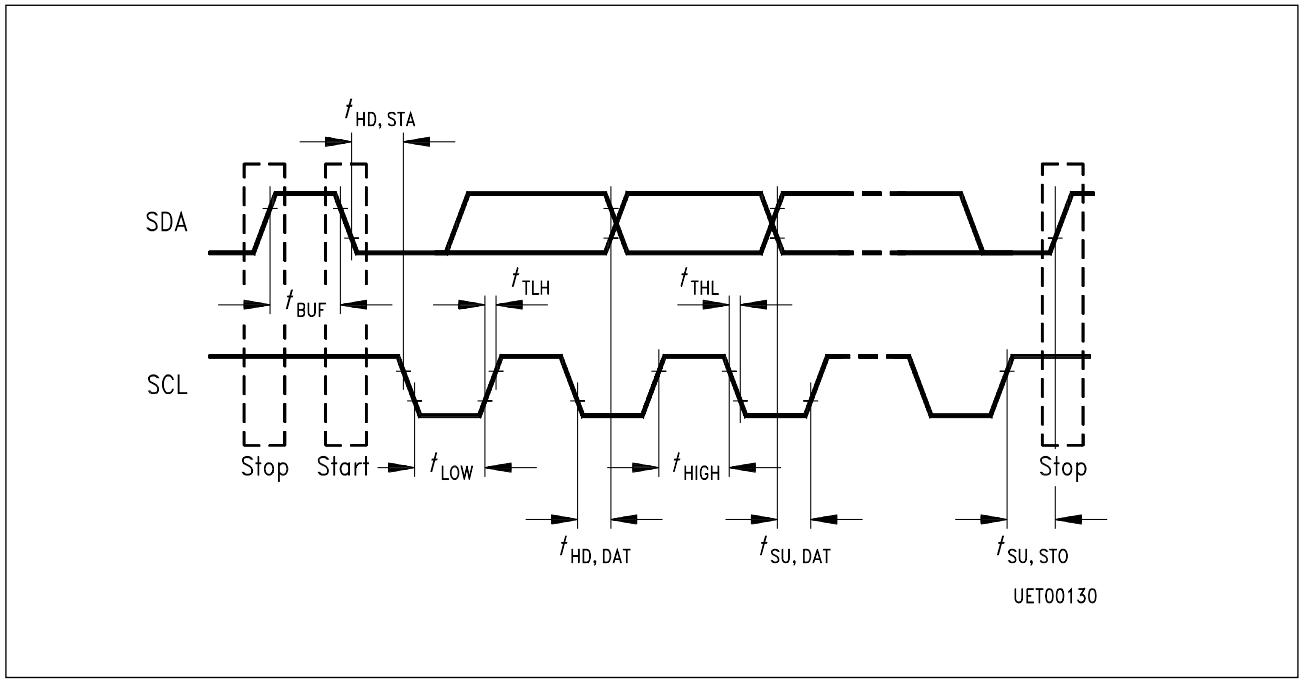


Figure 22
Timing for I²C Bus

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Clock frequency	f_{SCL}	0	100	kHz
Inactive time before start of new transmission	t_{BUF}	4.7		µs
Hold time for start condition (after this time first clock pulse is generated)	$t_{HD; STA}$	4.0		µs
Low clock phase	t_{LOW}	4.7		µs
High clock phase	t_{HIGH}	4.0		µs
Setup time for data	$t_{SU; DAT}$	250		ns
Rise time for SDA and SCL signals	t_{TLH}		1	µs
Fall time for SDA and SCL signals	t_{THL}		300	ns
Setup time for SCL clock in stop condition	$t_{SU; STO}$	4.7		µs

All values are referred to specified input levels V_{IH} and V_{IL}.