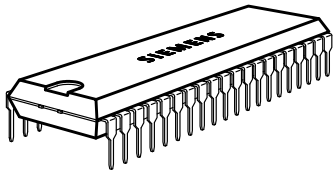
SIEMENS

Digital Deflection Controller SDA 9064-5

Preliminary Data **NMOS IC**

Features

- Pipeline processor structure controls deflection stages
- Raster alignment by keyboard or automatically
- Adaptable beam current compensation for picture height and width
- Protection input stops the exceeding
- For double the line frequency and 100-/120-Hz vertical frequency interlaced



P-DIP-40-1

Type	Ordering Code	Package
SDA 9064-5	Q67100-H8382	P-DIP-40-1

Circuit Description

The DDC consists essentially of a processor with program ROM and RAM, ports for input and output signals and a clock rate divider that supplies the whole chip with clock signals.

The processor is specially manufactured for the arithmetic operations performed in the DDC. It operates according to the pipeline principle on account of the high requirements involved with regard to time. It has two 16-bit accumulators. The 16-bit data bus and the 7-bit address bus take care of the data traffic between the processor and the ports. The size of the static RAM is 96 x 16 bits; the program ROM can store 800 16-bit instructions.

The V port and the Φ2 port comprise counters for coarse conversion and a chain of 32 resistors for amplitute quantization of fine conversion. The Φ2 port further measures the position of the ZR pulses with respect to time and transfers measured data to the processor. The east/west port similarly has a counter for digital time conversion but manages without fine conversion.

The 9-bit analog-to-digital converter works on the principle of successive approximation using a capacitance field.

The I^2C Bus interface makes it possible to read and modify deflection data in the RAM. The protective circuitry monitors inputs SS, ZR and HA2EN using comparators.

The start-up circuitry has its own power and clock pulse supply. It is therefore completely independent of the other DDC functions.

Description of the Signal and Data I/O of the Digital Deflection Controller

The digital deflection controller (DDC) generates horizontal-frequency, pulsewidth modulated control signals for external deflection output stages of color TV sets. The output signal for the horizontal deflection is phase-shifted, the signal for the east/west raster correction is parabolic and the signal for the vertical deflection is saw-tooth modulated. Signal computation is performed with data values from an internal memory that can be written by the I^2C Bus. DDC is synchronized by means of a horizontal and a vertical input signal.

The HA2 output generates the control signals for a conventional horizontal output stage.

The east/west output drives the diode modulator via a switched small-signal transistor.

After the integration of the output signal a linear amplifier can be connected to the output VA1 to drive the V-output stage.

The above-mentioned data values which determine the raster are stored (system-specific for 45 AX picture tubes) in an integrated ROM for 50-Hz and 60-Hz vertical deflection frequencies. However, individual alignment is possible as well. The data obtained is written into a nonvolatile memory of the operating processor. During switch-on, the data is transferred via the I^2C Bus to the deflection RAM in the DDC.

In addition, the variable storage time of the horizontal deflection stage transistor is compensated ($\Phi 2$ control loop), while the pulse duty factor of the driver-control signal remains constant. The horizontal deflection stage is switched off via a protective circuitry, when the voltage at input SS exceeds a given level.

The start-up circuitry supplies the horizontal deflection stage transistor with control signals in the standby mode, the switch-off phase, and during system clock failure.

The system includes a control loop with an analog-to-digital converter to stabilize the shape and amplitude of the vertical deflection current (V-feedback).

The input signals HS2 and VS2 are supplied with double the frequency from a TV-standard conversion circuitry.

The resolution enhancement filter of the VDA can be set via two outputs with the I^2C Bus interface of the deflection controller.

The DDC can be externally reset via a RESET input (with L level).

Deflection frequencies: 100/120-Hz field frequency, 31.25/31.5-kHz line frequency.

Figure 1 shows the block diagram with the interface.

Description of the Start-Up Circuitry

The horizontal start-up circuitry is provided with the supply voltage of the operating processor via pin $V_{DD\,S}$. This supply voltage is already present in the standby mode of the TV set, although the supply voltage for the horizontal driver and horizontal output stages is not yet available.

During standby mode, the HA2 output signal shape corresponds to the standard mode, however, without Φ2 function. The H-level duration is 14.5 µs and the period ranges between 31.6 and 32.55 µs, depending on the tolerance of the ceramic resonator (± 1 %).

After the main supply voltage V_{DD} has been switched on and the HA2 signals of the start-up circuitry have been correlated with the HA2 signals arriving from the DDC (Φ2 circuitry), the standard mode is selected within one frame period (max. shift is – 2.8 to + 2.55 µs including all tolerances), if the following requirements are met:

- The DDC supplies the start-up circuitry with HA2 signals satisfactory with respect to the period and H-level duration
- The ZR-pulse threshold is not exceeded at pin SS
- The supply voltage at the horizontal driver exceeds the minimal value (threshold at pin HA2EN, if connected).

The standby mode is selected immediately in response to a drop in the DDC-main supply voltage and concomitant max. phase shifts of – 2.65 to + 2.8 µs.

The maximum period duration of HA2 with reference to LH junctions may be 36 µs in the event of faults (e.g. failure of LL1.5, malfunctions in the DDC with the exception of the start-up circuitry.

The switch-off time constant of $V_{DD\,S}$ should be larger than that of V_{DD}, ensuring that the HA2 pulses are continuously supplied during a voltage glitch of V_{DD} and exceed the duration of the horizontal output stage voltage supply during switch-off.

During all operating modes, HA2 will be high for the duration of the ZR pulse.

I²C Bus Protocol

The DDC includes a I²C Bus port designed for the following functions:

- Slave receiver
- Slave transmitter

Since the DDC does not include a master function, data transfers are always initiated and controlled by an external bus master. The actual data transfer is executed by the processor of the DDC serving its I²C Bus port every 32 µs and receiving or transferring data in accordance with the operating mode set.

A maximum of 127 memory locations is available for read/write operations via the processor of the DDC.

During the slave-receiver mode, the DDC accepts data from the I²C Bus master.
A bus telegram transmitted in this mode is characterized by the following:

Slave Receiver

STA	Slave-Addr	W	Ack	RAM-Addr	Ack	Data-H	Ack	Data-L	Ack	STOP

During the slave-transmitter mode, data is transmitted from the DDC to the I²C Bus master with the I²C Bus master clock. The first data byte to be transmitted is always the status word.

A bus telegram transmitted in the slave-transmitter mode is characterized by the following:

Slave Transmitter

STA	Slave-Addr	R	Ack	Status	Ack	Data-H	Ack	Data-L	NA	STOP

STA = Start identification
R = Read/write bit = high
Ack = Acknowledge
STOP = Stop identification
W = Read/write bit = low
NA = No acknowledge

The slave address of the DDC is 1000110. The following information can be received by the slave receiver during this operating mode:

Sub-addresses 0A to 29:	32 bytes for raster alignment at 100 and 120 Hz
	vertical deflection frequency
Sub-addresses 2A and 2B:	2 control words with control bits for DDC and VDA

The following information can be queried by the DDC during the slave-transmitter mode:

- Status word whose bits identify the status of the DDC
- Fixed raster data from the ROM
- Raster alignment data from the internal RAM

Tables 1 to 4 list the sub-addresses, name and effect of the individual data. The raster size setting (e.g. east/west pin cushion with EP) usually influences other raster characteristics (e.g. picture width). This influence can be avoided by changing other data values accordingly; refer to networking list shown in **table 5.** The table lists the useful steps of the data values to be adjusted and the necessary adaptation of the other data (per step width) for non-iterative setting.

The adjustment program INFRARAST in conjunction with the microcontroller SDA 20160 as I^2C Bus master of the TV receiver provides for user-friendly setting via remote control.

When the supply voltage V_{DD} is not present, pins SCL and SDA are in high-impedance state.

When the clock LL1.5 is not present, the I^2C Bus port is without function and SCL and SDA are in high-impedance state.

When the supply voltage V_{DD} is switched on (after internal power ON reset), data can be transferred via the I^2C Bus port after approx. 32 µs.

Table 1
I²C Bus Data of the DDC

Sub-addresses	Data								Definition
	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	
0A	HP 5	HP 4	HP 3	HP 2	HP 1	HP 0	X	X	Horizontal picture position
0B	X	X	X	X	X	X	X	X	None
0C	VSC 55	VSC 54	VSC 53	VSC 52	VSC 51	VSC 50	X	X	Vertical S-correction during 100-Hz operating mode
0D	X	X	X	X	X	X	X	X	None
0E	VSC 65	VSC 64	VSC 63	VSC 62	VSC 61	VSC 60	X	X	Vertical S-correction during 120-Hz operating mode
0F	X	X	X	X	X	X	X	X	None
10	VF 63	VF 62	VF 61	VF 60	VF 511	VF 510	VF 509	VF 508	Vertical upper linearity; 120-Hz adjustment values VF 6x and 100-Hz absolute values VF 5xx; 120-Hz absolute value VF 6xx = VF 5xx + 16 · VF 6x
11	VF 507	VF 506	VF 505	VF 504	VF 503	VF 502	VF 501	VF 500	
12	VC 3	VC 2	VC 1	VC 0	VS 511	VS 510	VS 509	VS 508	Picture height compensation VC for evaluating the beam current information ISTR and vertical picture position VS
13	VS 507	VS 506	VS 505	VS 504	VS 503	VS 502	VS 501	VS 500	
14	HC 3	HC 2	HC 1	HC 0	PH 511	PH 510	PH 509	PH 508	Picture width compensation HC for evaluating the beam current information ISTR and picture height PH
15	PH 507	PH 506	PH 505	PH 504	PH 503	PH 502	PH 501	PH 500	
16	VL 515	VL 514	VL 513	VL 512	VL 511	VL 510	VL 509	VL 508	Vertical linearity during 100-Hz operating mode
17	VL 507	VL 506	VL 505	VL 504	VL 503	VL 502	VL 501	VL 500	
18	EWC 55	EWC 54	EWC 53	EWC 52	EWC 51	EWC 50	PW 59	PW 58	East/west raster correction in the corners at 100-Hz operating mode EWC and picture width at 100-Hz operating mode PW
19	PW 57	PW 56	PW 55	PW 54	PW 53	PW 52	PW 51	PW 50	

Table 1
I²C Bus Data of the DDC (cont'd)

Sub-addresses	Data								Definition
	D 7	**D 6**	**D 5**	**D 4**	**D 3**	**D 2**	**D 1**	**D 0**	
1A	EP 515	EP 514	EP 513	EP 512	EP 511	EP 510	EP 509	EP 508	East/west parabola during 100-Hz operating mode
1B	EP 507	EP 506	EP 505	EP 504	EP 503	EP 502	EP 501	EP 500	
1C	TR 515	TR 514	TR 513	TR 512	TR 511	TR 510	TR 509	TR 508	East/west trapezoidal correction during 100-Hz operating mode
1D	TR 507	TR 506	TR 505	TR 504	TR 503	TR 502	TR 501	TR 500	
1E	X	X	X	X	VS 611	VS 610	VS 609	VS 608	Vertical picture position during 120-Hz operating mode
1F	VS 607	VS 606	VS 605	VS 604	VS 603	VS 602	VS 601	VS 600	
20	EHTH 3	EHTH 2	EHTH 1	EHTH 0	PH 611	PH 610	PH 609	PH 608	Dynamic picture width compensation EHTH for evaluating the beam current information ISTR and picture height during 120-Hz operating mode PH
21	PH 607	PH 606	PH 605	PH 604	PG 603	PH 602	PH 601	PH 600	
22	VL 615	VL 614	VL 613	VL 612	VL 611	VL 610	VL 609	VL 608	Vertical linearity during 120-Hz operating mode
23	VL 607	VL 606	VL 605	VL 604	VL 603	VL 602	VL 601	VL 600	
24	EWC 65	EWC 64	EWC 63	EWC 62	EWC 61	EWC 60	PW 69	PW 68	East/west raster correction in the corners during 120-Hz operating mode EWC and picture width during 120-Hz operating mode PW
25	PW 67	PW 66	PW 65	PW 64	PW 63	PW 62	PW 61	PW 60	
26	EP 615	EP 614	EP 613	EP 612	EP 611	EP 610	EP 609	EP 608	East/west parabola during 120-Hz operating mode
27	EP 607	EP 606	EP 605	EP 604	EP 603	EP 602	EP 601	EP 600	
28	TR 615	TR 614	TR 613	TR 612	TR 611	TR 610	TR 609	TR 608	East/west trapezoidal correction during 100-Hz operating mode
29	TR 607	TR 606	TR 605	TR 604	TR 603	TR 602	TR 601	TR 600	
2A	X	X	X	X	X	X	I²C1	I²C0	Control word 1, control bits for outputs I²C0 … 1
2B	X	X	EFS	FS	RAM	X	X	X	Control word 2, **refer to table 2**
C4-CB	X	X	X	X	X	X	X	X	These adresses are reserved for test operation and must not be used
CC-CD	X	X	X	X	X	X	X	X	Switch back to normal operating mode
	PONRES	HOFF	X	X	X	X	X	FD	Status word, **refer to table 3**

Table 2
Control Word 2

	0	1
EFS	100/120-Hz operating mode	
	dedicted by the DDC	determined by the FS bit
FS	100-Hz operating mode	120-Hz operating mode
RAM	DDC uses fixed raster data	
	from the internal ROM	from the internal RAM

Table 3
Status Word 2

	0	1
PONRES	Status word is read	
	after reset of bus master	after each DDC reset
FD	DDC recognized 100 Hz	120 Hz recognized
HOFF	Standard HA2 function	HA2 set “high” by protective circuitry

Table 4
Effect of the Raster Alignment Data

Sub-addresses	Data Value	Range (in decimals)	Effect
0A	HP 5 … HP 0	– 32 … + 31	Picture to the right … to the left
0C	VSC 55 … VSC 50	– 32 … + 31	S-correction max. neg. … max. positive
0E	VSC 65 … VSC 60	– 32 … + 31	S-correction max. neg. … max. positive
10	VF 63 … VF 60	– 8 … + 7	Line spacing small on top … large on top (**refer to table 1**)
10 and 11	VF 511 … VF 500	2400 … 3600	Line spacing small on top … large on top (**refer to table 1**)
12	VC 3 … VC 0	– 8 … 0	V-deflection current decreases considerably/ does not decrease when increasing beam current
12 and 13	VS 511 … VS 500	2600 … 3400	Picture position bottom … top
14	HC 3 … HC 0	– 8 … 0	H-deflection current decreasing considerably/ does not decrease when increasing beam current
14 and 15	PH 511 … PH 500	1450 … 2150	Picture height min. … max.
16 and 17	VL 515 … VL 500	– 32768 … + 32767	Line spacing bottom > top … top > bottom
18	EWC 55 … EWC 50	– 32 … + 31	Vertical lines in the corners facing max. outward … max. inward
18 and 19	PW 59 … PW 50	0 … 1023	Picture width max. … min., PW must be > 0, when HC is to be effective
1A and 1B	EP 515 … EP 500	– 32768 … … + 32767	East-West raster max. concave … max. convex
1C and 1D	TR 515 … TR 500	– 32768 … 0	Picture wider … narrower on bottom
1E and 1F	VS 611 … VS 600	2600 … 3400	Picture position bottom … top
20	EHTH 3 … EHTH 0	– 8 … 0	Considerable … no reduction in H-deflection current with white H stripe
20 and 21	PH 611 … PH 600	1450 … 2150	Picture height min. … max.
22 and 23	VL 615 … VL 600	– 32768 … + 32767	Line spacing bottom > top … top > bottom
24	EWC 65 … EWC 60	– 32 … + 31	Vertical lines in the corners facing max. outward … max. inward
24 and 25	PW 69 … PW 60	0 … 1023	Picture width max. … min., PW must be > 0, HC is to be effective

Table 4
Effect of the Raster Alignment Data (cont'd)

Sub-addresses	Data Value	Range (in decimals)	Effect
26 and 27	EP 615 … EP 600	– 32768 … … + 32767	East-West raster max. concave … convex
28 and 29	TR 615 … TR 600	– 32768 … 0	Picture wider … narrower on bottom

Networking Lists

Table 5.1
East/West Data 100 Hz

Setting:	Changes:	EWC 5	EP 5	TR 5	PW 5
(increase) picture width		–	–	–	– 2
Trapezoidal correction (smaller at the bottom)		–	–	102	– 4
(Magnify) parabola		–	260	– 634	12
Corners (facing inward)		1	760	– 618	6

Table 5.2
East/West Data 120 Hz

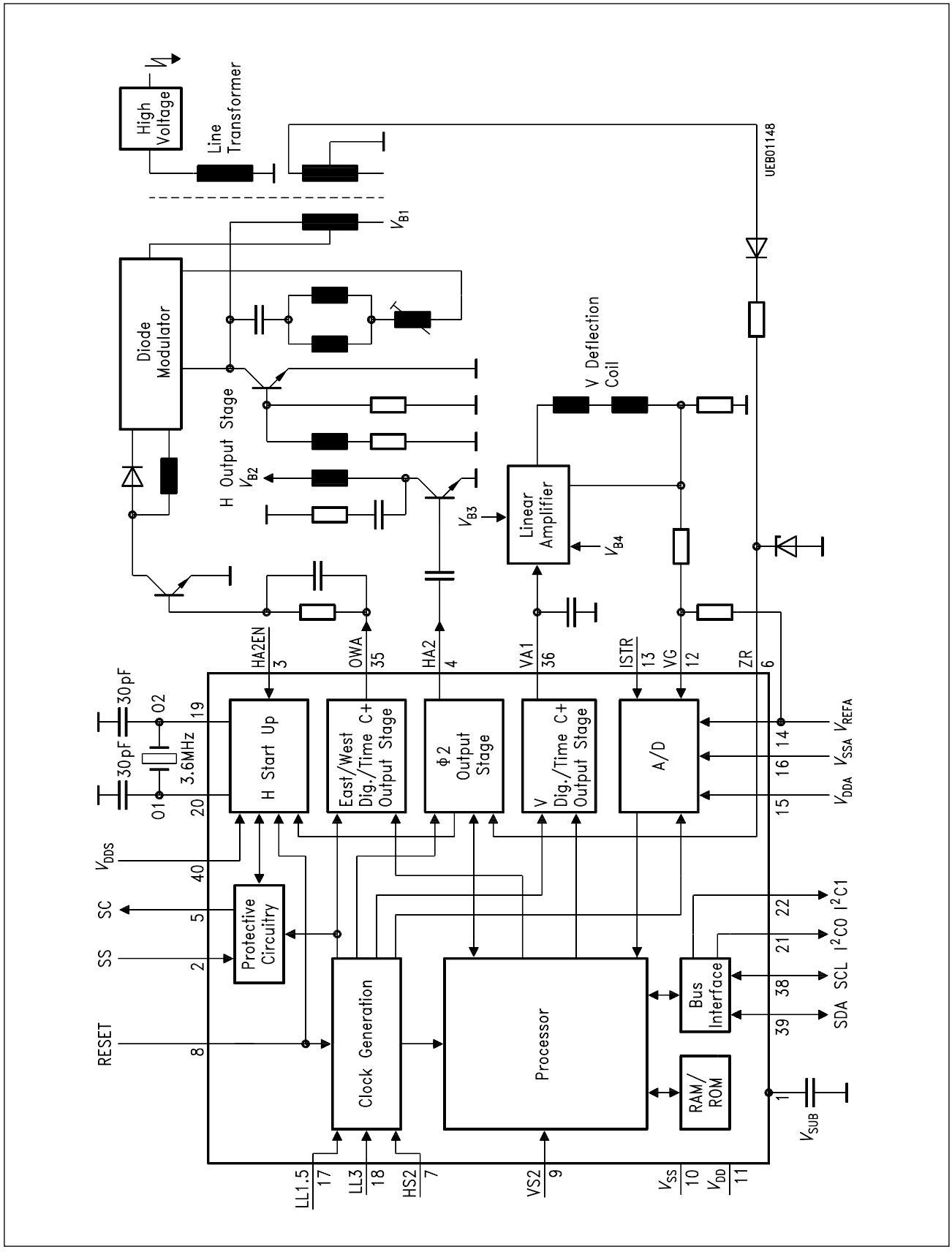
Setting:	Changes:	EWC 6	EP 6	TR 6	VF 6 PW 6
(increase) picture width		–	–	–	– 2
Trapezoidal correction (smaller at the bottom)		–	–	125	– 4
(magnify) parabola		–	382	– 782	12
Corners (facing inward)		2	1073	– 732	6

Table 5.3
Vertical Data 100 Hz

Setting:	Changes:	VSC 5	VL 5	PH 5	VF 5	VS 5
Picture position (to the top)		–	–	–	–	16
(Magnify) picture height		–	–	8	12	–
Linearity (top > bottom)		–	64	–	12	– 26
(Magnify) S-correction		1	– 283	19	11	–

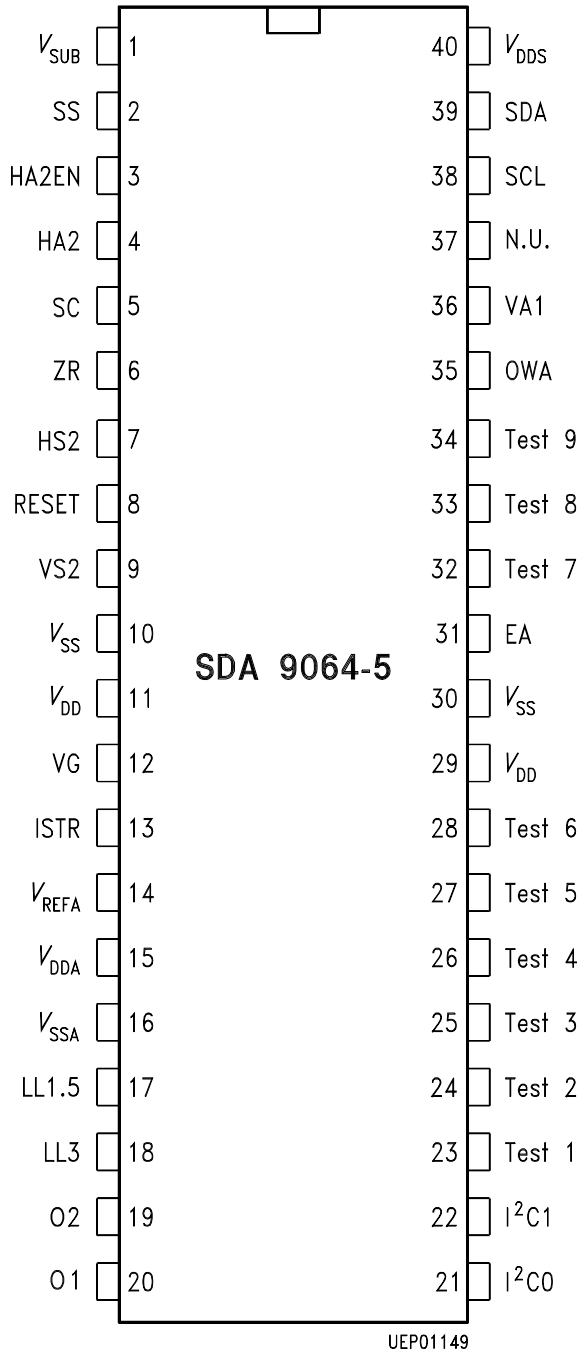
Table 5.4
Vertical Data 120 Hz

Setting:	Changes:	VSC 6	VL 6	PH 6	VF 6 PW 6	VS 6
Picture position (to the top)		–	–	–	–	16
(Magnify) picture height		–	–	8	12/16	–
Linearity (top > bottom)		–	93	–	12/16	– 26
(Magnify) S-correction		2	– 475	19	11/16	–



Block Diagram

Pin Configuration
(top view)



Pin Definitions and Functions

Pin	Symbol	Function	Description
1	V_{SUB}	Substrate voltage	Substrate voltage pin to connect an external smoothing capacitor for the internally generated substrate voltage.
2	SS	Protective circuitry	The protective circuitry switches off the horizontal output stage and blanks the picture tube. Usually a signal derived from the line flyback is injected at SS. If the input signal exceeds a given upper level, the blanking mode is enabled (sandcastle pulse with $V_{OH\,1}$ level) and the output HA2 goes to high. If the input signal falls below a given lower level at SS, only the blanking mode is enabled. After the protective circuitry responds via $V_{IH\,1}$, POR should be enabled (switch ON/OFF of $V_{DD\,S}$).
3	HA2EN		Enable/disable of HA2 pulse.
4	HA2	Output horizontal driver	The L/H transition initiates the line retrace. The output stage transistor transfer delay is compensated (Φ_2). The pulse duty factor is kept constant. During all operating modes, HA2 is high for the duration of the ZR signal.
5	SC	Sandcastle	The combined key pulse SC is generated from the horizontal and vertical flyback and the burst. The pulse can be switched to continuous blanking with the protective circuitry. The pulse is a two-level pulse.
6	ZR	Line retrace input	The signal voltage for this input is derived from the horizontal deflection stage. The behavior of the signal voltage corresponds to the voltage at the horizontal deflection coil. The control signal for the horizontal deflection stage (HA2) is controlled in such a manner that the input signal ZR arrives at a certain location in the blanking period of the CVBS signal.
7	HS2	Horizontal synchronous pulse	The HS2 pulse is supplied by the TV-standard conversion circuitry and is used as line reference signal.

Pin Definitions and Functions (cont'd)

Pin	Symbol	Function	Description
8	RESET	Input for external reset signal	The external RESET as well as power-on reset are effective in the following sections: start-up circuitry, clock divider, processor, program ROM, Φ_2 circuitry, A/D converter. The IC goes into the 100-Hz mode and into the ROM mode of the deflection data. (The ROM mode is retained until the RAM mode is selected via the bus interface). The blanking mode is enabled via output SC. The start-up circuitry goes into the standby mode when V_{DDS} is switched on or during external RESET. The HA2 pulses are present during an external RESET. The RAM and the OW port are not reset. The external RESET does not affect the I^2C Bus port, since the port is brought into a defined state each time it is addressed via the I^2C Bus interface. However, the POR bit is set in the status word. The REF outputs are not influenced by external RESET.
9	VS2	Vertical synchronous pulse	The input VS2 is supplied by a pulse from the TV-standard conversion circuitry, which is used as picture reference signal.
10	V_{SS}		Ground potential
11	V_{DD}		Positive supply voltage
12	VG	Vertical feedback input	The voltage drop at the feedback resistor which is proportional to the current flowing through the vertical deflection coils is used as input signal. The vertical current is adjusted to a given nominal value with this signal. Continuous blanking will be enabled via the output SC when the vertical saw-tooth current is missing.
13	ISTR	Input/beam current of picture tube	The voltage signal proportional to the beam current is used as input signal for the following purpose: By means of beam currents differing in value (change in image brightness), the high voltage is varied and thus also the deflection angle of the beam which determines the modulation of the picture width and height.
14	V_{REFA}		Reference voltage for A/D converter
15	V_{DDA}		Supply voltage for A/D converter
16	V_{SSA}		Ground potential for A/D converter
17	LL1.5		27-MHz system clock
18	LL3		13.5-MHz-clock signal from CGC
19	O2		Oscillator output for start-up circuitry
20	O1		Oscillator input for start-up circuitry

Pin Definitions and Functions (cont'd)

Pin	Symbol	Function	Description
21 22	I^2C0 I^2C1		General purpose output ports controlled by I^2C Bus
23 24 25 26 27 28	Test 1 Test 2 Test 3 Test 4 Test 5 Test 6	Test	Do not connect pins
29	V_{DD}		Positive supply voltage
30	V_{SS}		Ground potential
31 32 33	Test 7 Test 8 Test 9	Test	Do not connect pins
34	N.C.		Not connected
35	OWA	Output east/west raster correction	The course of the pulse duration of the PDM signal over the picture period is that of a parabola. The course of the pulse duration is established primarily by the programmed deflection data.
36	VA1	Vertical deflection 1	The saw-tooth signal required by the analog vertical output stage is generated in a digital time converter which effects the conversion of a binary data word into a pulse duty factor. An increase of resolution by the factor of 32 is effected by amplitute quantization during the rising edge of the PDM signal within a clock period ($1/f_T$). By connecting an external capacitor, the saw-tooth voltage for the vertical output stage is generated.
37	N.U.	not used	Do not connect pin
38 39	SCL SDA	I^2C Bus interface	The data traffic between SDA 9064-5 and its environment is processed on the basis of the I^2C Bus standard via a 2-wire interface. The interface of the SDA 9064-5 has been designed only for the slave function. The SDA 9064-5 can be addressed as transmitter or receiver. A message transmitted via the I^2C Bus is defined by a start and a stop identification. The actual message comprises one or several telegrams which can be separated by repeating the start condition. A telegram consists of data with a 2-byte organization, an address byte, and a status byte.
40	$V_{DD\,S}$		Standby supply voltage

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input voltage	V_{IM}	– 0.5	6.0	V
Supply voltage	V_{DD}	– 0.3	6.0	V
Substrate voltage	V_{SUB}	– 3.2	0	V
Total power dissipation	P_{tot}		1.7	W
Ambient temperature range	T_A	0	70	°C
Storage temperature range	T_{stg}	– 55	125	°C
Thermal resistance system-air	$R_{th\ SA}$		36	K/W

Characteristics

T_A = 25 °C (all voltages are referred to V_{SS})

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_{DD} [4]	4.5	5.5 300	V mA
Standby supply voltage for start-up circuitry	V_{DDS} [1]	4.5	5.5 15	V mA
Supply voltage for A/D converter	V_{DDA} I_{DDA}	4.5	5.5 1.5	V mA
Ripple against V_{SSA}			0.5	mV
Substrate voltage at pin for connecting an external smoothing capacitor	V_{SUB} [2]	– 3	– 2 100	V µA
Ripple against V_{SSA}			50	mV
Ambient temperature range	T_A	0	70	°C
Input currents				
Pin 3, 6, 8, 17, 20, 38, 39	I_{IH}		10	µA
Pin 7, 9, 12, 13, 18	I_{IH}		100	µA
Pin 2	I_{IH}	100	1000	µA
Pin 6, 17, 20, 38, 39	I_{IL}	– 10		µA
Pin 2, 3, 8, 12, 13	I_{IL}	– 100		µA
Pin 7, 9, 18	I_{IL}	– 1000	– 10	µA

[1] The voltage must have reached the required operating level prior to connecting the supply voltages for V_{DD} and the H-output stage. In addition, the voltage must glitch-free and switched off only after the H-supply voltage has been deactivated.

[2] Internally generated, however, can also be connected externally.

[3] The I_{DDS} feedback current flows across pin 10.

[4] V_{DD} must be switched on and off without contact chatter.

Characteristics (cont'd)

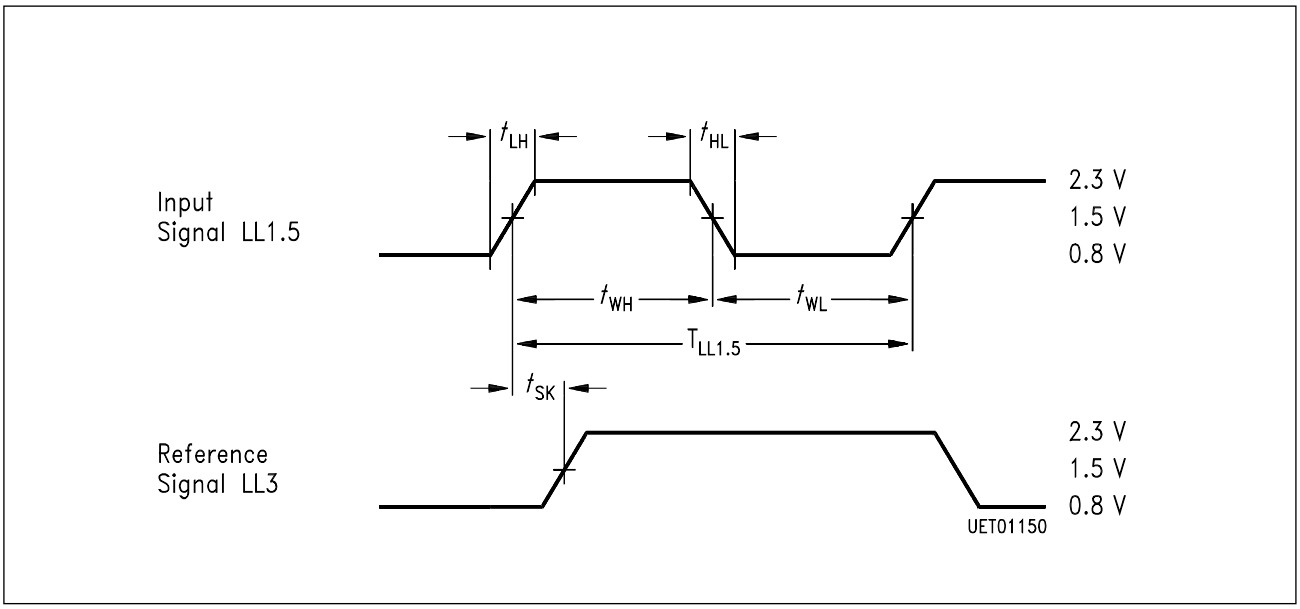
T_A = 25 °C; V_{DD} = 5 V (all voltages are referred to V_{SS})

Parameter	Symbol	Limit Values			Unit	Test Circuit
		min.	typ.	max.		
Input Signals: LL1.5 100-Hz (120-Hz) Field PAL (NTSC); TTL Input						
H-input voltage	V_{IH}	2.3		V_{DD}	V	*
L-input voltage	V_{IL}	V_{SS}		0.8	V	*
Input capacitance measured against V_{SS}, V_I = 0 V	C_I			5	pF	*
Period	$T_{LL1.5}$	34.6	37	39.8	ns	2
Pulse duty factor	$t_{WH}/T_{LL1.5}$	0.43	0.5	0.57		2
Skew for LL3	t_{SK}	– 5		5	ns	*
Transition times	t_{HL}, t_{LH}	2		6	ns	2
Input Signals: LL3 100-Hz (120-Hz) Field PAL (NTSC); TTL Input						
H-input voltage	V_{IH}	2.3		V_{DD}	V	*
L-input voltage	V_{IL}	V_{SS}		0.8	V	*
Input capacitance measured against V_{SS}, V_I = 0 V	C_I			5	pF	*
Period **	T_{LL3}	69.2	74	79.6	ns	2
Pulse duty factor	t_{WH}/T_{LL3}	0.43	0.5	0.57		2
Skew for LL3	t_{SK}	see LL1.5				*
Transition times	t_{HL}, t_{LH}	2		6	ns	2

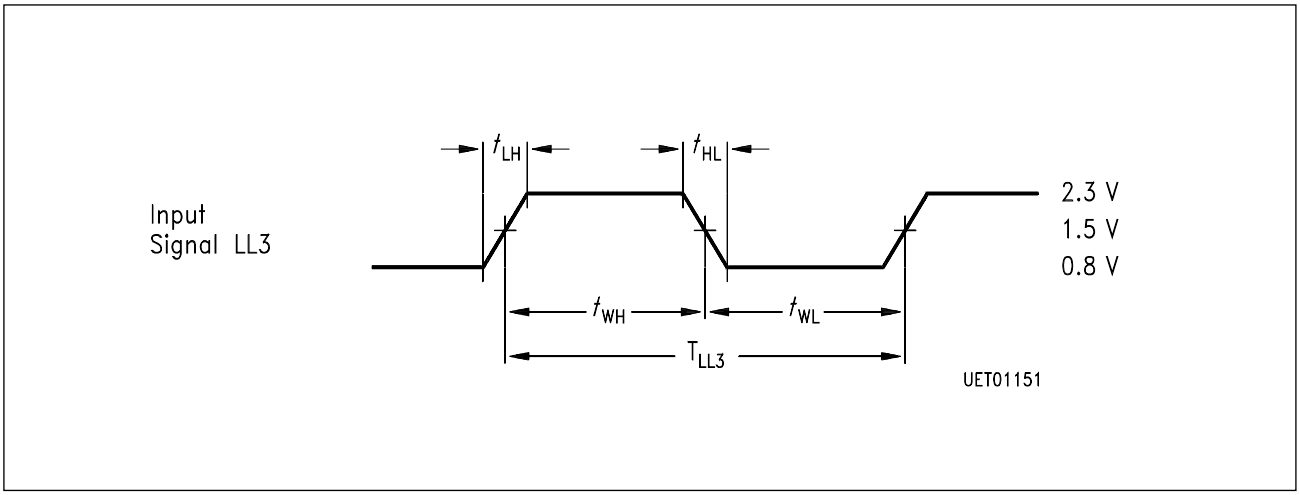
* Measurement only possible with considerable effort.

** Instead of LL3, LL1.5 can be fed into this input if HS2 is clocked with LL1.5. (For tolerances see sheet for Input LL1.5).

Input Signals LL1.5



Input Signals LL3



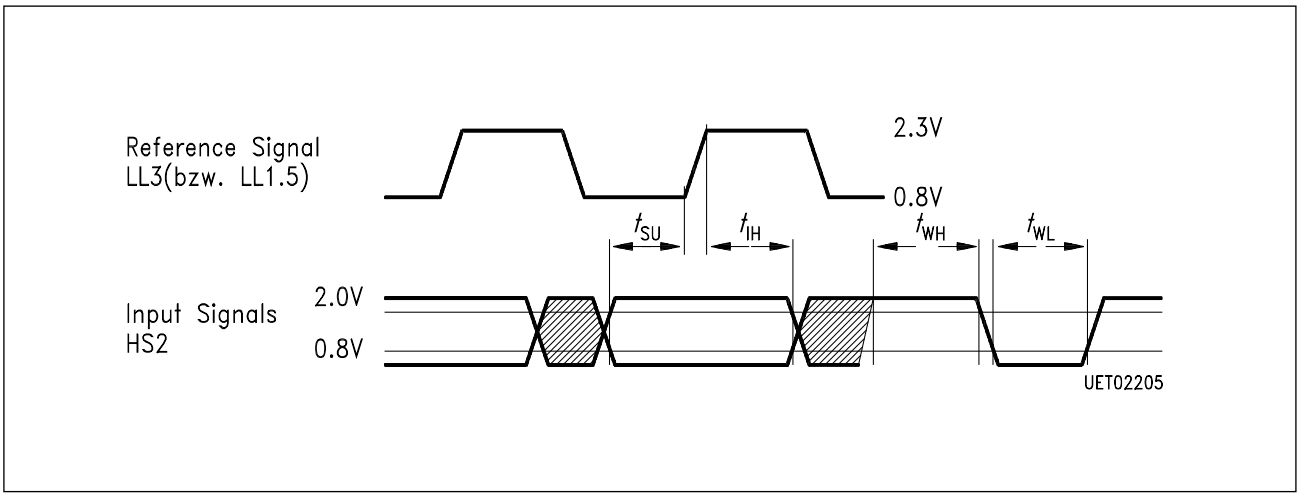
Characteristics (cont'd)

T_A = 25 °C; V_{DD} = 5 V (all voltages are referred to V_{SS})

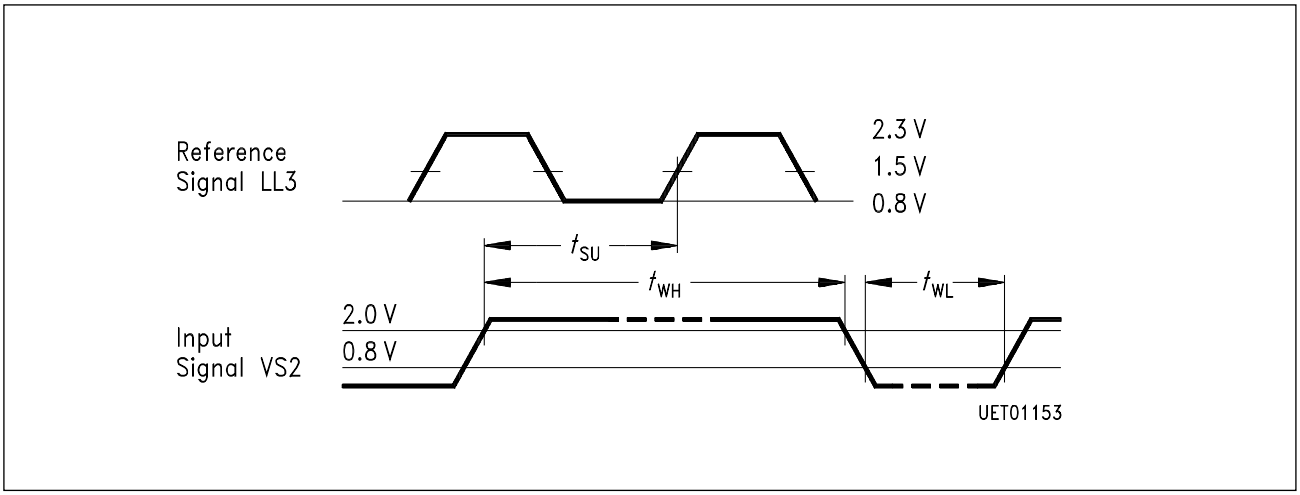
Parameter	Symbol	Limit Values			Unit	Test Circuit
		min.	typ.	max.		
Input Signals: HS2 100-Hz (120-Hz) Field Horizontal Sync Pulse						
H-input voltage	V_{IH}	2		V_{DD}	V	*
L-input voltage	V_{IL}	V_{SS}		0.8	V	*
H-pulse width	t_{WH}	16			$T_{LL1.5}$	3
Input capacitance measured against V_{SS}, V_I = 0 V	C_I			10	pF	*
Period	T_{HS2}		864 (858)		$T_{LL1.5}$	3
Start-up time for LL3	t_{SU}	12			ns	4
Hold time for LL3	t_{IH}	2.5			ns	4
L-pulse width	t_{WL}	16			$T_{LL1.5}$	4
Input Signals: VS2 100-Hz (120-Hz) Field Vertical Sync Pulse						
H-Input voltage	V_{IH}	2		V_{DD}	V	6
L-Input voltage	V_{IL}	V_{SS}		0.8	V	6
H-pulse width	t_{WH}	1		239	T_{HS2}	5
Input capacitance measured against V_{SS}, V_I = 0 V	C_I			10	pF	*
Period	T_{VS2}	240		342	T_{HS2}	5
Start-up time	t_{SU}	12			ns	*

* Measurement only possible with considerable effort.

Input Signals HS2



Input Signals VS2



Characteristics (cont'd)

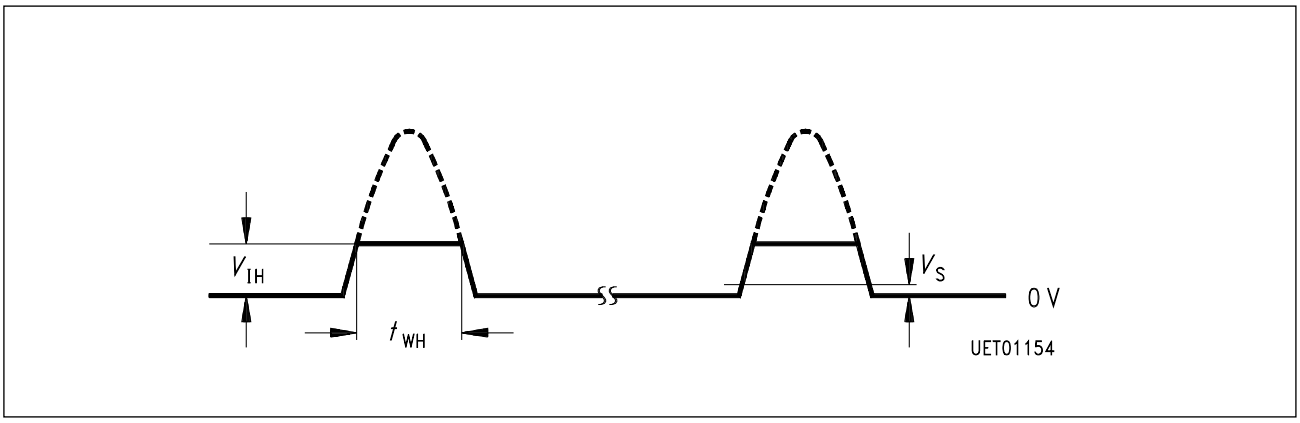
T_A = 25 °C; V_{DD} = 5 V (all voltages are referred to V_{SS})

Parameter	Symbol	Limit Values			Unit	Test Circuit
		min.	typ.	max.		
Input Signal: ZR-Line Retrace						
H-input voltage	V_{IH}	3.5		V_{DD}	V	*
L-input voltage	V_{IL}	– 0.3		0.8	V	*
H-pulse width	t_{WH}	4	5.5	7	µs	7
Input capacitance measured against V_{SS}, V_I = 0 V	C_I			10	pF	*
Switching threshold	V_S	1	1.8	2.1	V	*
Switching threshold** V_{REFA} = 5.1 V	V_{SHA}	2.5	3	3.5	V	8

* Measurement only possible with considerable effort.

** When the threshold V_{SHA} is exceeded, status HA2 = L is not longer possible. Application note: generate pulse at ZR by means of Z-diode circuitry.

Input Signal ZR



Characteristics (cont'd)

T_A = 25 °C; V_{DD} = 5 V (all voltages are referred to V_{SS})

Parameter	Symbol	Limit Values			Unit	Test Circuit
		min.	typ.	max.		
Input Signal: V_{REFA} Reference Voltage						
Input voltage (during operation) at 5.1 V on Z diode $TC \leq 1$ mV/K	V_{IH}	4.84	5.1	5.36	V	*
Input current	I_{IL}		2.3	5	mA	9
Input capacitance measured against V_{SS}, V_I = 0 V	C_I			25	pF	*
Ripple				0.5	mV	*
Input Signals: VG, ISTR (A/D converter inputs)						
Typ. input voltage ΔV_I = 1.36 V	V_I	1.73		3.09	V	*
Min. input voltage ΔV_I = 1.29 V, V_{REFA} = min	$V_{I\ min}$	1.64		2.93	V	*
Max. input voltage ΔV_I = 1.43 V, V_{REFA} = max	$V_{I\ max}$	1.81		3.24	V	*
Input capacitance for VG	C_I			70	pF	*
Input capacitance for ISTR	C_I			70	pF	*
Sampling time***	t_S		168/LL1.5**		µs	*
Conversion time	t_C		798/LL1.5**		µs	*
Conversion Data						
Resolution 9 bits (LSB = 1.36 V: 2^9 = 2.6 mV) Absolute accuracy (offset and gain errors)				± 4	LSB	*
Non-linearity (deviation from straight line)				± 1/2	LSB	*
Differential non-linearity				± 1/2	LSB	*
Conversion time	t_C			29.5	µs	*

* Measurement only possible with considerable effort.

** LL1.5 in MHz

*** During the sampling time, the generator resistance must be able to charge/discharge the input capacitance from max. 70 pF to an accuracy of 9 bits (exactly ΔV = 1.43 V).

Characteristics (cont'd)

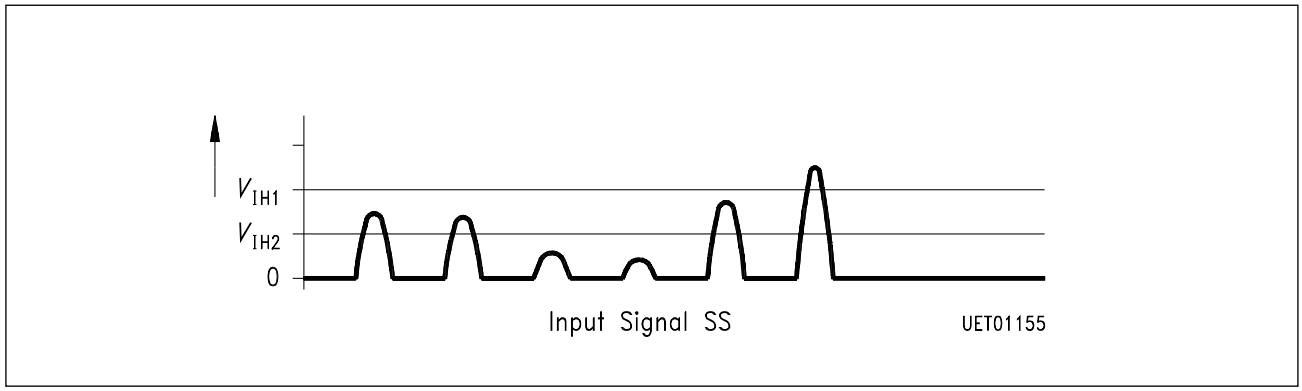
T_A = 25 °C; V_{DD} = 5 V (all voltages are referred to V_{SS})

Parameter	Symbol	Limit Values			Unit	Test Circuit
		min.	typ.	max.		
Input Signal: SS-Protective Circuitry						
H-input voltage $V_{IH1} \geq V_{IH} \geq V_{IH2}$ (protective circuitry does not respond)	V_{IH}	2.8	3.3	3.8	V	*
H-pulse width	t_{WH}		5.5		µs	*
L-pulse width	t_{WL}		26.5		µs	*
Input capacitance measured against V_{SS}, V_I = 0 V	C_I			10	pF	*
Response threshold for protective circuitry V_{REFA} = 5.1 V	$V_{IH\,1}$	3.9	4	4.2	V	10
	$V_{IH\,2}$	2.1	2.4	2.7	V	*
Input Signal: (I^2C Bus clock)						
H-input voltage I_{IH} = 10 µµA max at V_{DD} = min	V_{IH}	3.0		V_{DD}	V	*
L-input voltage $-I_{IH}$ = 10 µµA	V_{IL}	V_{SS}		1.5	V	*
Input capacitance measured against V_{SS}, V_I = 0 V	C_I			10	pF	*

* Measurement only possible with considerable effort

For timing and transfer modes refer to I^2C Bus protocol

Input Signal SS

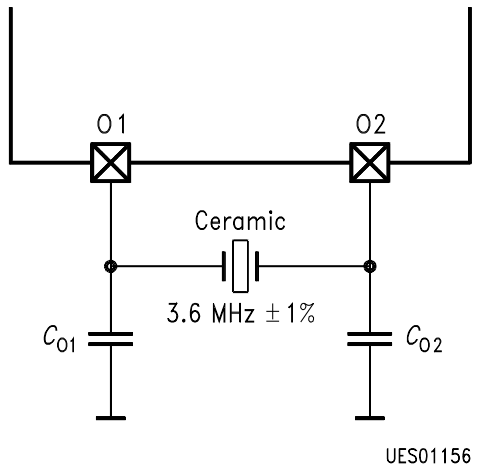


Characteristics (cont'd)

T_A = 25 °C; V_{DD} = 5 V (all voltages are referred to V_{SS})

Parameter	Symbol	Limit Values			Unit	Test Circuit
		min.	typ.	max.		
Input Signal: HA2EN Enabling/Disabling of HA2 Pulses						
H-input voltage**	V_{IH}	4		V_{DDS}	V	11
L-input voltage**	V_{IL}	V_{SS}		2.9	V	11
Input capacitance V_I = 0 V	C_I			10	pF	*
Input Signal: O1 Oscillator Input Start-Up Circuitry						
H-input voltage	V_{IH}	3.5		V_{DDS}	V	12
L-input voltage	V_{IL}	V_{SS}		1.5	V	12
Input capacitance V_I = 0 V	C_I			10	pF	*
External capacitance**** (depends on the characteristics of the ceramic resonator)	C_{O1} C_{O2}		30 30		pF pF	13 13
Input Signal: RESET Input for External Reset Signal						
H-input voltage***	V_{IH}	2		V_{DD}	V	14
L-input voltage***	V_{IL}	V_{SS}		0.8	V	14
Input capacitance V_I = 0 V	C_I			10	pF	*

Input Signal O1



* Measurement only possible with considerable effort.

** Input is high (by internally pull-up resistor approx. 100 kΩ) and HA2 pulses are enabled.
Input is low and HA2 pulses are disabled. V_{REFA} = 5.1 V

*** Input is high (by internally pull-up resistor approx. 100 kΩ), i.e. the IC is in the active mode.
Input is low, i.e. the IC has been reset.

**** Dependent upon characteristics of ceramic oscillator.

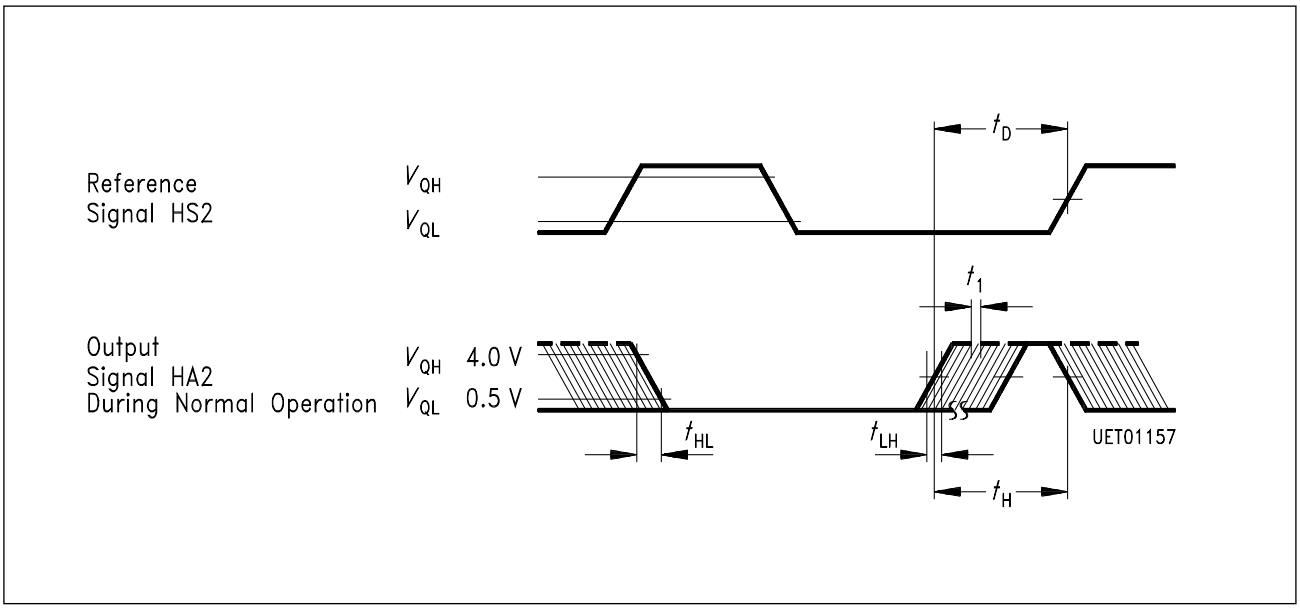
Characteristics (cont'd)

T_A = 25 °C; V_{DD} = 5 V (all voltages are referred to V_{SS})

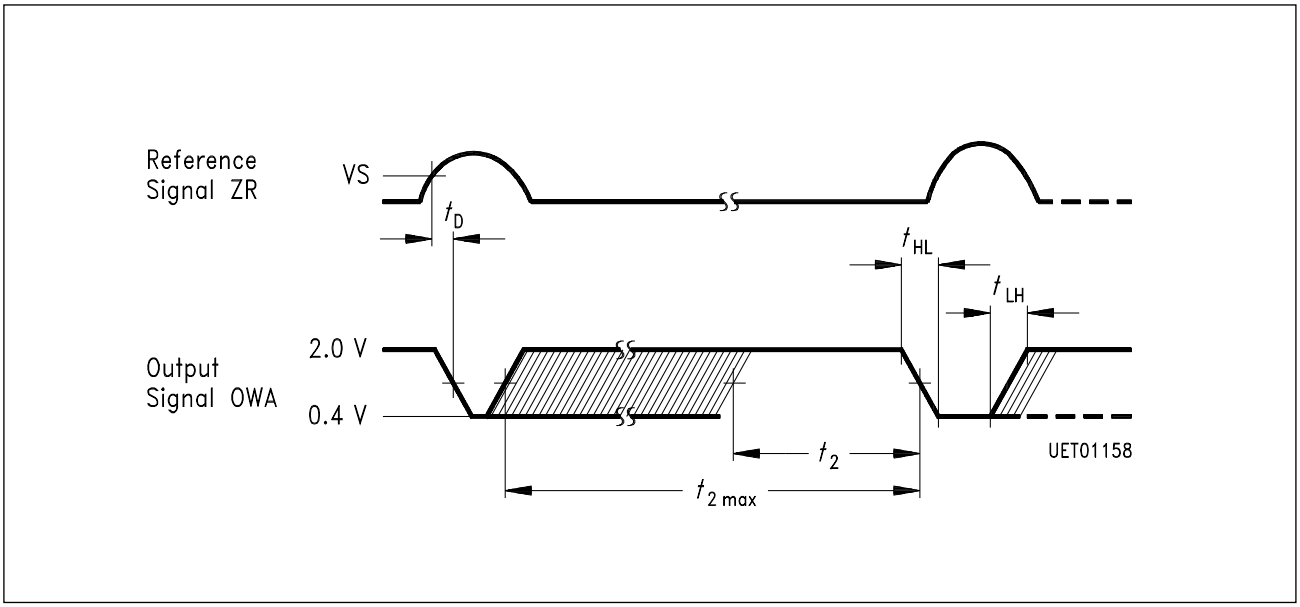
Parameter	Symbol	Limit Values			Unit	Test Circuit
		min.	typ.	max.		
Bidirectional Signal: SDA (open drain I²C Bus)						
H-input voltage I_{IH} = 10 µA max at V_{DD} = min	V_{IH}	3		V_{DD}	V	*
L-input voltage – I_{IL} = 10 µA	V_{IL}	V_{SS}		1.5	V	*
H-output voltage[1] – I_{QH} = 10 µA	V_{QH}			V_{DD}	V	*
L-output voltage – I_{QL} = 2 mA	V_{QL}			0.4	V	*
H-L transition time C_L = 300 pF	t_{THL}			0.5	µs	*
L-H transition time[2] C_L = 300 pF	t_{TLH}				µs	*
Input capacitance measured against V_{SS}, V_I = 0 V	C_I			10	pF	*
For timing and transfer modes refer to I²C Bus protocol						
Output Signals: HA2 100 Hz- (120-Hz) Field Horizontal Driver						
H-output voltage – I_{QH} = 0.5 mA	V_{QH}	4		V_{DD}	V	*
L-output voltage – I_{QL} = 3 mA	V_{QL}	V_{SS}		0.5	V	*
Limiting current[3]	I_{lim}			± 10	mA	*
Rise time C_L = 300 pF	t_{LH}			80	ns	15
Fall time C_L = 300 pF	t_{HL}			80	ns	15
Pulse width[4] t_H = constant	t_H	13.55	14.5	15.59	µs	16
Quantization step	t_1		2.3		ns	*
Delay time	t_D	3.2		10.4	µs	7

* Measurement only possible with considerable effort.
1) Minimum output voltage depends on external pull-up resistor and the leakage current I_{QH}.
2) Depends on pull-up resistor.
3) Max. permissible output current. Output is not short-circuit resistant.
4) At maximum permissible frequency fluctuation of LL1.5.

Output Signals HA2



Output Signal: OWA



Characteristics (cont'd)

T_A = 25 °C; V_{DD} = 5 V (all voltages are referred to V_{SS})

Parameter	Symbol	Limit Values			Unit	Test Circuit
		min.	typ.	max.		
Output Signal: VA1 Vertical Deflection						
(short-circuit resistant against V_{SS}) H-output voltage** – I_{QH} = 5 µA	V_{QH}	2		V_{DD} – 1	V	*
L-output voltage I_{QL} = 1 mA	V_{QL}	V_{SS}		1.3	V	*
Quantization steps	t_{QS}		1.15		ns	*
Sum of quantization steps	Σ_{QS}		32			*
Clock period	$T_{LL1.5}$		37		ns	*
Output Signal: OWA (East/West raster correction)						
H-output voltage – I_{QH} = 5 mA	V_{QH}	2		V_{DD}	V	*
H-output voltage I_{QH} = 5 mA	V_{QL}	V_{SS}		0.4	V	*
Limiting current	I_{lim}			10	mA	*
Rise time C_L = 300 pF	t_{LH}			30	ns	17
Fall time C_L = 300 pF	t_{HL}			30	ns	17
H-pulse width	t_2			864	LL1.5	*
Delay time	t_D	depends on Φ_2 adjustment circ.			µs	

* Measurement only possible with considerable effort.
** Modulation determined by ROM occupancy.

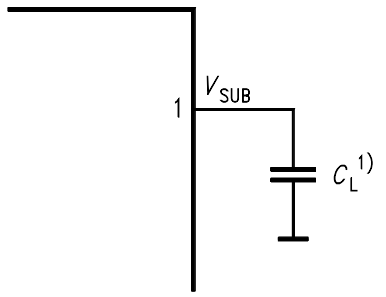
Characteristics (cont'd)

T_A = 25 °C; V_{DD} = 5 V (all voltages are referred to V_{SS})

Parameter	Symbol	Limit Values			Unit	Test Circuit
		min.	typ.	max.		
Substrate Bias Voltage V_{SUB}						
Substrate (internally generated, but can be supplied externally as well)	V_{SUB}	– 3	– 2.5	– 2	V	18
Load capacitance (recommended) measured against V_{SSA}	C_L		100		nF	
Ripple measured against V_{SSA}				50	mV	*

* Measurement only possible with considerable effort.

Substrate Bias Voltage



1) Ceramic Capacitor UET01159

Characteristics (cont'd)

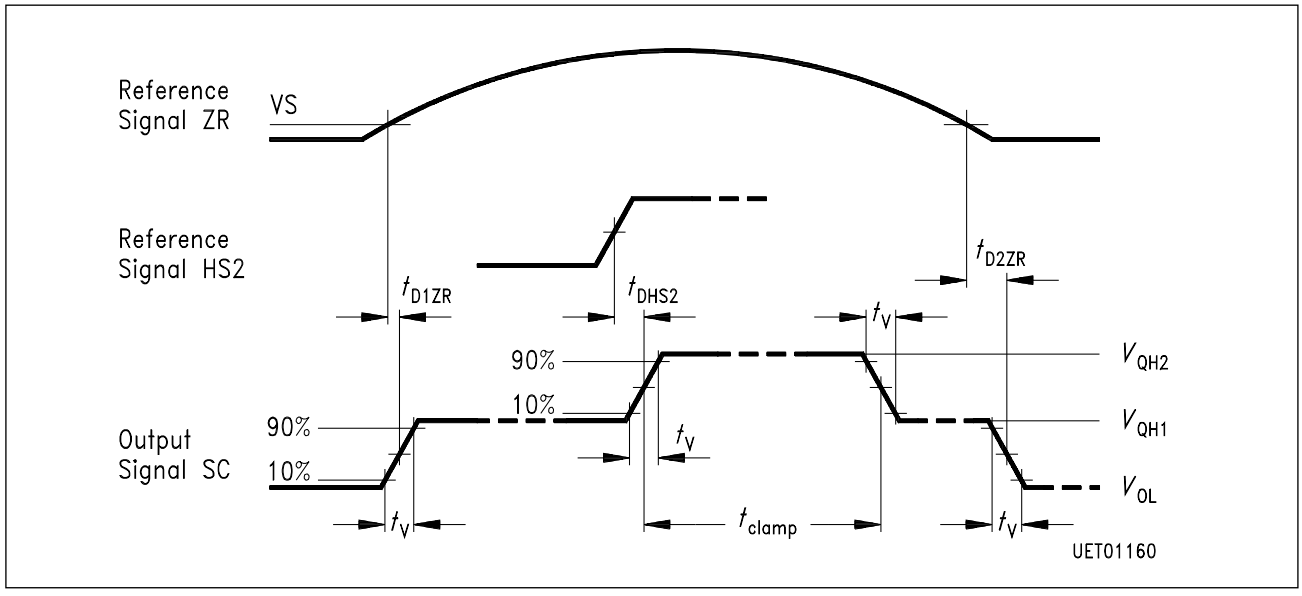
T_A = 25 °C; V_{DD} = 5 V (all voltages are referred to V_{SS})

Parameter	Symbol	Limit Values			Unit	Test Circuit
		min.	typ.	max.		
Output Signal: SC Sandcastle						
H-output voltage, level 2 I_{QH2} = – 50 µA	V_{QH2}	4.1	5	V_{DD}	V	*
H-output voltage, level 1 I_{QH1} = 100 µA	V_{QH1}	2.1	2.5	2.9	V	*
L-output voltage I_{OL} = 100 µA	V_{OL}	V_{SS}		1	V	*
Delay time with respect to ZR	t_{D1ZR} t_{D2ZR}			200 300	ns ns	*
Delay time with respect to HS2 LL1.5 = 27 MHz	t_{DHS2}	1.2		1.5	µs	19
Clamping pulse	t_{clamp}		54		$T_{LL1.5}$	1
Rise/fall time C_L = 15 pF	t		200		ns	*
Limiting current	I_{lim}			4	mA	*

* Measurement only possible with considerable effort.

For reference signal V line retrace **see page 85**.

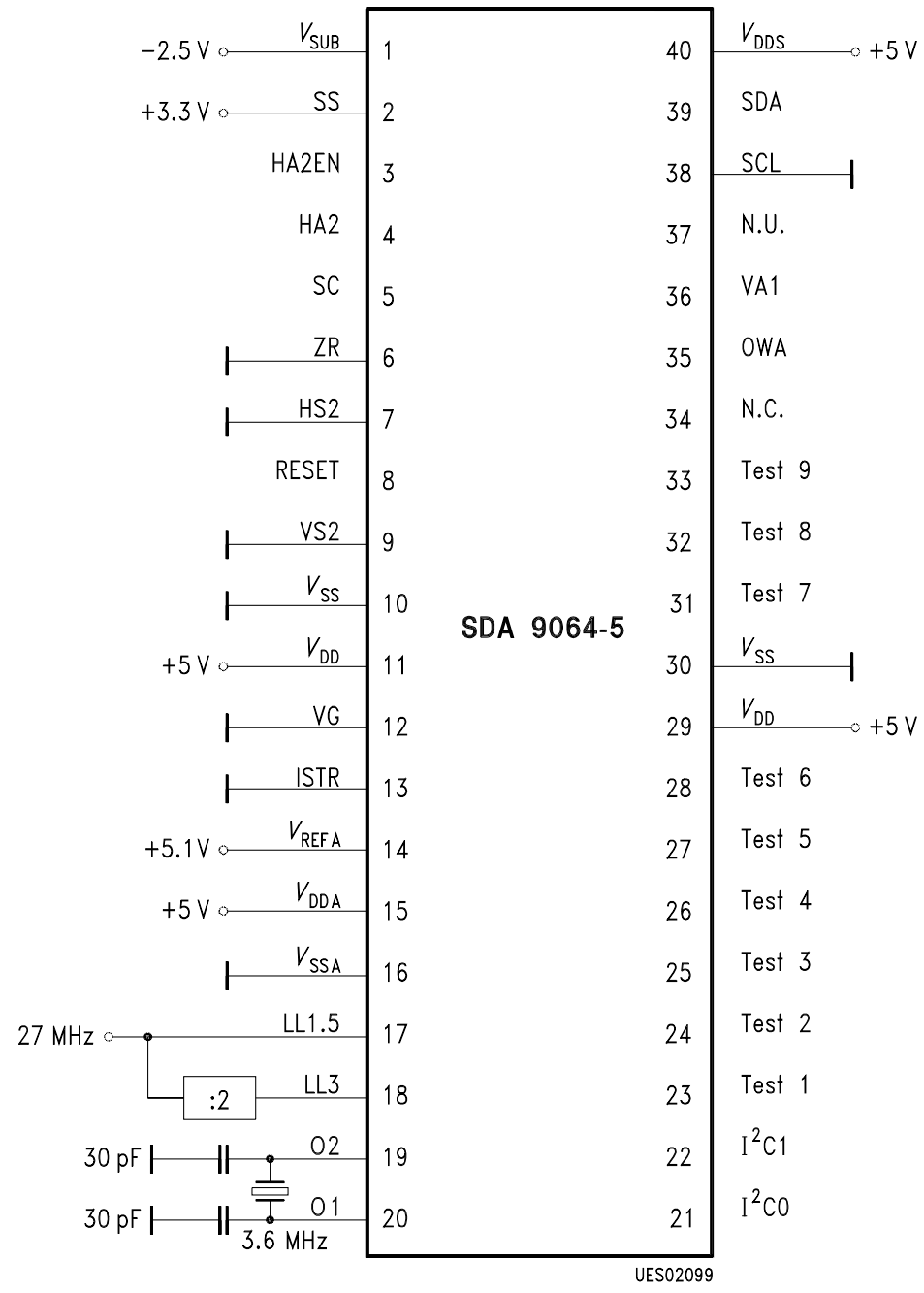
Output Signal SC



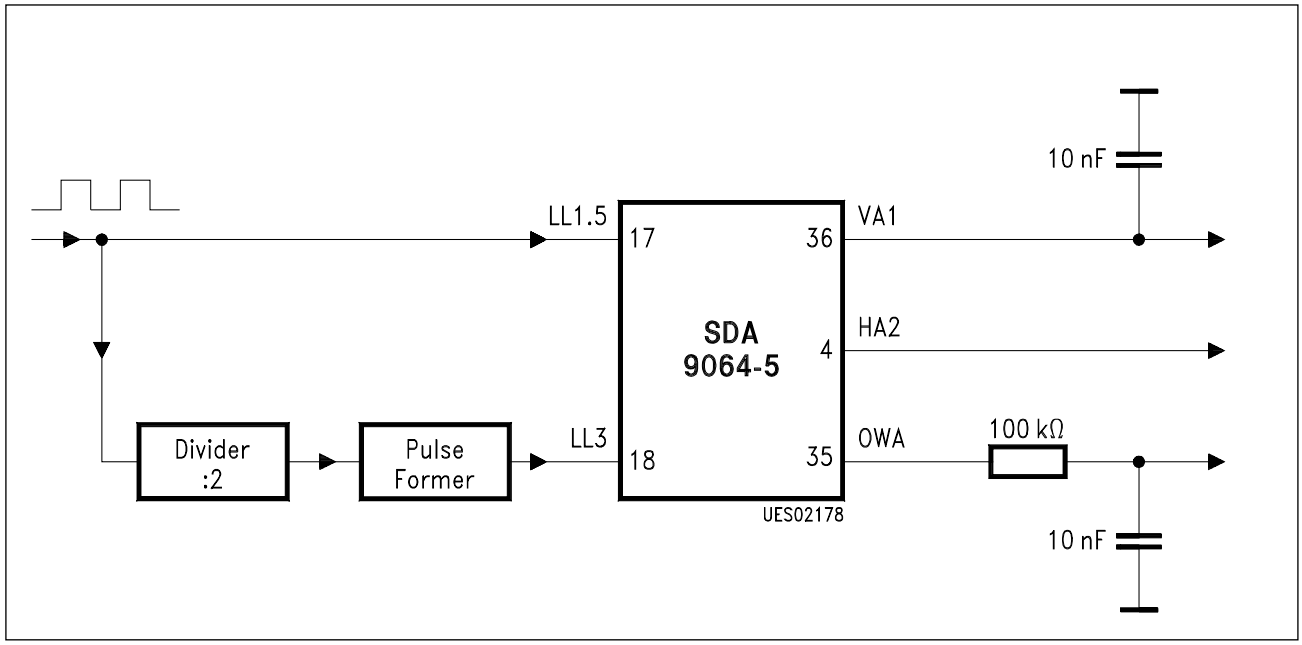
Characteristics (cont'd)

T_A = 25 °C; V_{DD} = 5 V (all voltages are referred to V_{SS})

Parameter	Symbol	Limit Values			Unit	Test Circuit
		min.	typ.	max.		
Output Signal: O2 Oscillator Output Start-Up Circuitry						
H-output voltage – I_{QH} = 100 µA	V_{QH}	3.5		V_{DDS}	V	20
L-output voltage I_{QL} = 200 µA	V_{QL}	V_{SS}		1.5	V	21
External capacitance	C_{O2}	see oscillator input			pF	
Output Signals: I²C0, I²C1						
H-output voltage – I_{QH} = 0.5 mA	V_{QH}	3		V_{DD}	V	22
L-output voltage I_{QL} = 3 mA	V_{QL}	V_{SS}		0.5	V	23

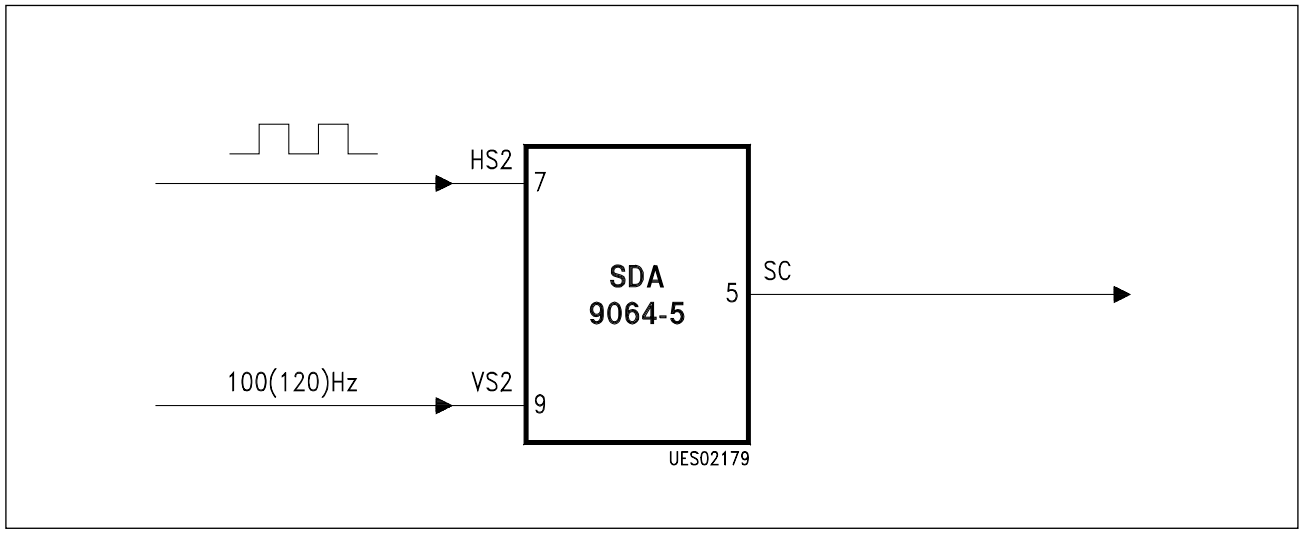


Test Circuit 1
Output Signals and Phase Relationships



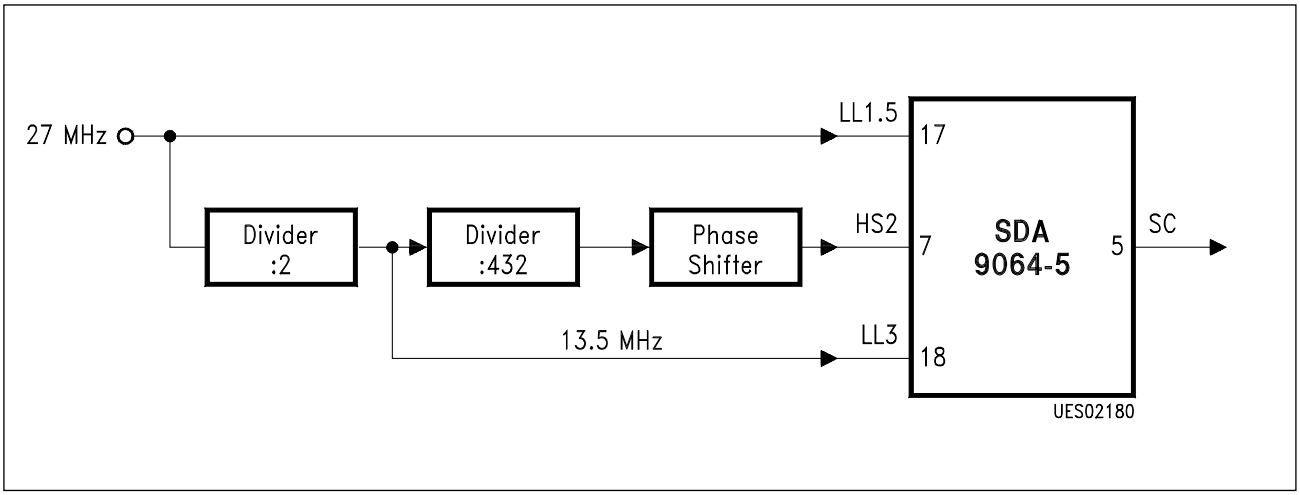
Test Circuit 2
Frequency and Pulse Duty Factor of LL1.5 and LL3

Apply to input LL1.5 a clock pulse varying in frequency, pulse duty factor and transition times and apply via a pulse shaper to input LL3 a clock pulse divided by a factor of 2. Monitor outputs HA2 (horizontal frequency pulses), OWA (vertical frequency parabola) and VA1 (vertical frequency saw-tooth). Connect all other pins as shown in **test circuit 1**.



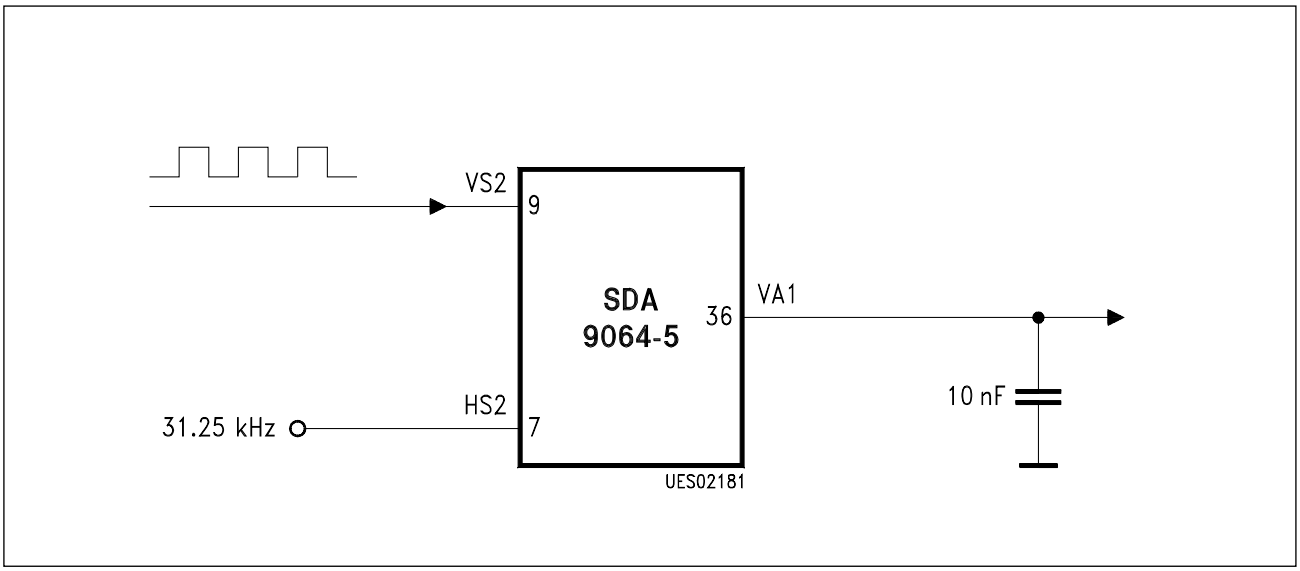
Test Circuit 3
Frequency and Pulse Duty Factor of HS2

Apply a clock pulse varying in frequency and pulse duty factor to input HS2 and monitor the time during which the pulses at output SC are synchronous with input signal HS2. Apply to input VS2 100 Hz for the 100-Hz operating mode and 120 Hz for the 120-Hz operating mode. Connect all other pins as shown in **test circuit 1.**



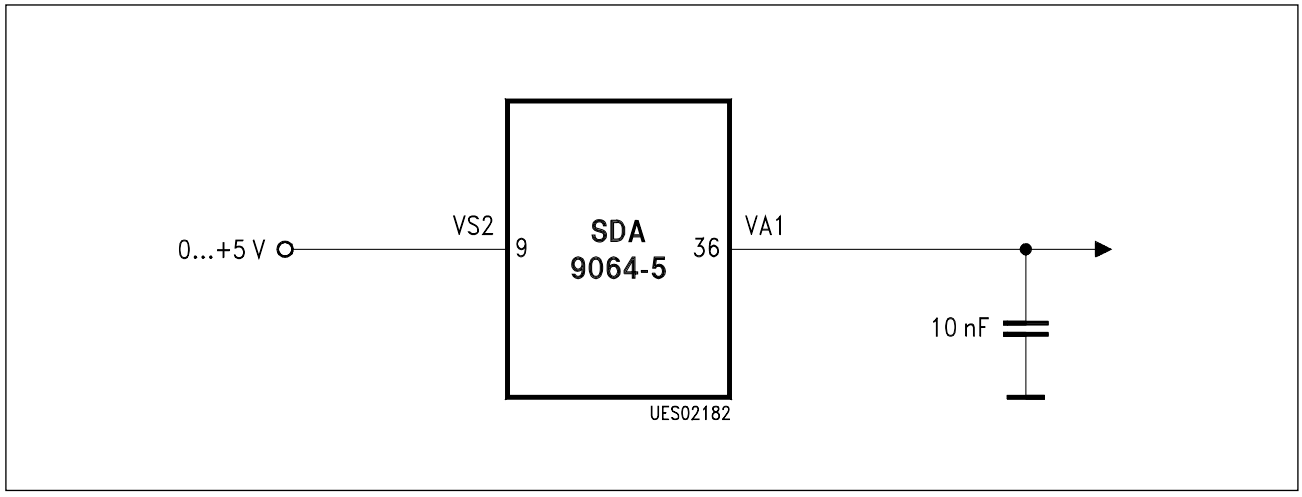
Test Circuit 4
Phase of HS2 with Respect to LL3

Apply to input HS2 a clock pulse having a frequency of 13.5 MHz/432 via an adjustable phase shifter and set the phase exactly to that at which the pulses at output SC jitter with respect to HS2 by one LL3-clock pulse. Then read off the phase between HS2 and LL3. Connect all other pins as shown in **test circuit 1**.



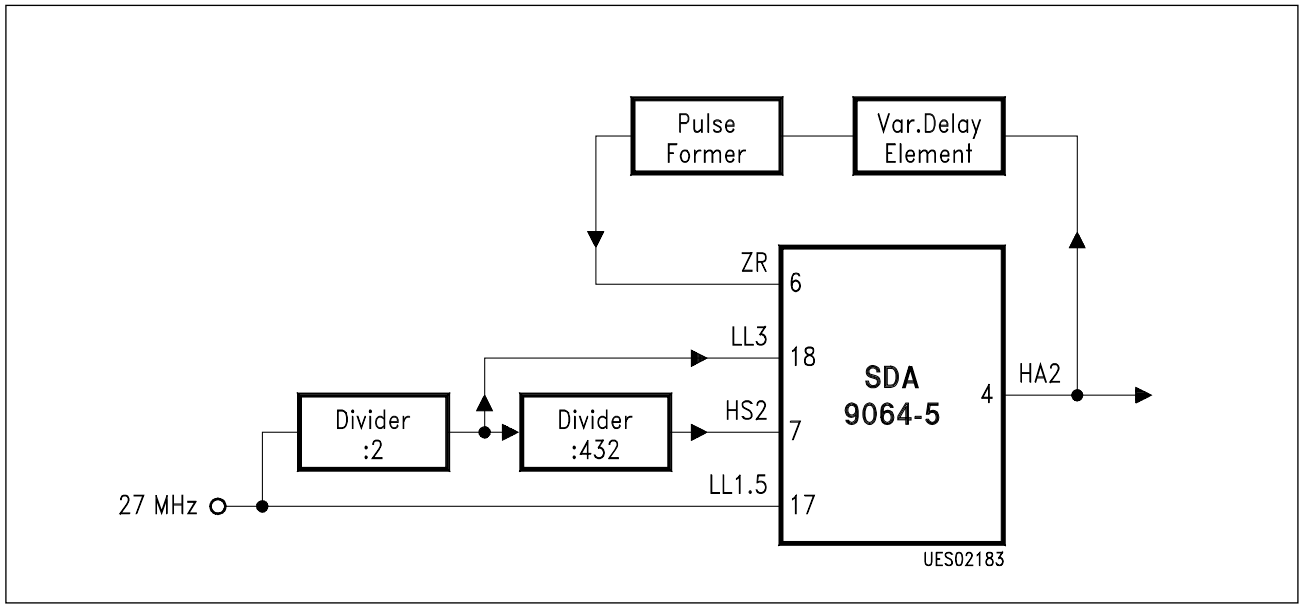
Test Circuit 5
Frequency and Pulse Duty Factor of VS2

Apply to input VS2 a clock pulse varying in frequency and pulse duty factor and monitor the time during which the saw-tooth at output VA1 is synchronous with input signal VS2. Apply a clock pulse of 31.25 kHz to input HS2. Connect all other pins as shown in **test circuit 1**.



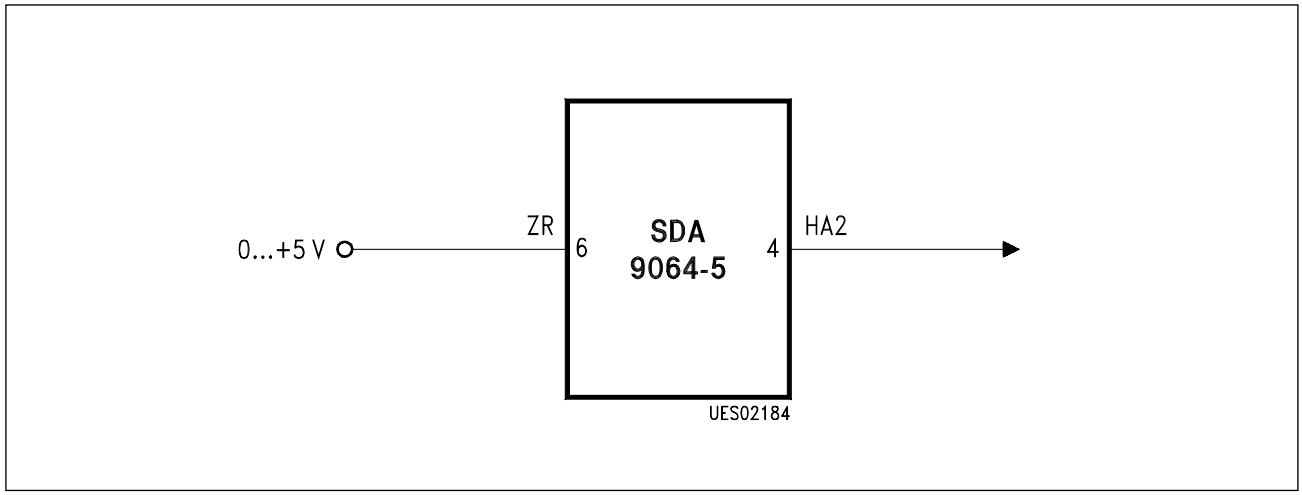
Test Circuit 6
Switching Threshold of VS2

Increase a DC voltage at input VS2, starting at 0 V, until the period of the saw-tooth output signal VA1 is appreciably reduced. Connect all other pins as shown in **test circuit 1**.



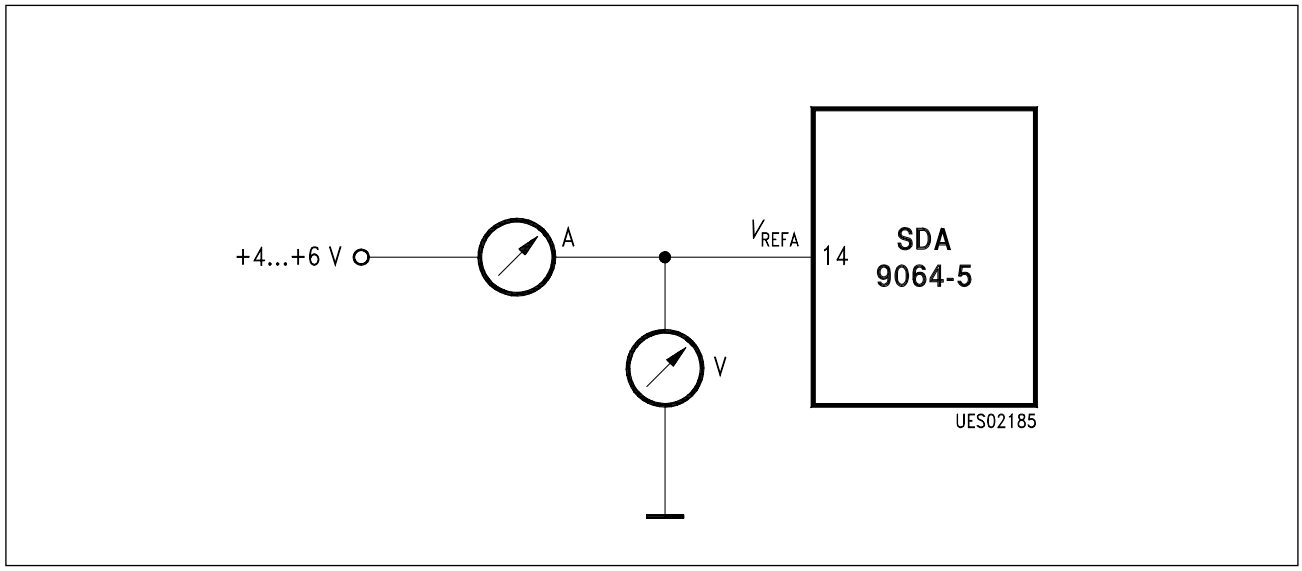
Test Circuit 7
Pulse Width of ZR

Apply clock pulse LL3 divided by a factor of 432 to output HS2. Vary the feedback signal HA2 at the ZR input with the delay element (phase) and pulse shaper (pulse width) until the center of the ZR pulse with respect to time is moved compared to the HS2 signal. Connect all other pins as shown in **test circuit 1**. This circuit may also be used to measure the time delay t_D of output signal HA2.



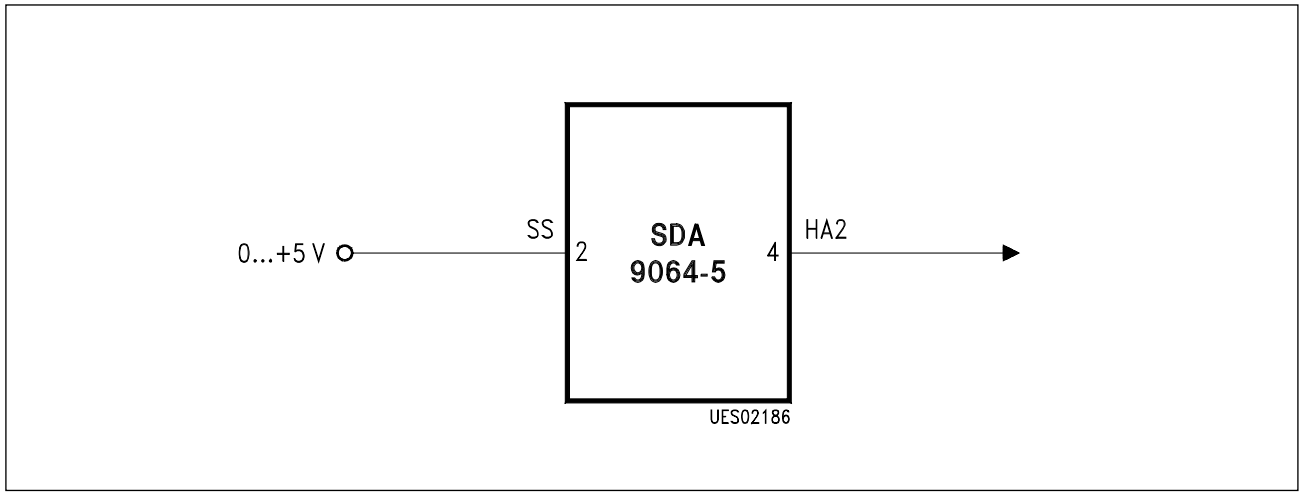
Test Circuit 8
Switching Threshold of ZR

Increase a DC voltage starting at 0 V at input ZR until output HA2 goes to high. Connect all other pins as shown in **test circuit 1**.



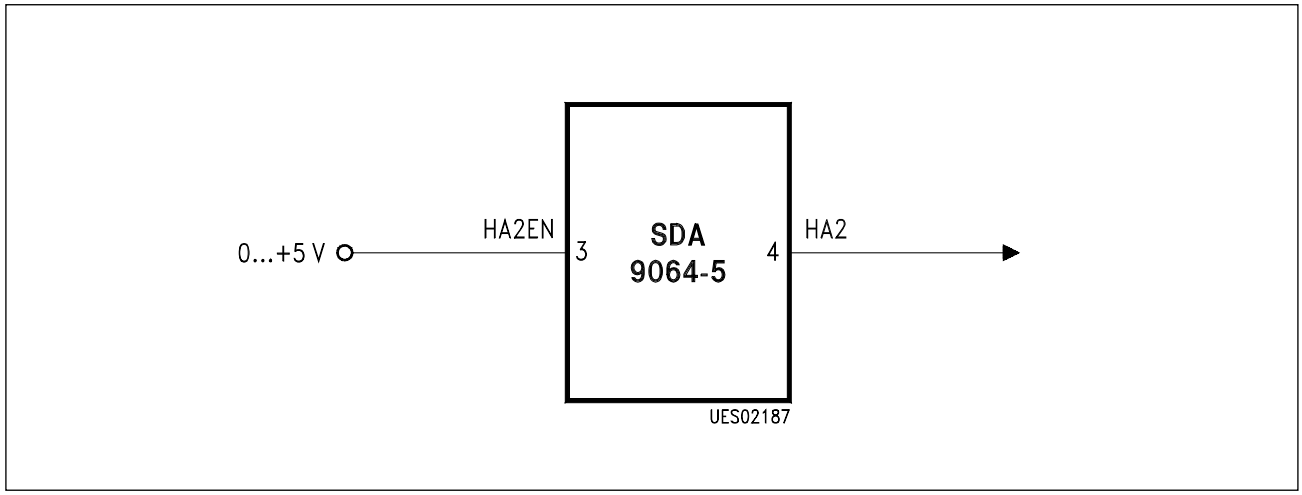
Test Circuit 9
Input Current of V_{REFA}

Set DC voltage before the ammeter such that 5.1 V are measured at input V_{REFA} with the voltmeter. Connect all other pins as shown in **test circuit 1**.



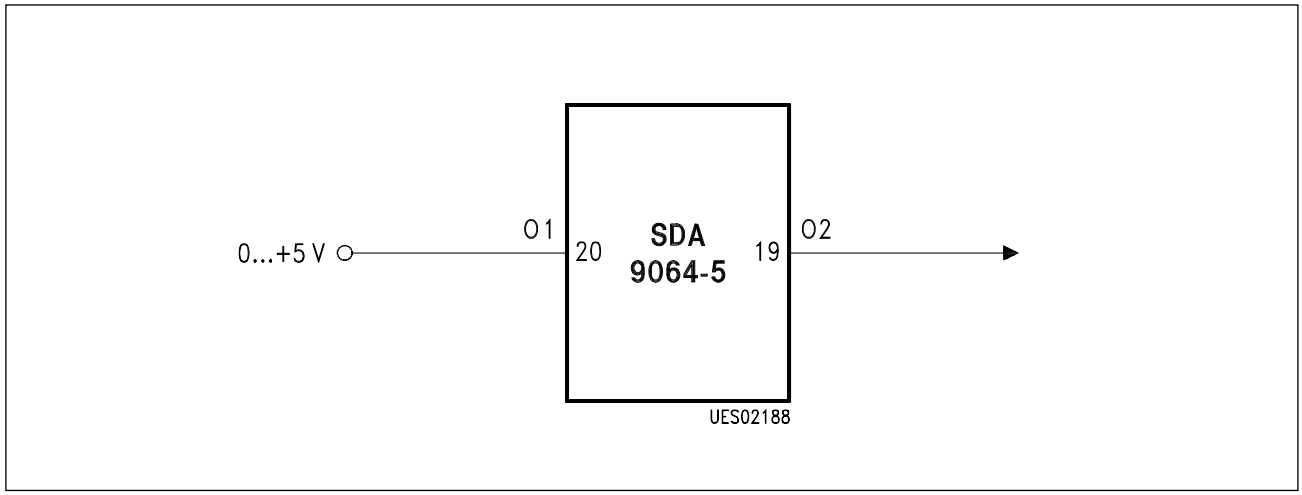
Test Circuit 10
Switching Threshold of SS

Increase a DC voltage at input SS, starting at 0 V, until output HA2 goes to high. The inhibition of HA2 can be cancelled by switching V_{DDS} on and off. Connect all other pins as shown in **test circuit 1**.



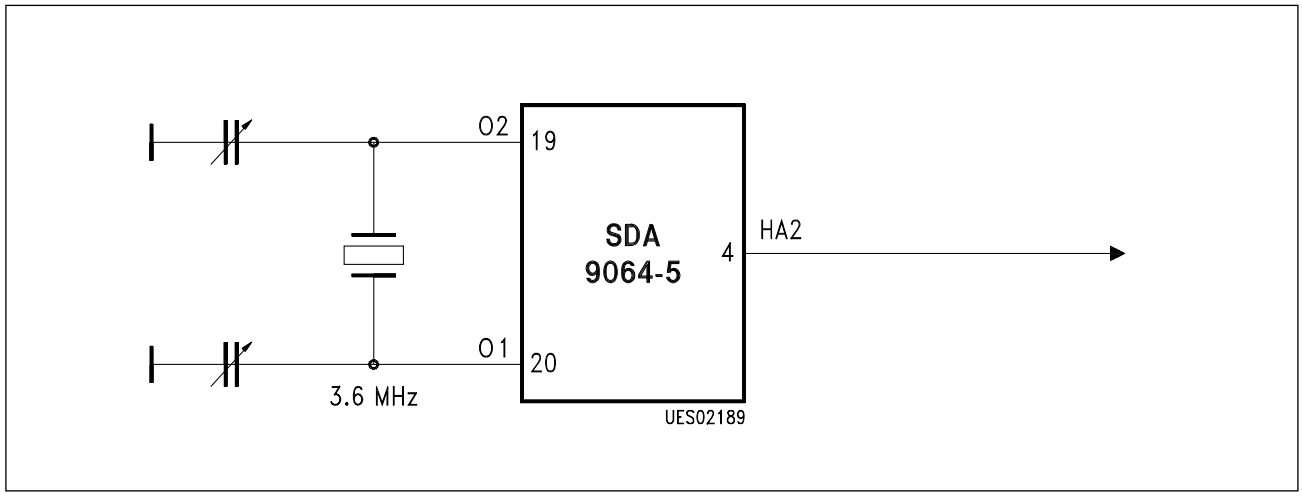
Test Circuit 11
Switching Threshold of HA2EN

Reduce a DC voltage at input HA2EN, starting at + 5 V, until output HA2 goes to high. Connect all other pins as shown in **test circuit 1**.



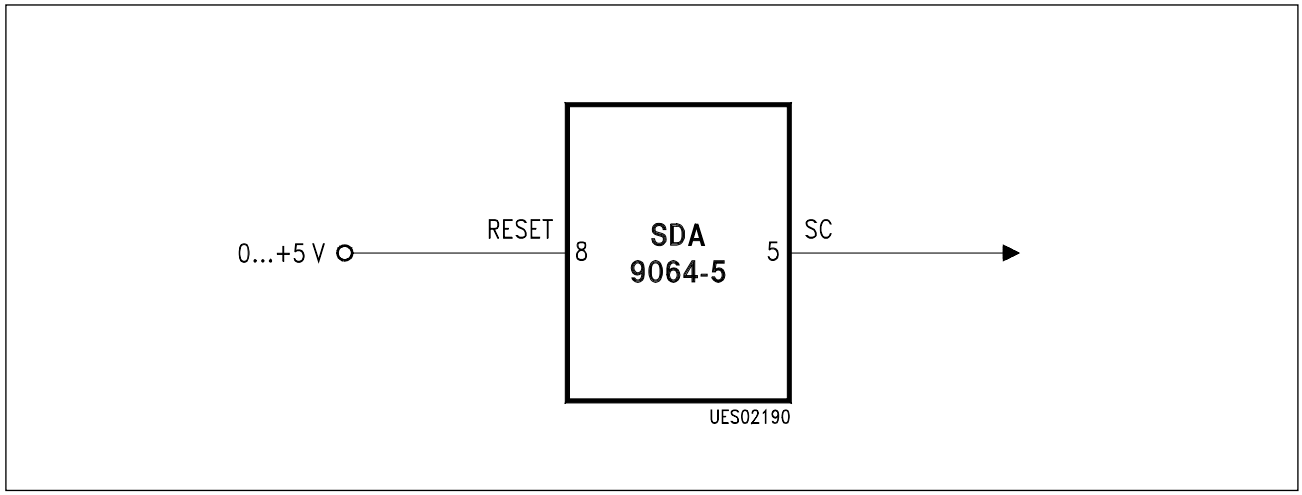
Test Circuit 12
Switching Threshold of O1

Increase a DC voltage at input O1, starting at 0 V, until O1 and O2 are equipotential. Connect all other pins as shown in **test circuit 1**.



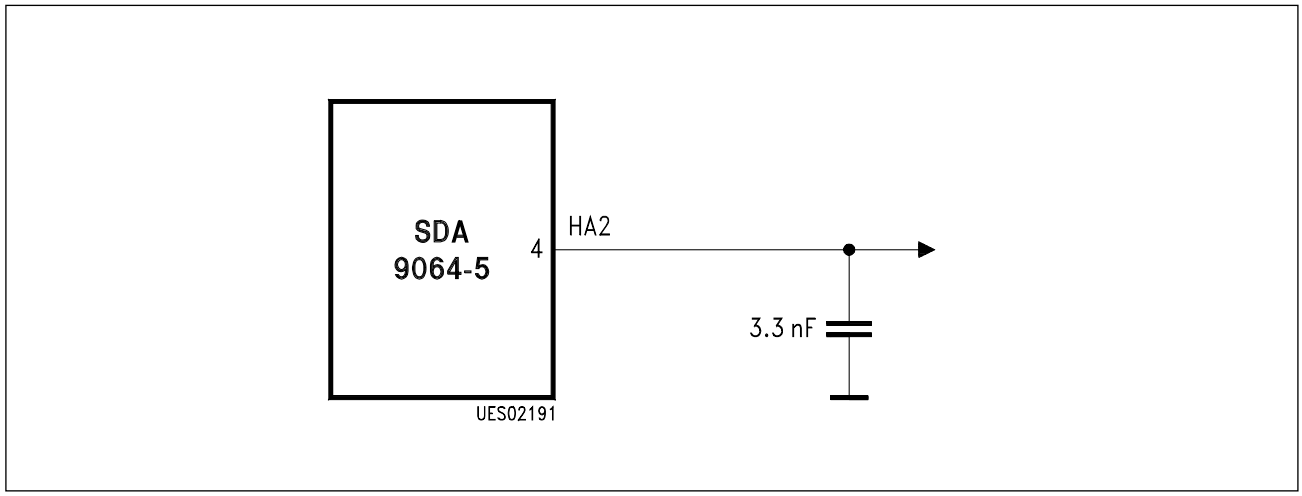
Test Circuit 13
Capacitors at O1 and O2

Vary capacitors C_1 and C_2 until the pulses specified for output HA2 are barely available at the output. Connect all other pins as shown in **test circuit 1**.



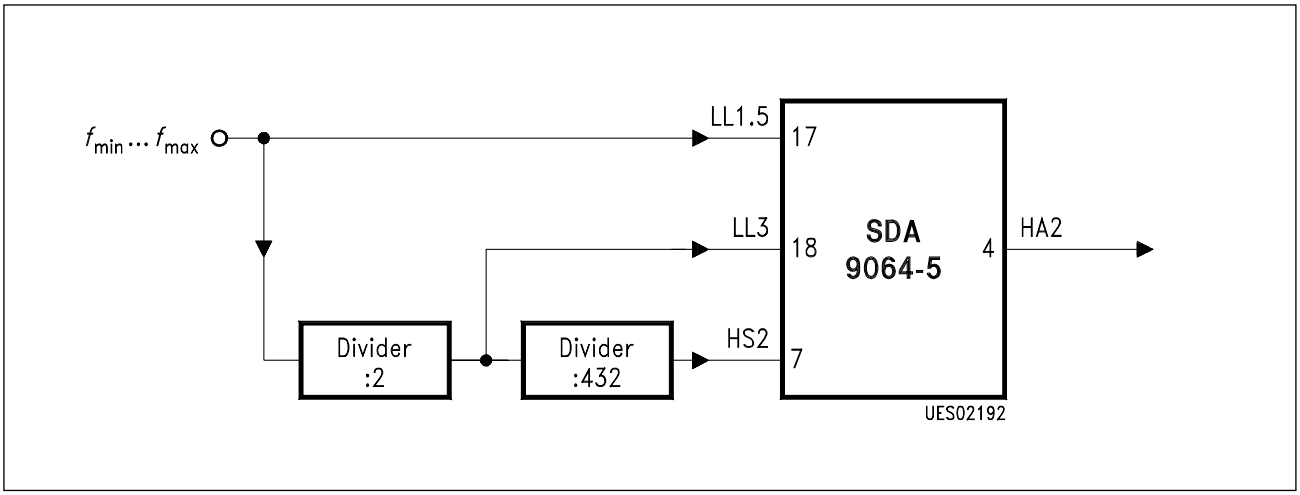
Test Circuit 14
Switching Threshold of RESET

Reduce a DC voltage at output RESET, starting at + 5 V, until output SC no longer provides any pulses. Connect all other pins as shown in **test circuit 1**.



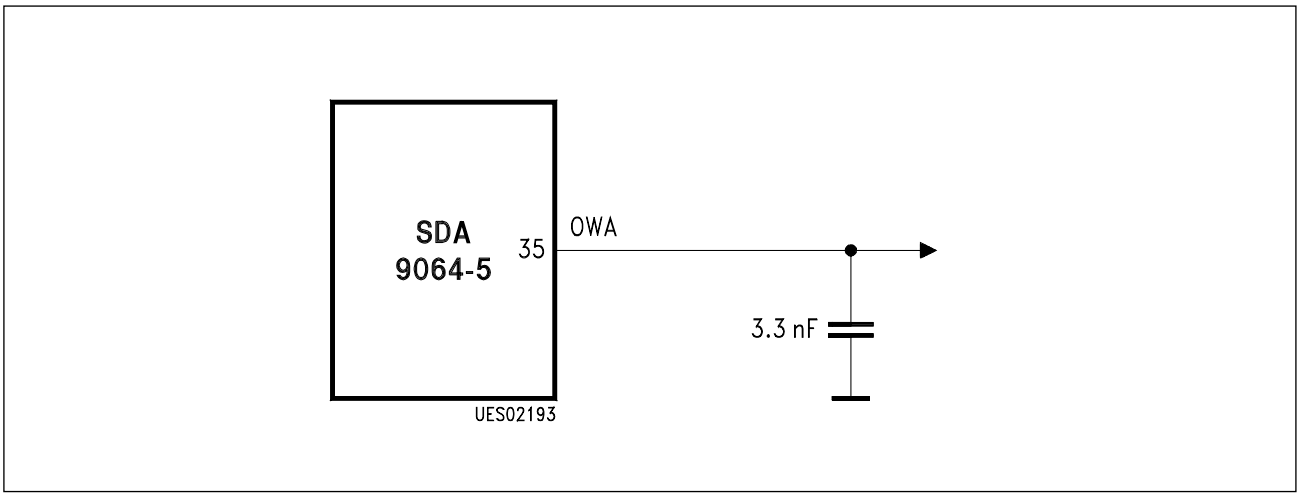
Test Circuit 15
Transition Times of HA2

Connect a 3.3 nF capacitor to output HA2 and measure the transition times between V_{QH} and V_{QL}. Convert to the load capacitance specified in the characteristics. Connect all other pins as shown in **test circuit 1**.



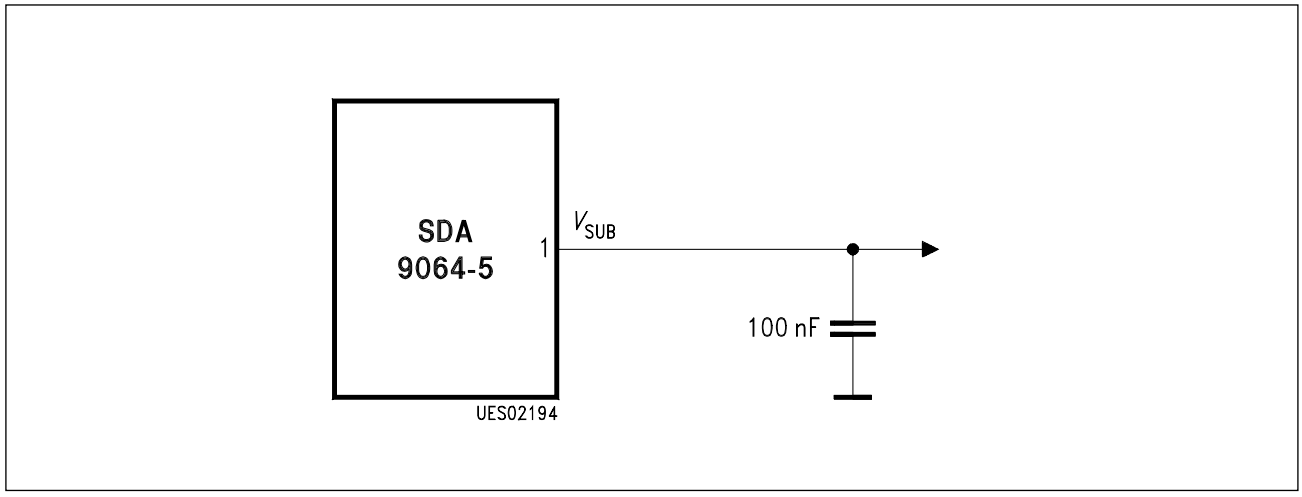
Test Circuit 16
Pulse Width of HA2

Apply to input LL1.5 a clock pulse having minimum and maximum permissible frequency (refer to characteristics of LL1.5), to input LL3 the clock pulse LL1.5 divided by a factor of 2, and to input HS2 the clock pulse LL3 divided by a factor of 432, and measure the pulse width t_H of HA2. Connect all other pins as shown in **test circuit 1**.



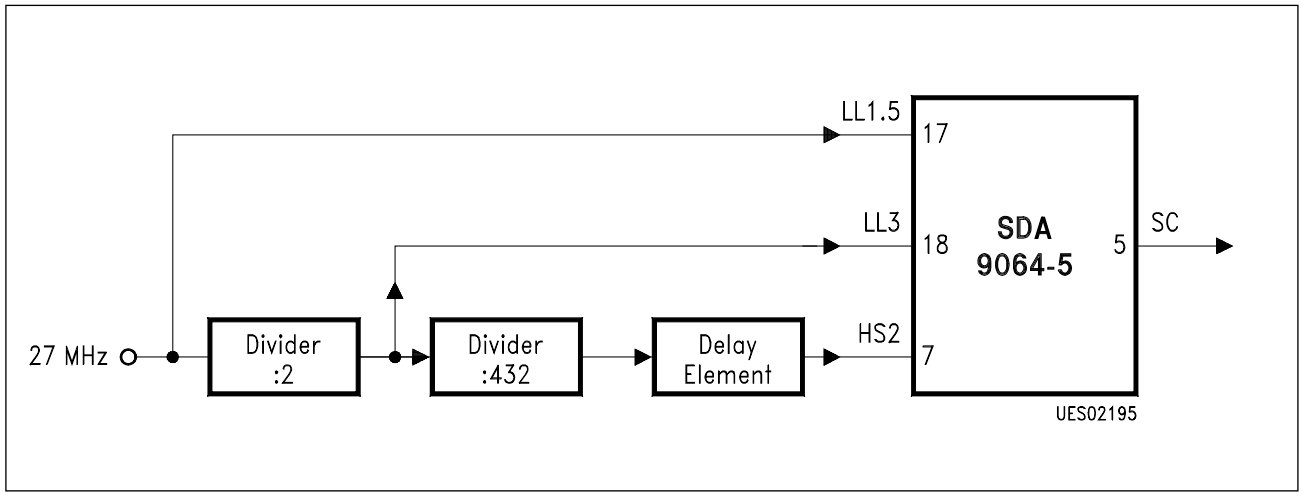
Test Circuit 17
Transition Times of OWA

Connect a 3.3 nF capacitor to output OWA and measure the transition times between V_{QH} and V_{QL}. Convert to the load capacitance specified in the characteristics. Connect all other pins as shown in **test circuit 1**.



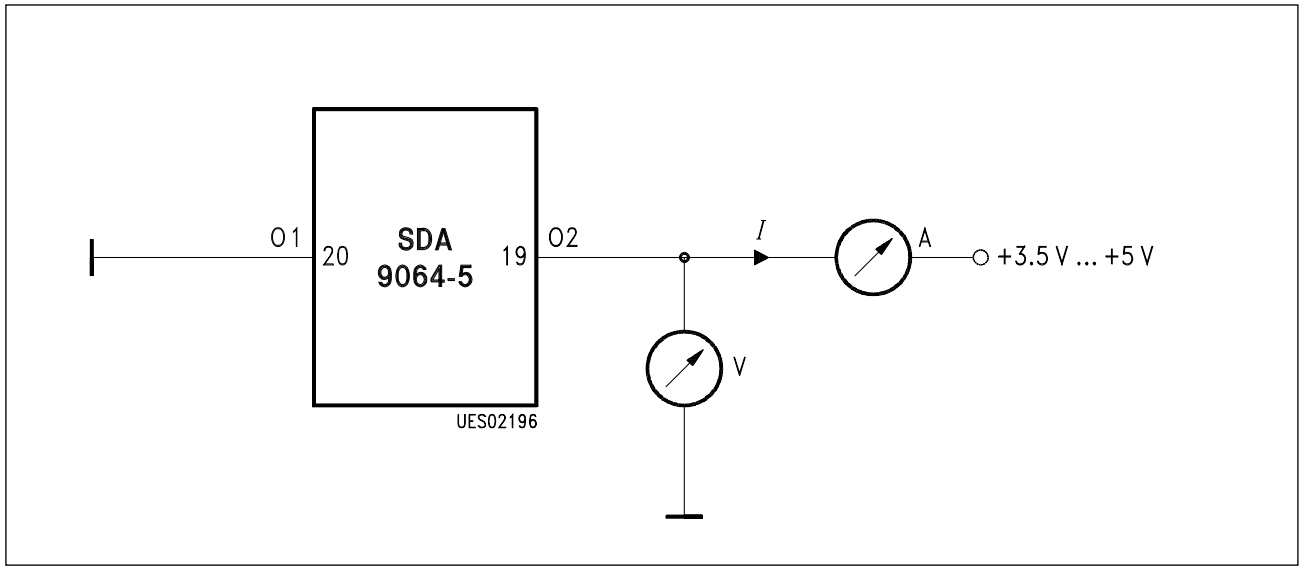
Test Circuit 18
Substrate Bias Voltage

Connect a 100 nF capacitor to pin V_{SUB} and measure the negative subtrate bias voltage V_{SUB}. Connect all other pins as shown in **test circuit 1**.



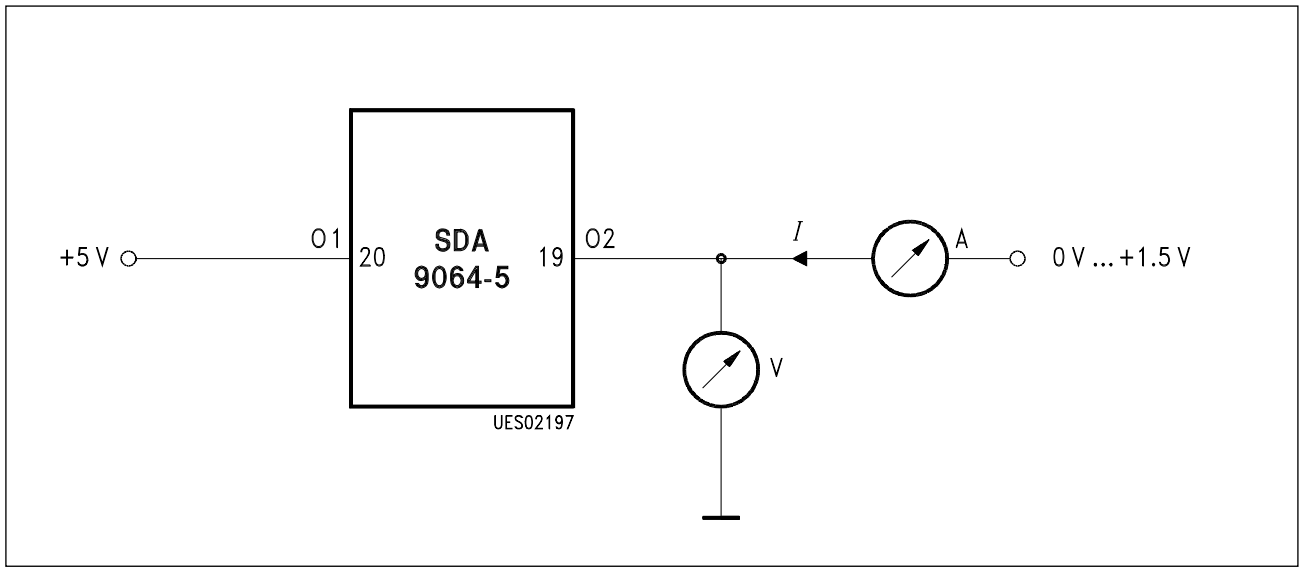
Test Circuit 19
Delay of SC with Respect to HS2

Apply clock pulse LL3 divided by a factor of 432 via a delay element to input HS2 and vary the delay by just over one LL3 period. Read off minimum and maximum delay t_{DHS2} of the clamping pulse to HS2. Connect all other pins as shown in **test circuit 1**.



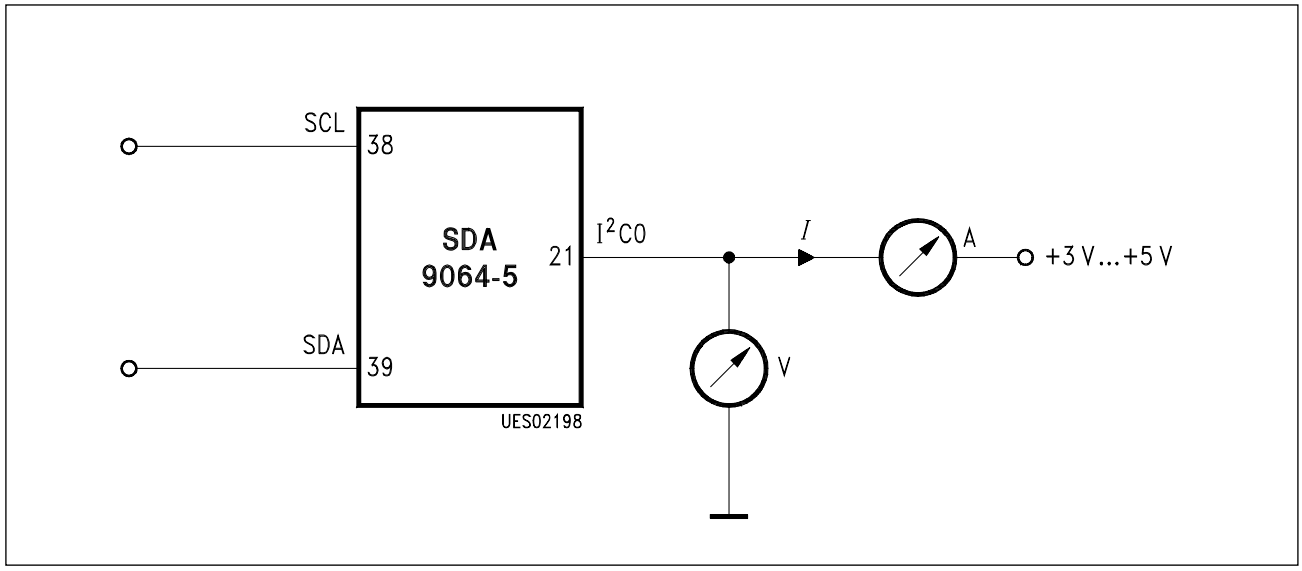
Test Circuit 20
H Level of O2

Ground input O1. Set voltage on the ammeter so that the current specified in the characteristics flows from output O2. Read off H level at O2. Connect all other pins as shown in **test circuit 1**.



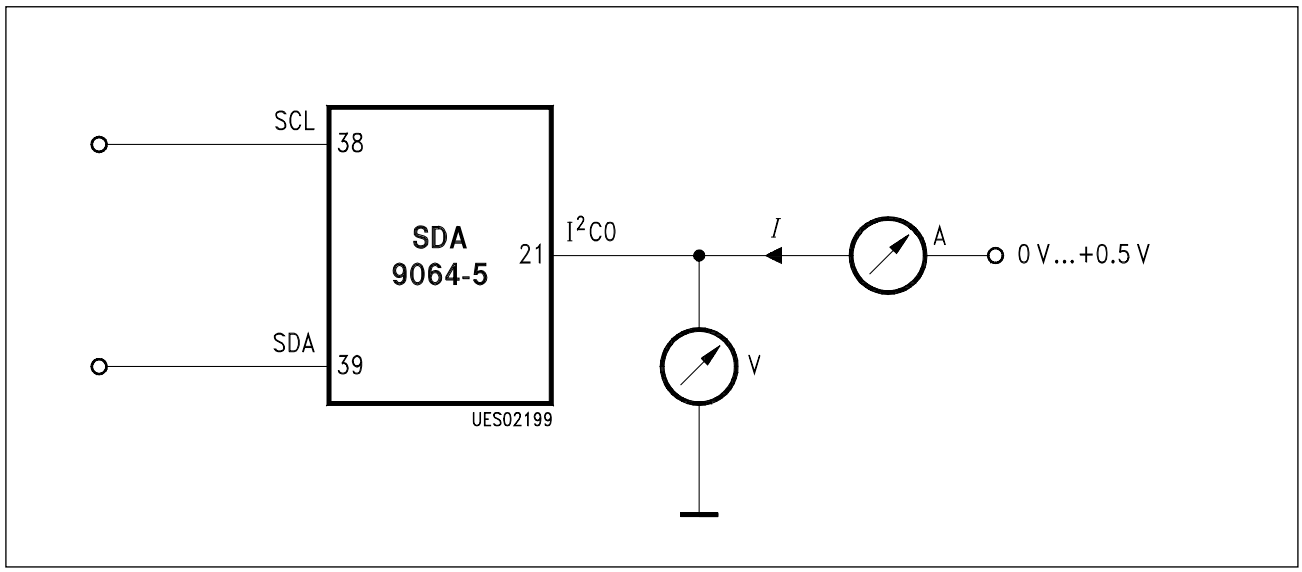
Test Circuit 21
L Level of O2

Apply + 5 V to input O1. Set the voltage on the ammeter so that the current specified in the characteristics flows into output O2. Measure L level at O2. Connect all other pins as shown in **test circuit 1**.



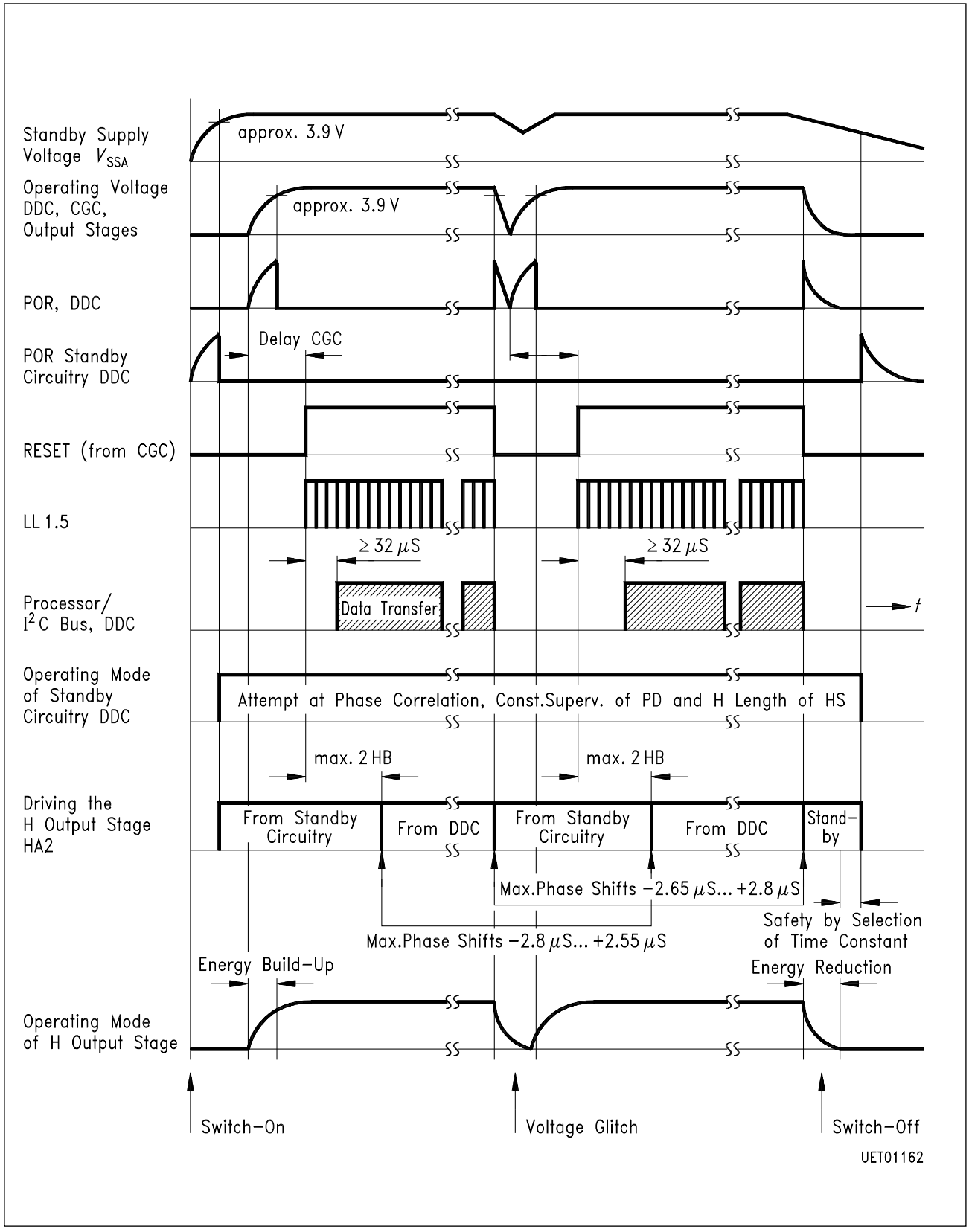
Test Circuit 22
H Level of I²C0

Set output I²C0 to high using the I²C Bus. Set the voltage on the ammeter so that the current specified in the characteristics flows from output I²C0. Measure H level at I²C0. Connect all other pins as shown in **test circuit 1**.
This measuring circuit can also be used for output I²C1.

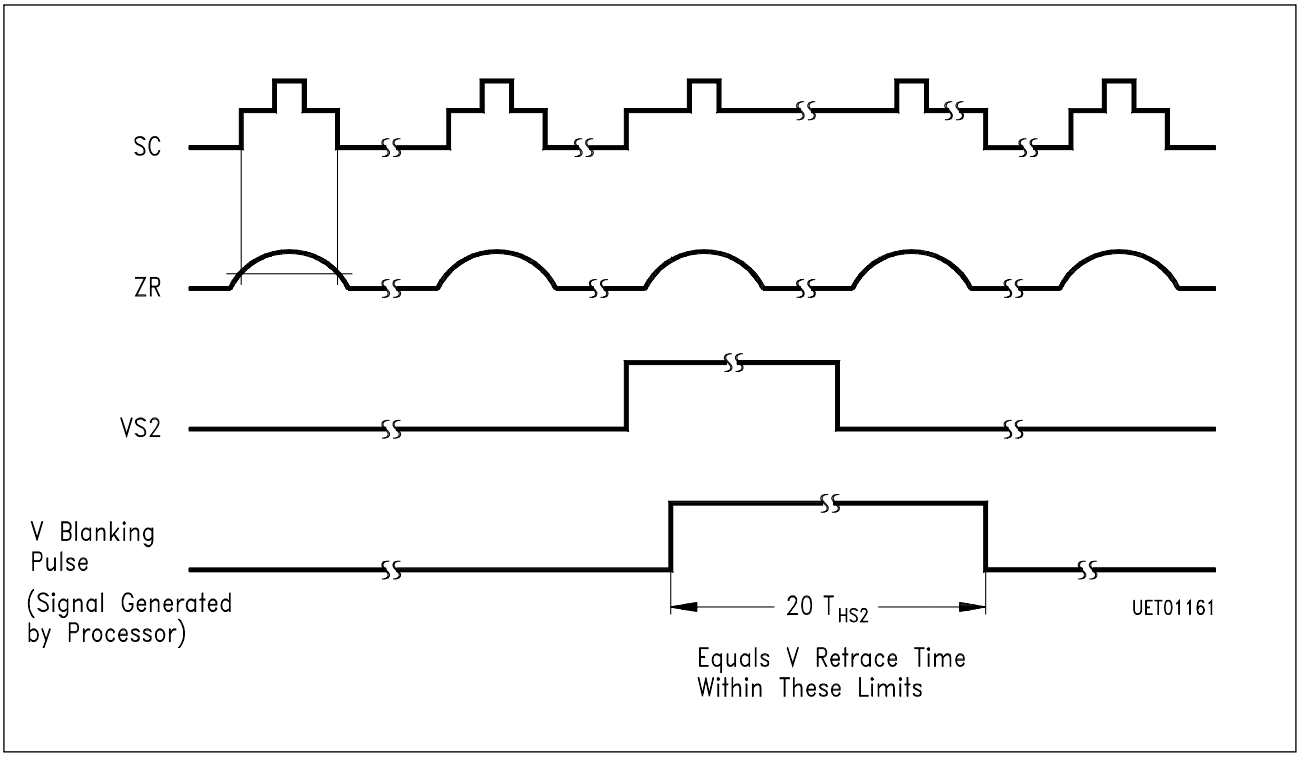


Test Circuit 23
L Level of I²C0

Set output I²C0 to low using the I²C Bus (or switch IC ON and OFF). Set the voltage on ammeter so that the current specified in the characteristics flows into output I²C0. Read off L level at I²C0. Connect all other pins as shown in **test circuit 1**.
This measuring circuit can also be used for output I²C1.



DDC SDA 9064-5 Behavior with H-Start-Up Circuitry and Driving of the H-Output Stage during Switch-ON/OFF and Operating Voltage Glitch



Interrelation of SC, ZR and VS2