The Digital Display Processor SDA 9280 with Integrated 9-Bit Triple D/A Converter for Enhanced TV Applications

Abstract

The described single IC performs processing and a 9-bit DA conversion of video component signals. It accepts multiple input data formats and improves picture quality by luminance peaking filtering, digital chrominance transition improvement and oversampling techniques. Display format control (4:3, 16:9, …) is realized by time compression or expansion.

Summary

Cost-reduction of TV systems by reduction of the analog application requirements, coupled with an improvement of the picture quality can be achieved by extended digital signal processing. Some of this DSP possibilities, being combined with on-chip D/A conversion have been implemented in the presented display processor in a 1-µm CMOS technology with two layer metallization. The chip has an area of 50.17 mm^2, containing 179397 transistors. Most of the used registers are of a dynamic 8-transistor type. The IC is completely controlled by I^2C Bus.

The possible input data formats are 4:1:1, 4:2:2 parallel, CCIR 656 and 4:4:4 with 8-bit word length. The maximal input clock frequency is 30 MHz. For internal processing the chrominance data of other formats are interpolated to the 4:4:4 parallel format by two interpolation filters (interpolator 1). Each filter performs a two fold oversampling.

A luminance peaking filter improves the over all frequency response of the luminance channel. It consists of three filters working in parallel. They have lowpass, bandpass and highpass characteristics and are separately programmable. An amplification of up to 14 dB at the half of the sample frequency is available.

A new digital algorithm has been implemented to improve transitions of the chrominance signals, resulting in a better picture sharpness. A slow change from one color to another because of small chrominance bandwidth is replaced by a steep transition. Two bandwidth optimized paths are implemented to detect the position of a color transition in the incoming chrominance signals. The better suited path is chosen automatically. The sensitivity of this Digital Color Transition Improvement (DCTI) circuit is programmable.

A compander for time-compression or time-expansion enables a display of signals having different display formats with correct geometric proportions, e.g. 4:3 signals on 16:9 screens or 16:9 signals on 4:3 screens. The horizontal compression or expansion of the video signals is performed by raising or reducing the sample frequency. The data is written into a memory using the system clock and read with a clock of higher or lower frequency. The compander is a FIFO memory with a storage capacity of 28 x 188 = 5264 bits implemented as a two-pointer controlled DRAM with dynamic three-transistor memory cells. The operation frequency of the compander is reduced to maximal 10 MHz by 4-bit parallel-conversion of the serial input write data and parallel-serial-conversion of the output read data.

A two fold oversampling filter (interpolator 2) transforms the internal used data format 4:4:4 to 8:8:8 before DA conversion in order to reduce the requirements for external analog postfiltering. A pipelined carry save architecture is used for the digital filter. Carry-select Vector Merging Adders (VMA) add the sum and carry word vectors for each sample. The filter is of a halfband type. A two phase processing structure is realized. The filter consists of a simple delay path and a filter path, both working at half the oversampling frequency. The output samples are taken alternating from the delay path and the filter path. The interpolator 2 has a steep transition at half the sampling frequency, an out of band rejection of more than 30 dB, a flat frequency response in the pass band and low overshooting in the time domain. The maximal output clock frequency is 80 MHz.

Three different values can be inserted into the video signal: black level, a colored background area and an arbitrary colored pattern. All insertions are performed after oversampling resulting in sharp transitions without overshooting.

To avoid a deterioration of the signal-to-noise ratio caused by word length reduction a first order noise shaper is implemented before D/A conversion.

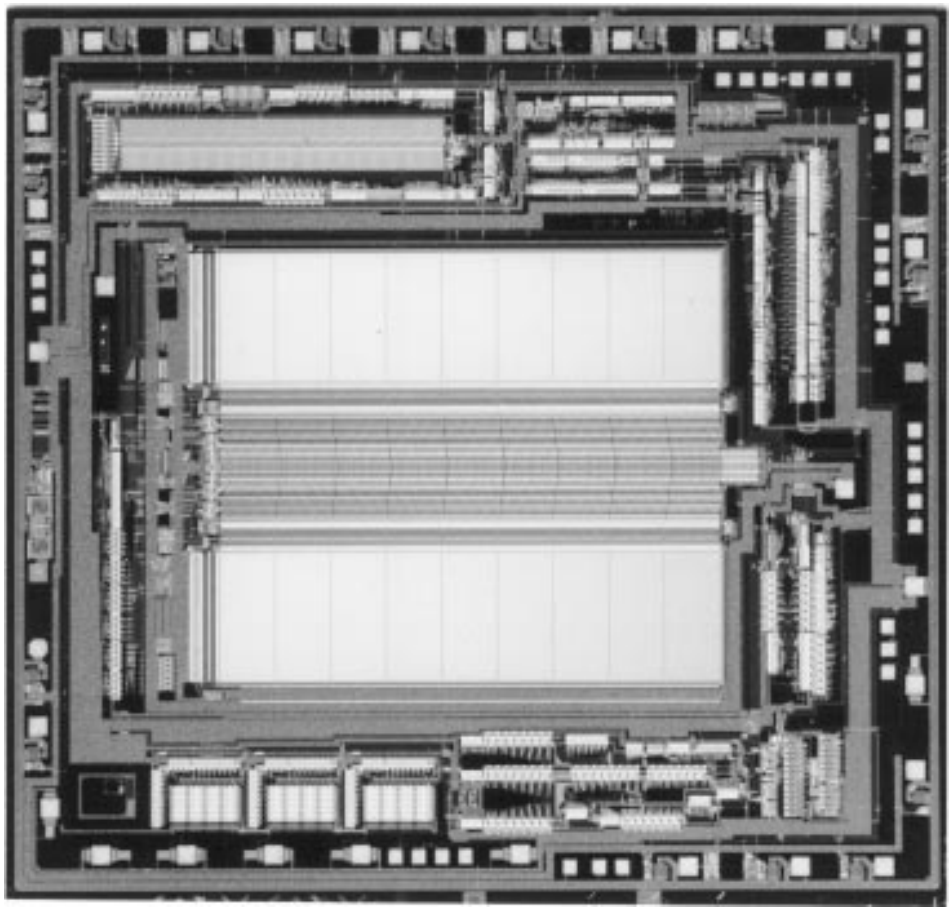
The architecture of the triple D/A converter has been chosen to be a mixture of binary weighted current cells and monotonic decoding of unity cells: The 5 MSBs are created in a linear array of 31 unit cells delivering a 16 x LSB current. The 4 LSBs are added as binary weighted current sources.

The measurements of the triple D/A converter show a total linearity error of less than 0.5 LSB and a S/N ratio of 50 dB (rms-rms) in a 25-MHz band, at an analog frequency of 12 MHz and a operation frequency of 108 MHz.

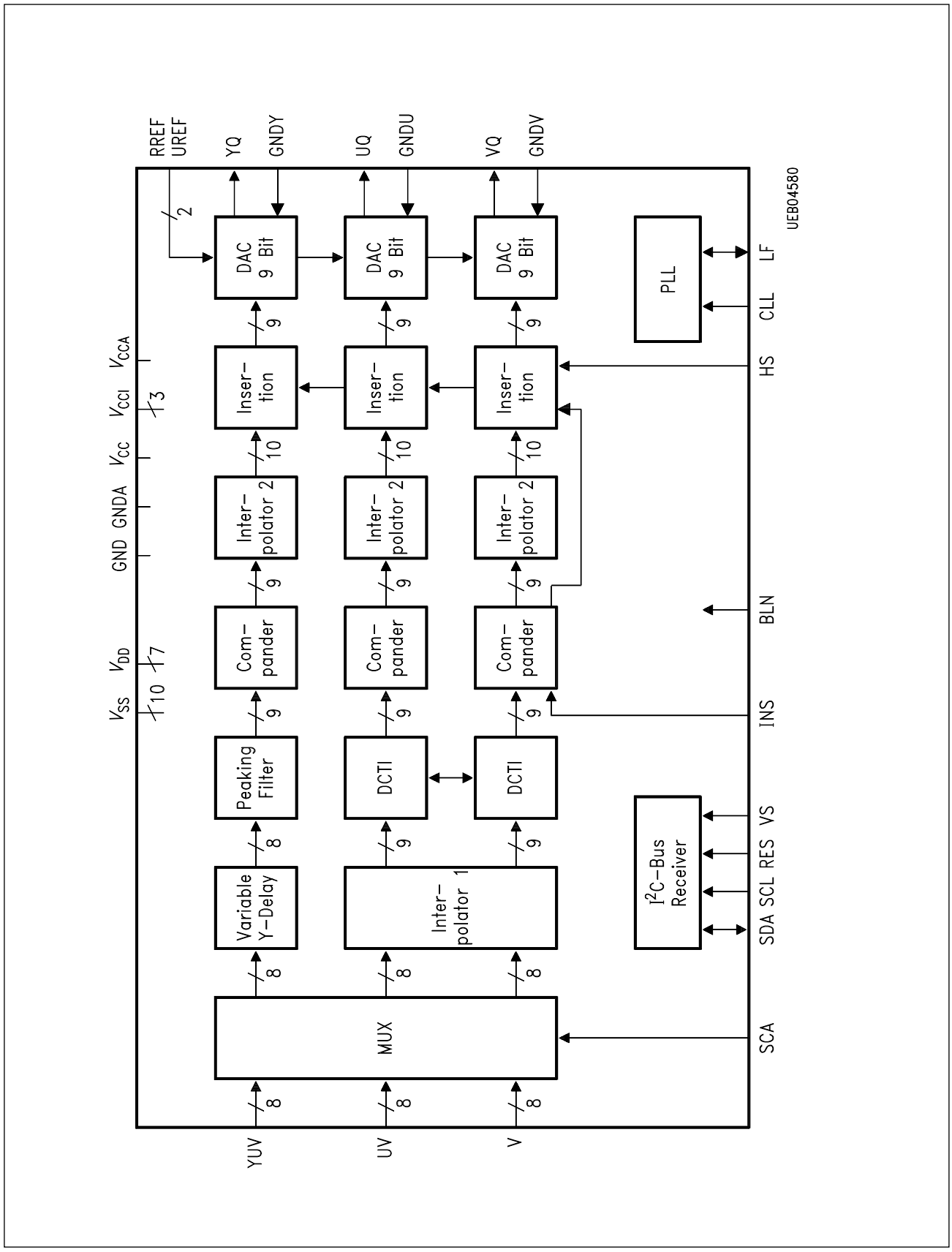
An internal PLL supplies the clock signals needed for all operation modes. It is designed with a differential 5-stage ring oscillator (VCO), a digital type-4 phase detector providing short anti backlash impulses and a single-ended external loop filter. The output frequency of the PLL is programmable in a wide range.

The clock system is divided into six subsystems, each generating a four-phase non-overlapping clock. Two subsystems are used for the synchronization of the input data. The demultiplexing of the various input data formats especially for 'zoom'-mode applications raise the necessity of the third clock subsystem. The further clock systems are used for the system clock, the compander reading clock and the oversampling clock.

All functions have been verified with oversampling clock frequencies in excess 108 MHz at typical operation conditions.



Chip Microphotograph



Block Diagram