SDA 9257: A Generator Chip as Frequency Synthesizer for TV Applications

Color TV sets with the Siemens Featurebox are notable for their flicker-free picture and convenient functions such as frame freeze picture-in-picture, 9-in-1 picture and noise reduction. Following development of the SDA 9205-2 triple A/D converter and SDA 9257 clock sync generator, television sets with analog processing of the video signal can now enjoy all the advantages of the digital Featurebox. The SDA 9257 can also be used as a general purpose video pulse generator and frequency synthesizer.

Using the clock sync generator (CSG), the triple ADC and an analog color decoder (e.g. TDA 4555), analog TV frontends can now be designed that produce all the picture signals, sync pulses and clock pulses required by the Featurebox (**figure 1**). The CSG works with all standards for composite video blanking signals (CVBS), such as 50 Hz, 60 Hz, PAL, NTSC and SECAM, and is optimized in its clock and sync generation for different TV and VCR sources.

Frequency Synthesizer

Used as a frequency synthesizer, the CSG generates frequencies between approximately 10.3 and 37.7 MHz at its clock outputs. The required frequency can be set in very fine increments by a 16-bit value on the I^2C Bus and can also be crystal-controlled with an external crystal as a reference (**figure 2**).

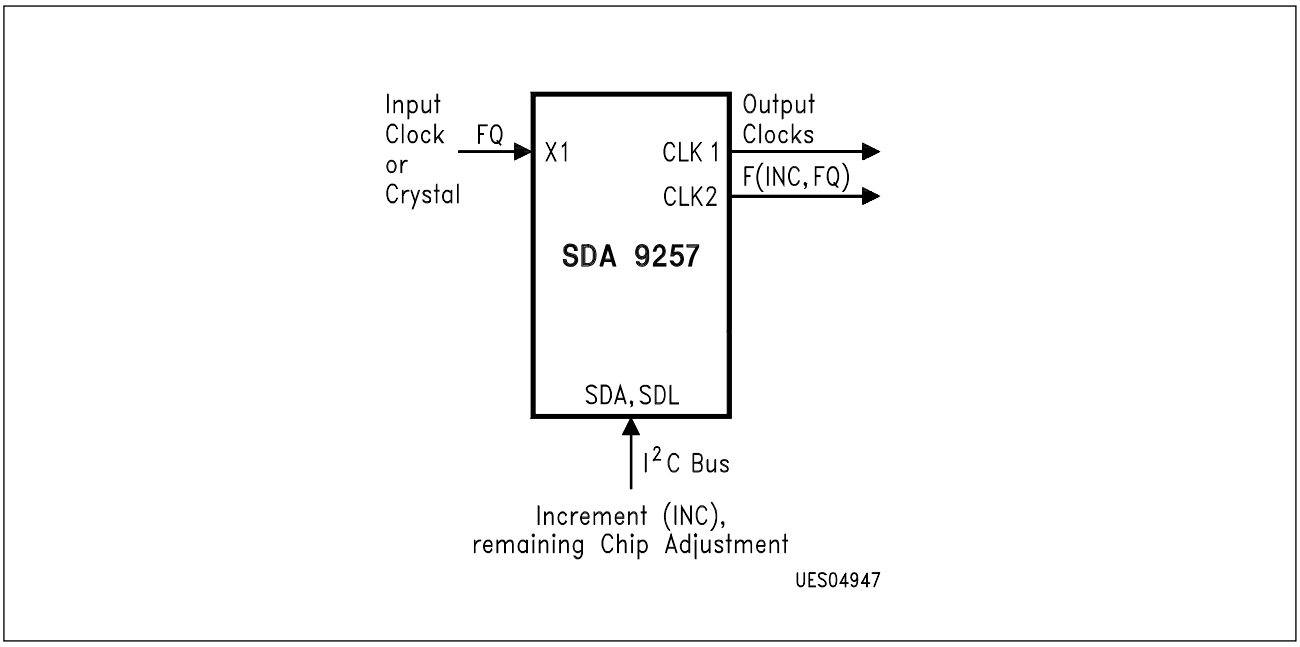

Figure 1
Featurebox Environment with Analog Color Decoder

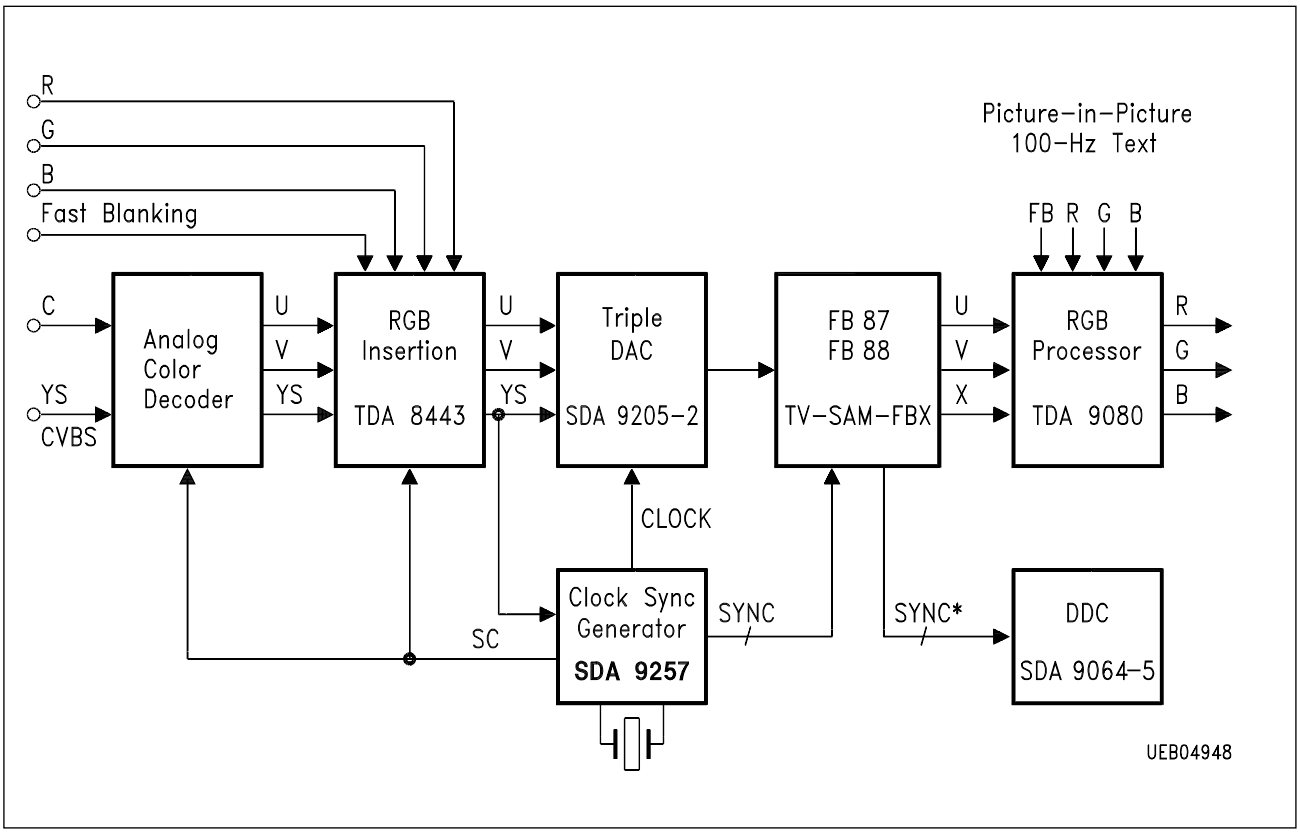

Figure 2
Clock Sync Generator (CSG) as Frequency Synthesizer

Automatic Clamping

The CVBS-input signal can be clamped by the CSG automatically. If a video signal multiplexer heads the circuit, clamping will be made there and the CSG provides the multiplexer with the necessary clamping pulses. The CSG can also be supplied with a sync or a YS signal; the clamping then has to be disabled. By means of clamping, the CVBS signal with an unknown DC component is shifted in its DC position so that its sync signal component is within the driving range of the internal A/D converter and the horizontal PLL (HPLL) can securely lock onto the H pulses.

The clamping algorithm covers four phases and is started by the power-on:

- Phase 1: A transistor switch clamps the CVBS to the lower ADC-reference voltage of 0 V for the duration of six TV lines.
- Phase 2: A transistor switch then clamps the CVBS to 5 V every time the underflow bit of the ADC appears for longer than 1.1 µs. Following this phase it is certain that a major part of the sync signal component is within the driving range of the ADC.

From phase 3 onward, a constant check is made to ensure that the CVBS goes below the mean value of the ADC-driving range at least once per line. If not, clamping phase 1 is started again. Underflow is also monitored: if the CVBS goes below the lower ADC-driving limit by more than 0.1 V and for longer than 1.1 µs, a switch briefly clamps to 5 V.

- Phase 3: The switch clamps to 0 V with a pulse that lags approx. 1 µs behind the H-sync leading edge.

Phase 4 is initiated and maintained when the HPLL is locked to the CVBS for better than approx. 600 ns.

- Phase 4: The switch clamps to 0 V with a pulse coupled direct to the HPLL that appears in the first half of the H-sync pulse.

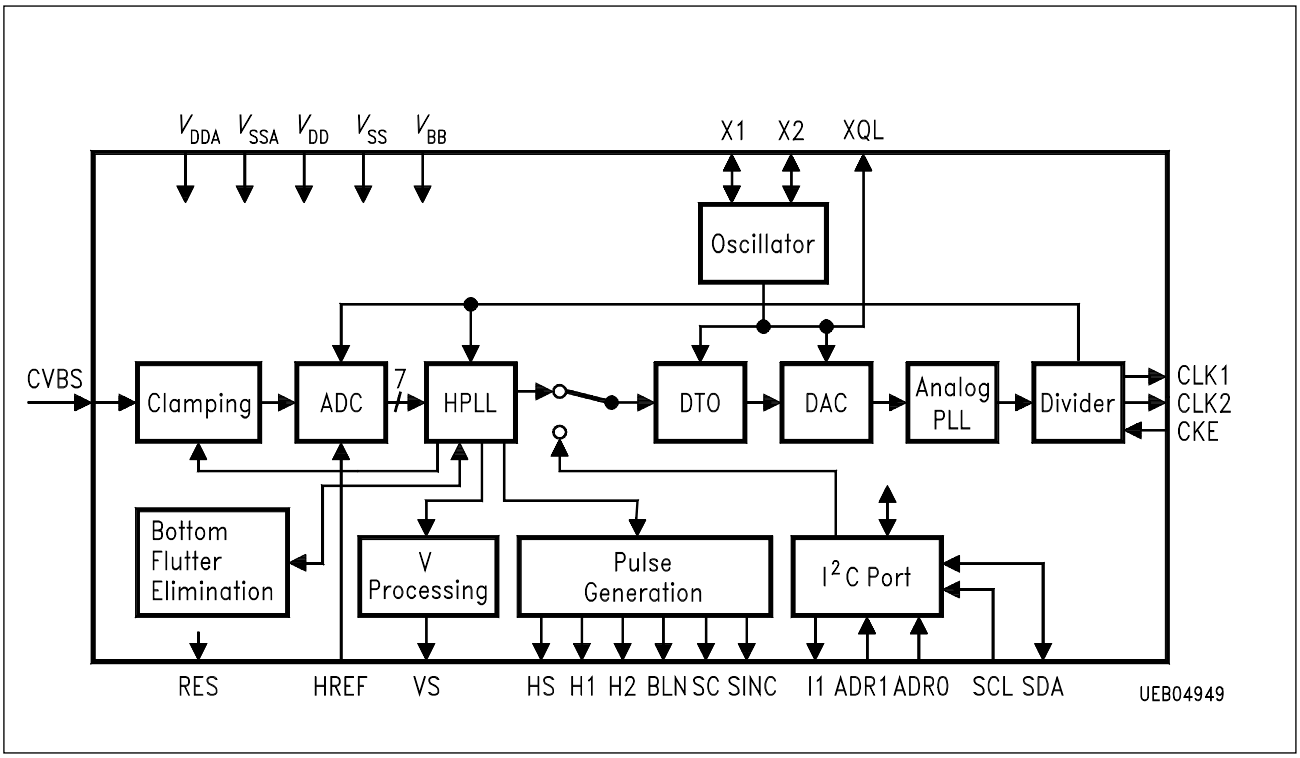

Figure 3
Block Diagram of Clock Sync Generator

Clock Generation

Clock generation basically consists of three parts (**figure 3**):

- The digital horizontal phase-locked loop (HPLL) generates a digital value that is proportional to the frequency of the clock line-locked to the CVBS.
- By means of a discrete timing oscillator (DTO) followed by a sine coder and DAC, a line-locked clock signal is produced whose frequency is a quarter of the output clock frequency.
- An analog PLL quadruples this frequency and minimizes the jitter.

This configuration enables separate optimization of the lock-in response and clock jitter.

Horizontal Phase-Locked Loop

Figure 4 illustrates the HPLL. After the CVBS has been A/D-converted with 7 bits resolution and 27 MHz, there follows an FIR lowpass filter with a cutoff frequency of 1 MHz to improve the SNR, eliminate the chroma component and produce defined edge steepness of the sync pulses (which is necessary for accurate digital measurement of the phase difference). Subtraction of the black level in the sync slicer leaves just the sync signal component of the CVBS at the output of the amplitude separator.

Comparison of the position of the sync edges with the pixel counter, which represents the phase of the HPLL, provides a rough value for the phase difference. Integration of the sync edge during a window defined by the pixel counter produces a precise value for the phase difference if the HPLL is already phased in accurately enough.

The phase difference is applied to a non-linear PI filter, whose coefficients are determined both by the instantaneous phase difference and by the mode (TV or VCR) set on the I²C Bus. The output of the PI loop filter is the increment of a discrete timing oscillator (DTO) and thus determines the clock frequency of the chip and the device outputs.

The momentary black level and sync level are constantly measured on the digital sync signal. The method of measurement is different for large and small phase differences. The value measured for the black level is fed to the black-level control. This produces the black level that is subtracted from the digitized CVBS in the sync slicer. From the black level and the measured sync signal, the threshold control forms a sync cutoff threshold with the aid of which coarse measurement of phase difference is made and the vertical pulse is separated.

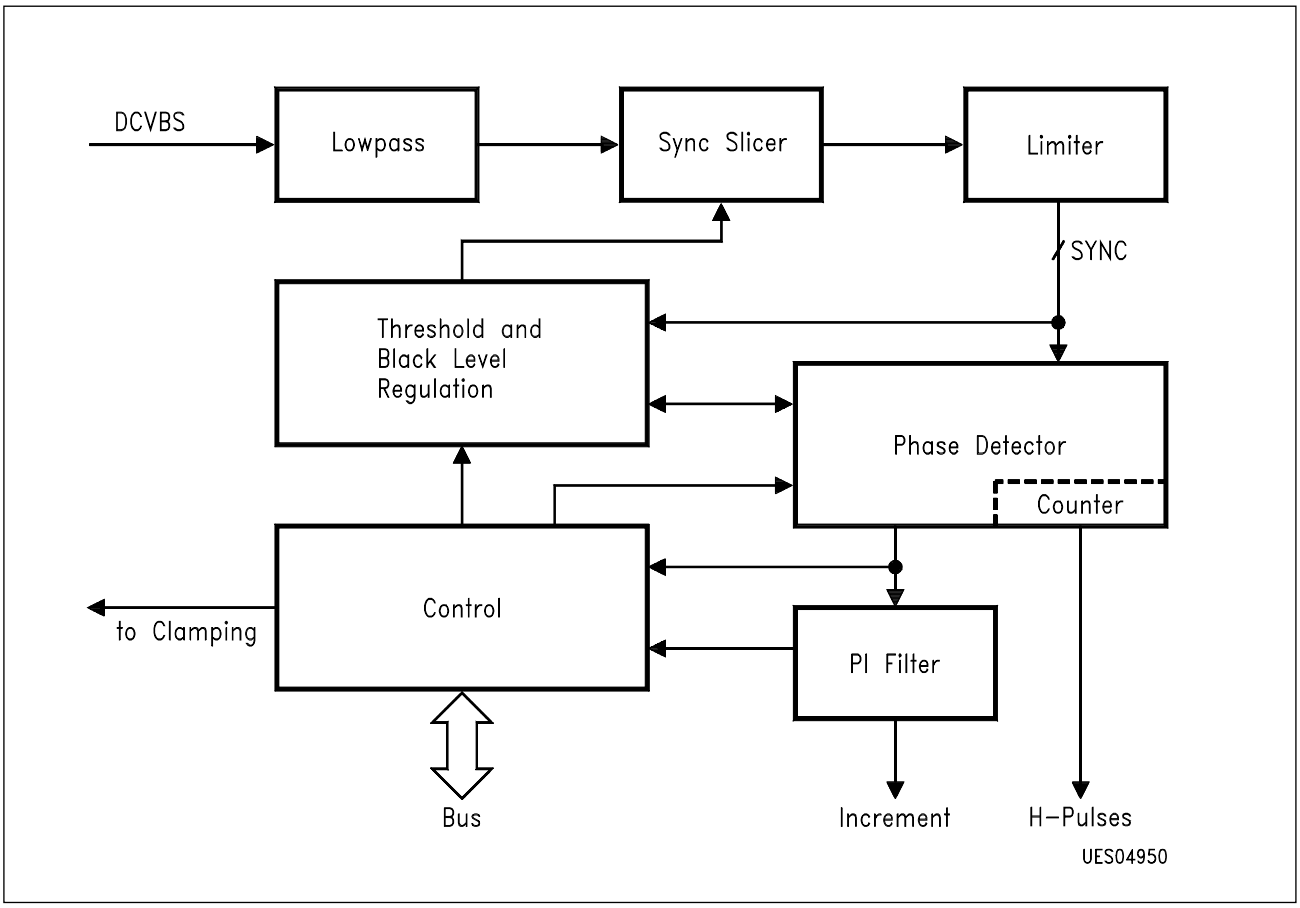

Figure 4
The Digital Horizontal PLL Generates a Digital Value

If the digital sync signal in the HPLL goes below the sync cutoff threshold, a counter is incremented; otherwise it is decremented. The reading of the counter is thus a measure of the length of the sync pulse. During the first main tail of the vertical blanking interval, the counter exceeds a given value and thus detects a vertical pulse in the CVBS. This kind of vertical pulse separation is largely the same as the analog principle. This pulse goes to vertical sync processing.

If there is no CVBS on the input of the CSG, the HPLL will ensure that the clock frequency is set to the nominal value. This makes sure in the TV set that the high voltage for the tube generated by the CSG pulses will not increase.

Discrete Timing Oscillator

The DTO (**figure 5**), consisting of an adder and a register with crystal-referenced timing, generates a sawtooth signal with a frequency proportional to the value of the increment and the crystal frequency. After recoding in a ROM, D/A conversion and bandpass filtering, the result is a sinusoidal analog signal that is converted into a clock signal in the Schmitt Trigger (ST). This clock frequency is only a quarter of the device output clock frequency so that the sampling theorem is fulfilled, but not with too high a crystal frequency (sampling frequency).

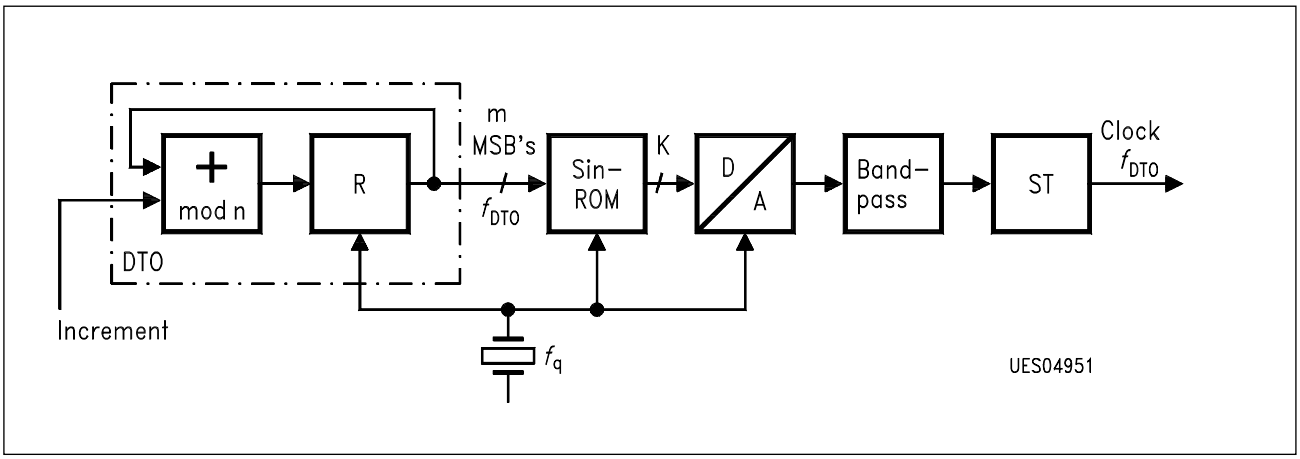

Figure 5
The Discrete Timing Oscillator Consists of an Adder and Register; it Generates a Sawtooth Signal

Analog Phase-Locked Loop

The analog PLL quadruples the frequency. Appropriate selection of the attenuation and natural frequency produces a marked reduction in high-frequency clock jitter, regardless of the low-frequency transient response (and jitter) of the HPLL. Furthermore, the resistances and capacitances of the analog loop filter are low and can therefore be integrated.

Vertical Sync Processing

Vertical sync processing detects the lines per field and reduces interference of the vertical pulse.

The line count, using the vertical pulse separated from the CVBS in the HPLL, first detects whether the line number per field is greater or smaller than 287. By means of different settings of a measuring window (wide or narrow) on the I^2C Bus, four ranges can be identified for the line count, and these can also be read out via the I^2C Bus. Integrated averaging and hysteresis ensure that these ranges are properly detected even when VCR signals fluctuate in their line count or broadcast signals are affected by heavy noise.

The line count also produces (on the I^2C Bus) a field bit. This toggles on each change of field, but it is always set to 0 when the separated vertical pulse appears within the first half of the line and also within the selected window when the vertical interference reduction is activated. In other words, this bit is always 0 during the first field.

When the vertical line interference reduction is activated, the vertical pulse from the HPLL is only allowed to pass within the selected window and appears as a pulse on the VS output of the device. Two different window widths (optimized for VCR and broadcast signals) can be set for 525-line or 625-line standards.

In the occasional absence of vertical pulses from the HPLL, a VS pulse is triggered at the latest after 340 or 288 lines. If a “flywheel” is also activated, missing V pulses are continuously added every 312.5 or 262.5 lines. The VS pulse can also be generated in a free wheeling manner, i.e. independent of the CVBS input, and for both 312.5 and 262.5 lines per field.

In what is called terminal mode, free-wheeling generation of the VS takes place with 312.0 or 262.0 lines per field. So if the CVBS contains a lot of noise, missing V pulses can be added by activating the flywheel and V-interference pulses can blanked by activating the interference reduction. Each of these can be activated independently of the other.

Bottom Flutter Elimination

The momentary frequency of the output clock pulses can be frozen in a line band about the vertical blanking interval to suppress bottom flutter in VCR mode. The beginning of the band before the V pulse and its duration can be set on the I^2C Bus.

Pulse Generation

The CSG supplies different sync pulses generated with the aid of the pixel counter in the HPLL. So these have clock-synchronized edges and are free of horizontal interference.

- The position of the horizontal pulse HS can be set across the entire line by means of the I^2C Bus, and the position of the H1 and H2 pulses can be set in a suitable band about the line blanking interval. As H1 and H2 can be used for external clamping, their width is also adjustable.
- In the case of the sandcastle or super-sand-castle pulse (depending on the pin function selected), there is no burst key. This has to be inserted externally because of its 11-V Ievel. For this purpose, the inverted burst pulse is available on a further pin. The location of the sandcastle and burst pulse, which are in a fixed relation, is adjustable.
- The composite sync pulse is derived directly from the filtered CVBS by means of the sync cutoff threshold formed in the HPLL. This calls for a CVBS input signal and cannot be varied in position.
- The blanking signal BLN for the Featurebox can be adjusted in position and width.

Abbreviations

ADC	Analog/Digital Converter
CVBS	Composite Video Blanking Signal
CSG	Clock Sync Generator
DAC	Digital/Analog Converter
DDC	Digital Deflection Controller
DTO	Discrete Timing Oscillator
FB, FBX	Featurebox
HPLL	Horizontal PLL
I^2C Bus	Serial data bus for entertainment electronics
MUX	Multiplexer
NTSC	National Television System Committee (US standard)
PAL	Phase Alternating Line (German standard)
PLL	Phase-Locked Loop
RGB	Red, Green, Blue component signals
ROM	Read-Only Memory
SECAM	Séquentielle Couleur A Mémoire (French Standard)
SNR	Signal/Noise Ratio
ST	Schmitt Trigger
VS	Vertical Sync pulse

References

[1] Hass, M.; Draxelmayr, D.; Kuttner, F.; Zojer, B.: A Monolithic Triple 8-Bit CMOS Video Coder. IEEE Transactions of Consumer Electronics, Vol. 36, No. 3, August 1990

[6] Kramer, R.: Bus Controlled Clock Generator. IEEE Transactions of Consumer Electronics, Vol. 37, No. 3, August 1991