Application Note

Vakat

The High-Speed Triple A/D Converter SDA 9205-2 for Video Applications

From the Siemens microelectronics design center in Villach, Austria, comes the fastest triple ADC ever for video applications. This is the SDA 9205-2, a CMOS chip that integrates three 8-bit converters with a sampling rate of 30 MHz. Even for high-grade video signals, this high sampling frequency allows twofold oversampling, which, combined with the chip's internal digital filtering, simplifies external anti-alias filtering. Besides internal clamping, the converter offers a total of eight selectable sampling and output data formats for a variety of applications.

Outstanding features of the SDA 9205-2 are its superior signal-to-noise ratio of typically 46 dB and excellent linearity. Its primary application is image processing in video equipment of every kind, such as TVs, video recorders, video printers, multimedia PCs and studio equipment. The many functions which this innovative chip can handle are explained below as application support for the prospective user.

Scope of Application

The SDA 9205-2 was designed for volume applications that call for high performance at low cost. A major application is in flicker-free TV sets. TVs of this kind, working at 100 Hz, use a digital picture memory to double the field frequency. In other words, digitization of the video signals is essential. The same applies to all kinds of TVs with a 16:9 aspect ratio. If the usual 4:3 pictures are to be presented on a 16:9 tube in the correct aspect ratio, they must be compressed horizontally by a factor of 4/3. This is best done with the aid of a digital line memory.

Figure 1 shows the basic configuration of a typical image memory application with an SDA 9205-2 at the front end.

If recordings are copied from one video recorder to another, digital timebase correction can improve picture quality quite appreciably. Here, too, image memory systems are used, requiring a triple analog/digital converter.

There are further applications in digital video processing, in TV-studio equipment (mixing and switching images from different cameras), in video printers and video telephones.

Conventional electronic photography (still video) mainly uses magnetic recording media to store single pictures in analog form. But systems have already been unveiled that work digitally with RAM-chip cards, permitting substantially higher picture quality. As soon as memory ICs of a sufficiently high level of integration become available to put these memory cards within the reach of consumers, a new mass market can be expected to emerge.

Last but not least, there is the personal computer. Here so-called frame grabbers, which digitize frames into stills and enable them to be processed further in a PC, have been in use for some time. This can be seen as a preliminary to multimedia systems, which will also be able to process full-motion video sequences including sound.

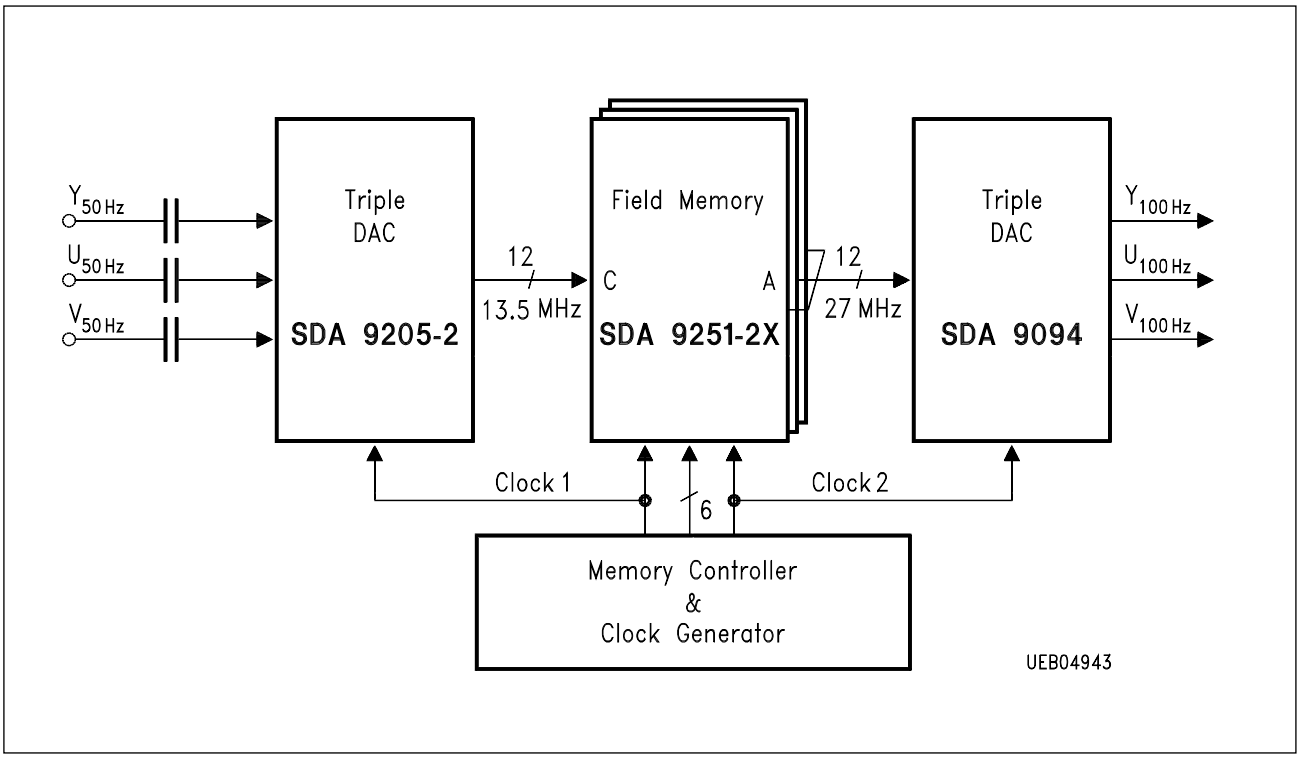

Figure 1
Typical Application in an Image Memory System

Technology of the SDA 9205-2

Figure 2 shows a block diagram of the triple analog/digital converter, consisting of three two-step flash converters with integrated clamping, a signal processor, output coding and output drivers. The SDA 9205-2 was developed in 1 µm CMOS technology with two metalization layers. The indisputable advantage of CMOS technology over much faster bipolar technology is that it can also integrate extensive logic components, thus saving current and space. The SDA 9205-2 makes full use of this capability.

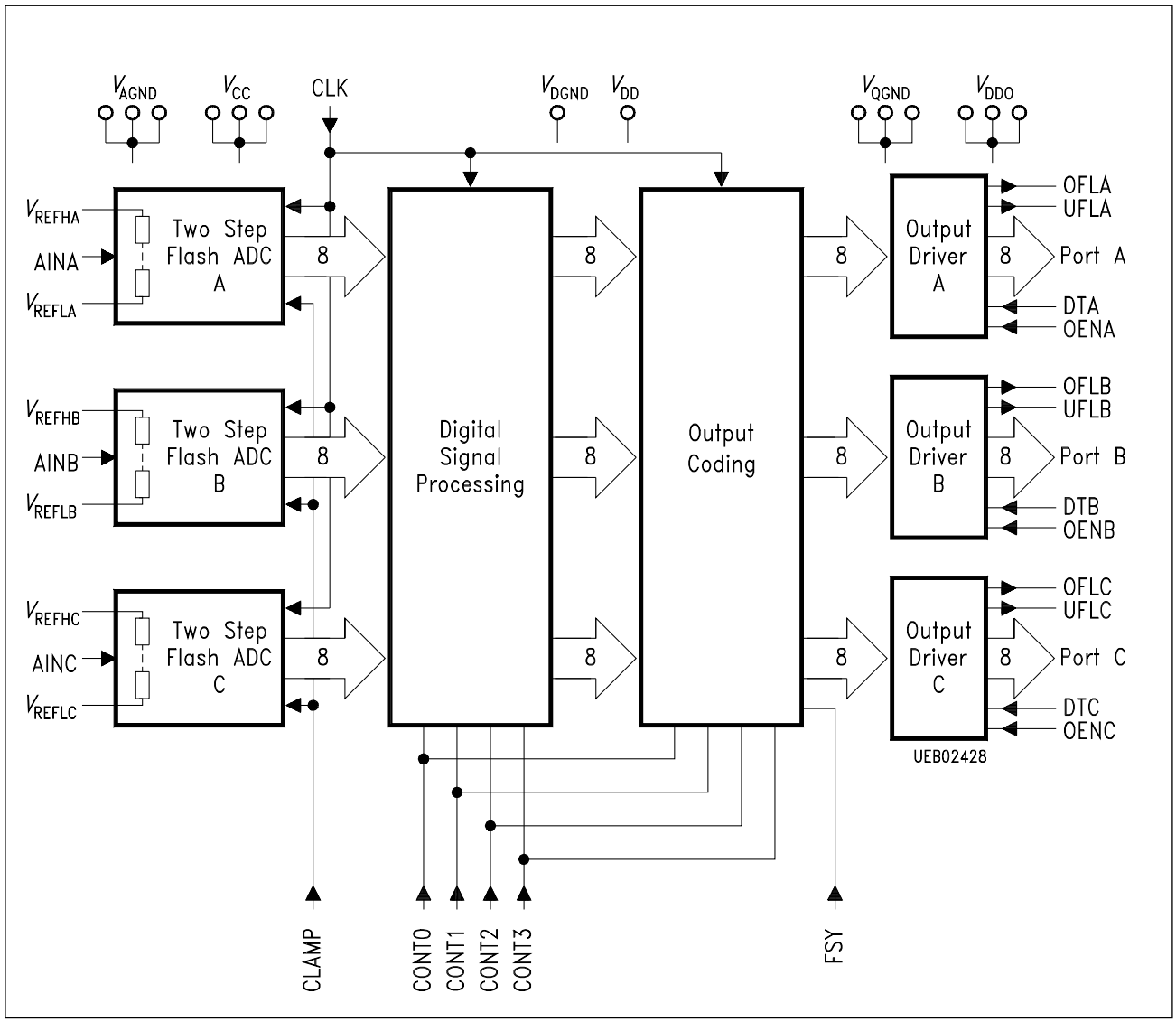

Figure 2
Block Diagram of Triple ADC SDA 9205-2

Converter Section

The principle of the converter is explained in detail in [1]. To ensure optimal clamping, the converter stages include input buffer amplifiers that produce both high input impedance and low input capacitance. The dynamic range can be adjusted separately within certain limits for all three converters by means of the reference voltage inputs. A reference voltage difference of 2 V produces a sensitivity of about 2 V for full drive. This value is advisable if a high signal/noise ratio and high linearity are called for. Although smaller values will in crease sensitivity, it should be noted that small input voltages are always more difficult to protect against interference picked up from other parts of the equipment. The simplest solution is to feed all converters from the same reference voltage sources.

The main purpose of clamping is make sure that the DC component can be reconstructed at any time despite capacitive coupling of the video signals. Any video signal more or less conforming to standard in the line-blanking interval – invisible on the screen – contains a range that is defined as its black level (porch). During the black-level phase of a few microseconds after capacitive coupling, the coupling capacitor is initially charged by means of a switch and a current source so that the signal's inherent black level reaches the standard level. In the SDA 9205-2, the standard level has the digital values specified by CCIR Recommendation 601 of 16 for Y, and 0 for U and V. Initial charging of the coupling capacitor is digitally controlled so that these standard values are produced to within one least significant bit (LSB). Once the video signal is digitized, its DC level is no longer important and the black level can be ignored. For image storage systems in particular, this means that the blanking intervals of the picture with the black level do not have to be stored. The black level is not coupled in again until just before digital/analog conversion (e.g. during the entire blanking interval) to avoid problems in the following analog stages. The clamping pulse is applied externally to match the timing of the black level, and its duration (positive polarity) should be at least about 1 µs so that a steady state is reached faster.

The only differences between the three converter stages are in the firmly programmed clamping value 16 (binary) for converter A, which is provided for the luminance signal (Y), and 0 (two's complement) for converters B (chrominance component U or -[B-Y]) and C (chrominance component V or -[R-Y]).

Signal Processor

In the signal-processor block, the three 8-bit output data streams of the converters are subjected to independent digital filtering and decimation (i.e. subsampling), which can be activated separately for channel A and channel B/C. The following functions are available:

$\alpha[n] = a[n-3]$ (1.0)

$\alpha[n] = (a[n-4] + a[n-3])/2$ (1.1)

$\beta[n] = b[n-3)$ (2.0)

$\gamma[n] = c[n-3]$

$\beta[n] = (b[n-4] + b[n-3])/2$ (2.1)

$\gamma[n] = (c[n-4] + c[n-3])/2$

$\beta[4n] = (b[4n-5] + b[4n-4] + b[4n-3] + b[4n-2])/4$ (2.2)

$\beta[4n-1]$, $\beta[4n-2]$, $\beta[4n-3]$ arbitrary

$\gamma[4n] = (c[4n-5] + c[4n-4] + c[4n-3] + c[4n-2])/4$

$\gamma[4n-1]$, $\gamma[4n-2]$, $\gamma[4n-3]$ arbitrary

$\beta[8n] = (b[8n-7] + b[8n-6] + \ldots b[8n])/8$ (2.3)

$\beta[8n-1]$, $\beta[8n-2]$ … $\beta[8n-7]$ arbitrary

$\gamma[8n] = (c[8n-7] + c[8n-6] + \ldots c[8n])/8$

$\gamma[8n-1]$, $\gamma[8n-2]$ … $\gamma[8n-7]$ arbitrary

Here $\alpha[n]$, $\beta[n]$ and $\gamma[n]$ are the output signal values and $a[n]$, $b[n]$ and $c[n]$ the input signal values of the signal processor block at the instant n (n = integer). All operations are matched in delay with a constant group delay of 3.5 sampling clock pulses. Exact compensation is impossible only when filtering (1.0 and 2.0) is inactive; the group delay is then three clock pulses. But this is only of importance when filtered and unfiltered modes are mixed, and even then it can usually be neglected.

Modes 2.2 and 2.3 can only be activated together with appropriate decimation (then the values shown as “arbitrary” are omitted). So a decimated data point is clearly composed of the arithmetic mean of four or eight input data values.

The digital filter operations can be characterized by a typical periodic frequency response for discrete signals which, in the range between 0 and half the sampling frequency, corresponds to what is usually understood by frequency response. With the exception of the phase term from the group delay, the mathematical form is given by

(1.1, 2.1) $H(f) = \sin(2\pi f/f_S)/(2\sin[\pi f/f_S])$

$= \cos(\pi f/f_S)$

(2.2) $H(f) = \sin(4\pi f/f_S)/(4\sin[\pi f/f_S])$

(2.3) $H(f) = \sin(8\pi f/f_S)/(8\sin[\pi f/f_S])$

Here f_S is the input sampling frequency given by the clock frequency. **Figure 3** is a graphic representation of these frequency responses. After subsampling (decimation) by factors of 2, 4 or 8, the frequencies between 0 and $f_S/4$, $f_S/8$ and $f_S/16$ describe the new useful ranges. Experts will notice immediately that anti-aliasing is particularly good in the range of multiples of the input sampling frequency, so unpleasant low-frequency alias interference in video signals is effectively avoided.

The digital filters intended for anti-alias filtering were deliberately kept simple for two reasons. First, many signals are already limited in bandwidth and consequently require no further filtering if the sampling frequency is chosen correctly. Second, the integrated digital filter simplifies external analog filtering quite considerably for signals that are not limited in bandwidth, and does so without generating overshoot or similar artifacts. So extra filtering can often be dispensed with in these cases as well. The impression produced by the picture is the final arbiter. Multiburst test patterns and sharp vertical edges are especially critical. Filters for video require optimization criteria quite different to those for audio, where the object is to obtain as flat a frequency response as possible.

To demonstrate this, a broadband text and graphic image was alternately sampled at 27 MHz

- without filtering,
- with high-order analog filtering (cutoff frequencies 6.75/1.6875/1.6875 MHz for Y/U/V) but without digital filtering, and
- without analog filtering but with the integrated digital filters. The image was then decimated to 4:1:1 format.

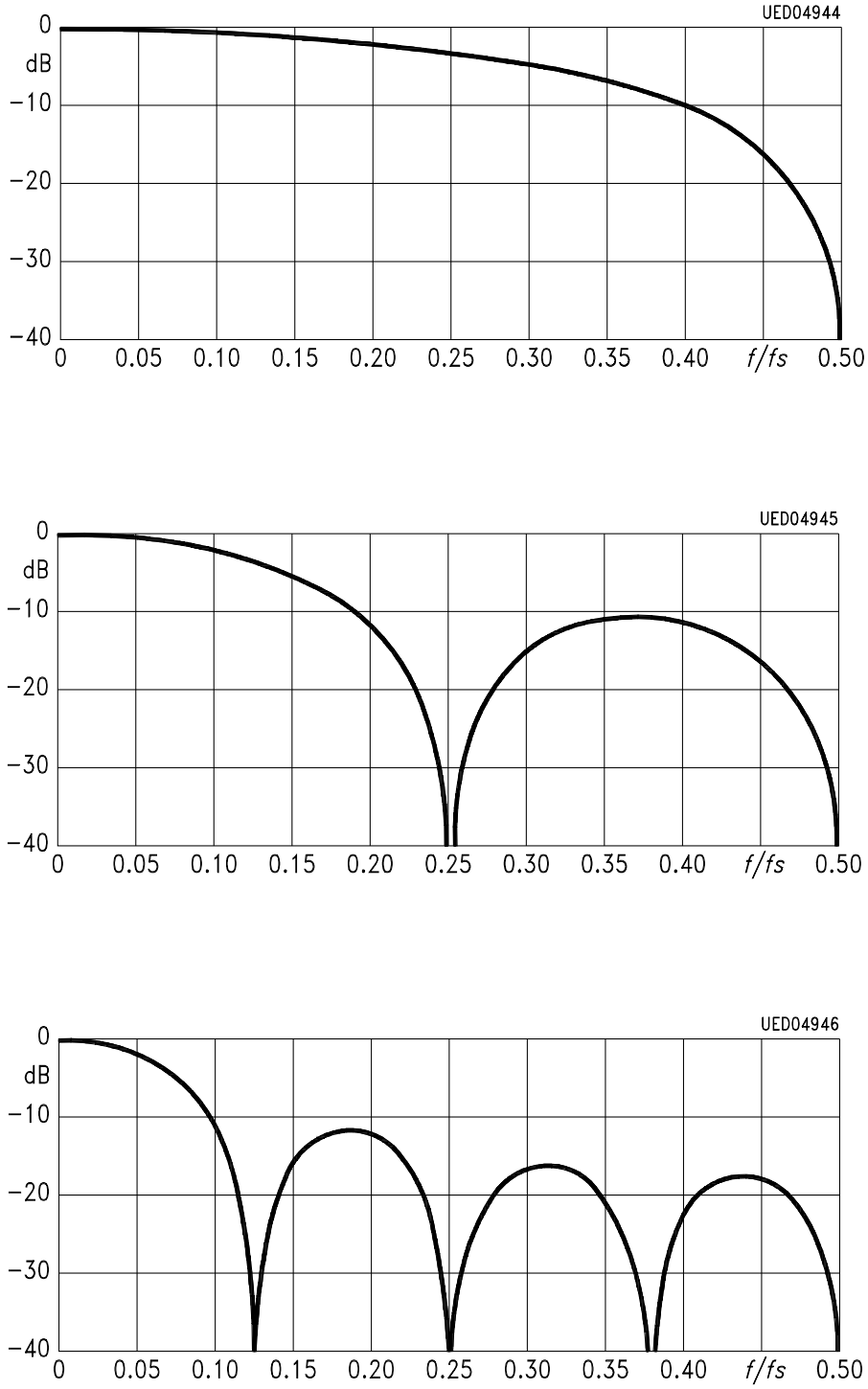

Figure 3
Standard Frequency Responses of Integrated Digital Filters 1.1/1.2, 2.2 and 2.3
Horizontal: Normalized Frequency f/f_S from 0 to Half Sampling Frequency (f_S = sampling frequency)
Vertical: Logarithmic Frequency Response in dB

The results left no room for doubt: clear artifacts were visible without any filtering at all, i.e. fine color traces were either much too wide or completely absent, depending on the arbitrary sampling phase. The analog-filtered image, as expected for 4:1:1, was somewhat more blurred and also exhibited visible ringing effects (overshoot) next to edges, while the digitally filtered image made the best impression through the lack of ringing effects.

One cause of alias interference in originally band-limited signals, and one that should not be underestimated, is non-linearities in analog preprocessing, which generate harmonics and thus cancel the band limiting. If the harmonics are in the immediate vicinity of the sampling frequency or multiples of it, they can then show up as low-frequency picture interference or even as jitter.

A very important feature of the integrated digital filters is that their frequency response tracks the sampling frequency. This also applies to the zeros of the frequency response at the decimated sampling frequency (output sampling frequency) and its multiples. Both precise zeroes and adaptivity – cannot be achieved with analog anti-alias filters.

If high-frequency interference is expected at the ADC input, analog filtering is recommended which will not influence the signal component and is the same for all three inputs to avoid differences in propagation delay. Given twofold oversampling, the remainder can be left to the digital filters. In critical special purpose applications, the internal digital filter can be switched off and replaced by an external decimator, specified by the user, at the output of the SDA 9205-2.

Output Coding

The format of the output data as a function of the sampling format is determined in the coding block on control pins CONT0 to 3. Whereas filtering (1.1) and (2.1) can be set independently of subsequent decimation, filtering (2.2) and (2.3) can only be combined with the appropriate subsampling. In all cases, of course, decimation is also possible without digital filtering. The different subsampling formats are shown in **table 1**. The terms 8:8:8, 4:2:2, etc. are taken from TV studio conventions, where 4:2:2, for example, defines a sampling rate ratio of 13.5:6.75:6.75 MHz for the color components YUV. So 8:8:8 consequently defines a ratio of 27:27:27 MHz. For the converter itself, only the ratio is important, because the sampling frequency is not fixed at 27 MHz but may be between 1 and 30 MHz in all modes. 8:8:8 therefore means f_S:f_S:f_S and 4:1:1, to quote another example, is f_S/2:f_S/8:f_S/8. As the table clearly shows, CONT0 switches the digital files off or on, CONT1 and CONT2 determine the chrominance decimation factor, while CONT3 is responsible for luminance decimation.

Table 1
Output Sampling Format and Filtering as a Function of Control Signals CONT0-3

Format	Filtering	CONT3	CONT2	CONT1	CONT0
8:8:8	1.0 + 2.0 1.1 + 2.1	0 0	0 0	0 0	0 1
8:4:4	1.0 + 2.0 1.1 + 2.1	0 0	0 0	1 1	0 1
8:2:2	1.0 + 2.0 1.1 + 2.2	0 0	1 1	0 0	0 1
8:1:1	1.0 + 2.0 1.1 + 2.3	0 0	1 1	1 1	0 1
4:8:8	1.0 + 2.0 1.1 + 2.1	1 1	0 0	0 0	0 1
4:4:4	1.0 + 2.0 1.1 + 2.1	1 1	0 0	1 1	0 1
4:2:2	1.0 + 2.0 1.1 + 2.2	1 1	1 1	1 1	0 1
4:1:1	1.0 + 2.0 1.1 + 2.1	0 0	0 0	0 0	0 1

It would go beyond the scope of this article to describe all output data formulas in full; details can be obtained from the SDA 9205-2 data sheet [2]. The major formats are the parallel format for 8:8:8 and 4:4:4 with 3 x 8 bits each, the semiparallel format for 8:4:4 and 4:2:2 with 8 bits for Y and 8 bits alternating in time for U and V, and the multiplex format for 8:2:2 and 4:1:1 with 8 bits for Y and U, V bit-serially on two lines each. The 4:8:8 format is a sort of by-product of the control-bit assignment and hardly likely to be of practical use.

The multiplex format is compatible with the Siemens Featurebox systems for digital television [3] and corresponds to the output format of the Philips digital color decoder SAA 9051. The 4:2:2 semiparallel format is supported by the new Siemens TV-SAM Featurebox. A special feature is the data format specified in CCIR 601/656, which is offered on the third output port in addition to the semiparallel format for 4:2:2. Here the three color components appear on eight lines one after the other in the sequence UYVY. The digital words 0 and 255 are intended for control functions as defined in CCIR 656, so corresponding signal values are mapped on 1 and 254. The data clock frequency in this case is twice the output sampling frequency for Y.

All sampling formats that contain a reduction of sampling rate require synchronization to determine the phase. For the SDA 9205-2, this synchronization is produced by the format sync control signal FSY. FSY is sampled with the chip clock; the first H level detected then defines the first output data word within a sequence. Basically, one-shot synchronization is enough, but it is advisable to repeat it at regular intervals so that the system will not be continuously out of sync if one-time errors occur. A line-frequency FSY signal is recommended, but any other control signal with a period of n x 8 clock cycles (n = 1, 2, 3, etc.) can be used.

It should be noted that in the event of asynchronism after first-time synchronization, at most the first output data words will be in valid for reasons of causality, depending on the output data format.

Output Stages

The timing of the output stages is selected for compatibility with common video memory ICs like the Siemens SDA 9251 TV-SAM or Texas Instruments TMS4C 1070 field memory. All outputs are, of course, TTL-compatible.

Because of the high clock rate, the output buffer stages in conjunction with the external capacitive load largely determine the total dissipation of the chip. Output lines not used by the set data format are therefore deactivated automatically (tristate). The user can also select ports for disconnection. For special applications, there are overflow and underflow outputs for each of the three ports. And the numeric format (binary or two's complement) can also be set for each port. The values 0 and 255 are only suppressed in 4:2:2 format in the “binary” setting because CCIR 656 presumes binary format.

Decimated output data are likewise synchronized with the high input sampling clock. It is ensured, however, that data words which must be repeated because they only have half, a quarter or an eighth of the sampling rate on the output are applied continuously without any spikes so that data is input at the receiver chip with suitably “relaxed” timing.

Application Notes

The external circuitry and wiring in the application device will largely determine whether the high performance of SDA 9205-2 is used in full. What is important is sufficient decoupling of the supply voltage pins (the chip has a total of seven ground and seven + 5 V pins) to guarantee high signal/noise ratio and prevent crosstalk between converters. The spacing between the blocking capacitors and the package pins in particular should therefore be kept as small as possible. Following adequate decoupling, supply pins of the same voltage can, of course, be combined; the same applies to the reference voltage pins.

Technical Data

Key technical data is listed in **table 2**. The typical luminance signal/noise ratio of 46 dB mentioned at the beginning applies to an input sampling frequency of 27 MHz. This does not allow for harmonics produced by non-linearities. The output sampling format is set for 4:1:1 without filtering. With the digital filtering turned on, the signal/noise ratio can even be somewhat higher because of noise-reducing averaging. It should be noted that the number of activated output drivers and their external capacitive load can generally influence the S/N ratio because of the steep-edged digital signals, so this number should be kept as low as possible.

Table 2
Major Technical Data at a Glance

SDA 9205-2	
Amplitude resolution Y, U, V	8 bits
Sampling rate Y, U, V	max. 30 MHz
Supply voltages	+ 5 V
Input capacitance	typ. 5 pF
Power bandwidth (– 3 dB)	min. 15 MHz
Differential non-linearity	max. $^1/_2$ LSB
Integral non-linearity	typ. $^1/_2$ LSB
Converter crosstalk	typ. – 50 dB
Package	P-LCC-68

References

[1] Haas, M.; Draxelmayr, D.; Kuttner, F.; Zojer, B.: A Monolithic Triple 8-bit Video Coder. IEEE Transactions on Consumer Electronics. CE-36 (1990) No. 3, pp. 722 to 729

[2] Siemens data sheet SDA 9205-2 (Triple Video ADC with Clamping)

[3] Bromba, M.; d'Andrea, G.: Featurebox 88: The Next Step in Digital Television. Siemens Components XXIII (1988) No. 6, pp. 240 to 245