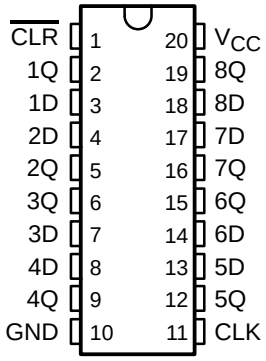
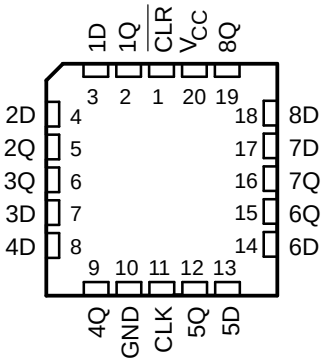
- **Operating Range 2-V to 5.5-V V_{CC}**
- ***EPIC***™ **(Enhanced-Performance Implanted CMOS) Process**
- **Contain Eight Flip-Flops With Single-Rail Outputs**
- **Direct Clear Input**
- **Individual Data Input to Each Flip-Flop**
- **Applications Include:**
  - **Buffer/Storage Registers**
  - **Shift Registers**
  - **Pattern Generators**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHC273 . . . J OR W PACKAGE
SN74AHC273 . . . DB, DGV, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54AHC273 . . . FK PACKAGE
(TOP VIEW)



description

These circuits are positive-edge-triggered D-type flip-flops with a direct clear ($\overline{CLR}$) input.

Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When CLK is at either the high or low level, the D input has no effect at the output.

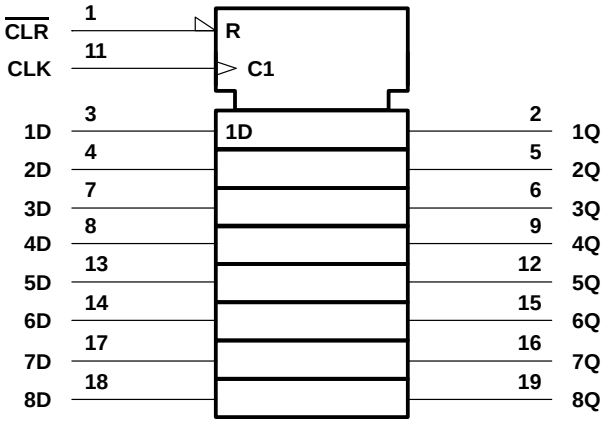
The SN54AHC273 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC273 is characterized for operation from –40°C to 85 °C.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{CLR}$	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

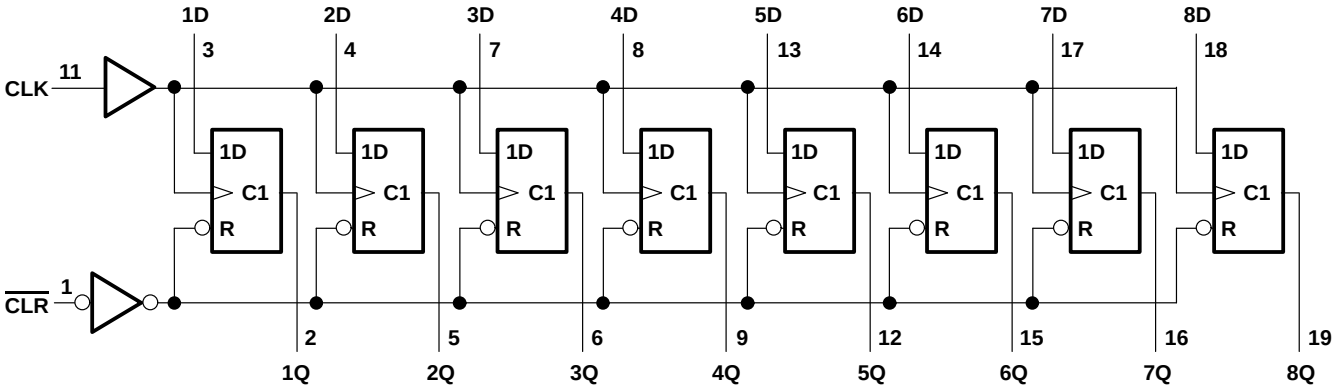
PRODUCT PREVIEW

logic symbol†

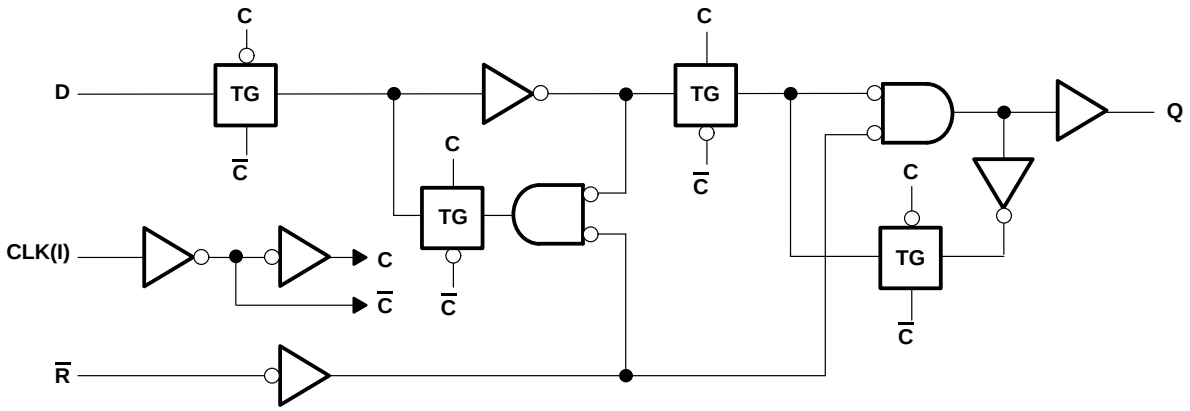


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



logic diagram, each flip-flop (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . –20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . . ±75 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package . . . . . 115°C/W
DGV package . . . . . 146°C/W
DW package . . . . . 97°C/W
N package . . . . . 67°C/W
PW package . . . . . 128°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions (see Note 3)

			SN54AHC273		SN74AHC273		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50		–50	μA
		V_{CC} = 3.3 V ± 0.3 V		–4		–4	mA
		V_{CC} = 5 V ± 0.5 V		–8		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4		4	mA
		V_{CC} = 5 V ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20		20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHC273		SN74AHC273		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	2 V	1.9			1.9		1.9		V
		3 V	2.9			2.9		2.9		
		4.5 V	4.4			4.4		4.4		
	I_{OH} = –4 mA	3 V	2.58			2.48		2.48		
	I_{OH} = –8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}	I_{OL} = 50 μA	2 V			0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
	I_{OL} = 4 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			4		40		40	μA
C_i	$V_I = V_{CC}$ or GND	5 V		4	10				10	pF

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		SN54AHC273		SN74AHC273		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{CLR}$ low	5		6		6		ns
		CLK high or low	5		6.5		6.5		
t_{su}	Setup time	Data before CLK↑	5.5		6.5		6.5		ns
		$\overline{CLR}$ before CLK↑	2.5		2.5		2.5		
t_h	Hold time, data after CLK↑		1		1		1		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		SN54AHC273		SN74AHC273		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{CLR}$ low	5		5		5		ns
		CLK high or low	5		5		5		
t_{su}	Setup time	Data before CLK↑	4.5		4.5		4.5		ns
		$\overline{CLR}$ before CLK↑	2		2		2		
t_h	Hold time, data after CLK↑		1		1		1		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHC273					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f_{max}			C_L = 15 pF*	75	120		65		MHz
			C_L = 50 pF	50	75		45		
t_{PHL}*	$\overline{CLR}$	Q	C_L = 15 pF		8.9	13.6	1	16	ns
t_{PLH}*	CLK	Q	C_L = 15 pF		8.7	13.6	1	16	ns
t_{PHL}*					8.7	13.6	1	16	
t_{PHL}	$\overline{CLR}$	Q	C_L = 50 pF		11.4	17.1	1	19.5	ns
t_{PLH}	CLK	Q	C_L = 50 pF		11.2	17.1	1	19.5	ns
t_{PHL}					11.2	17.1	1	19.5	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHC273					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f_{max}			C_L = 15 pF	75	120		65		MHz
			C_L = 50 pF	50	75		45		
t_{PHL}	$\overline{CLR}$	Q	C_L = 15 pF		8.9	13.6	1	16	ns
t_{PLH}	CLK	Q	C_L = 15 pF		8.7	13.6	1	16	ns
t_{PHL}					8.7	13.6	1	16	
t_{PHL}	$\overline{CLR}$	Q	C_L = 50 pF		11.4	17.1	1	19.5	ns
t_{PLH}	CLK	Q	C_L = 50 pF		11.2	17.1	1	19.5	ns
t_{PHL}					11.2	17.1	1	19.5	

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switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHC273					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f_{max}			C_L = 15 pF*	120	165		100		MHz
			C_L = 50 pF	80	110		70		
t_{PHL}*	$\overline{CLR}$	Q	C_L = 15 pF		5.2	8.5	1	10	ns
t_{PLH}*	CLK	Q	C_L = 15 pF		5.8	9	1	10.5	ns
t_{PHL}*					5.8	9	1	10.5	
t_{PHL}	$\overline{CLR}$	Q	C_L = 50 pF		6.7	10.5	1	12	ns
t_{PLH}	CLK	Q	C_L = 50 pF		7.3	11	1	12.5	ns
t_{PHL}					7.3	11	1	12.5	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHC273					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f_{max}			C_L = 15 pF	120	165		100		MHz
			C_L = 50 pF	80	110		70		
t_{PHL}	$\overline{CLR}$	Q	C_L = 15 pF		5.2	8.5	1	10	ns
t_{PLH}	CLK	Q	C_L = 15 pF		5.8	9	1	10.5	ns
t_{PHL}					5.8	9	1	10.5	
t_{PHL}	$\overline{CLR}$	Q	C_L = 50 pF		6.7	10.5	1	12	ns
t_{PLH}	CLK	Q	C_L = 50 pF		7.3	11	1	12.5	ns
t_{PHL}					7.3	11	1	12.5	

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER		V_{CC}	SN74AHC273			UNIT
			T_A = 25°C		MIN	MAX	
			MIN	MAX			
$t_{sk(o)}$	Output skew	3.3 V ± 0.3 V		1.5		1.5	ns
		5 V ± 0.5 V		1		1	

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

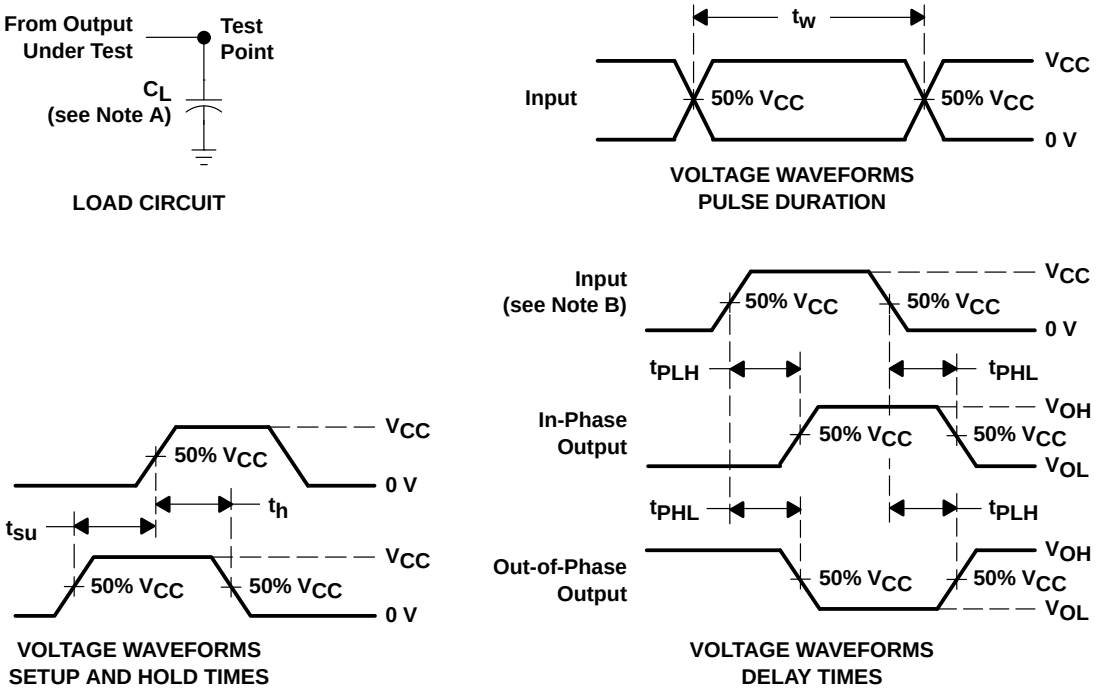
PARAMETER		SN74AHC273			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}			–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}				V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	No load	31	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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