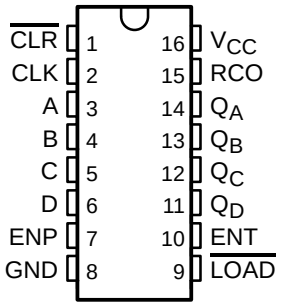
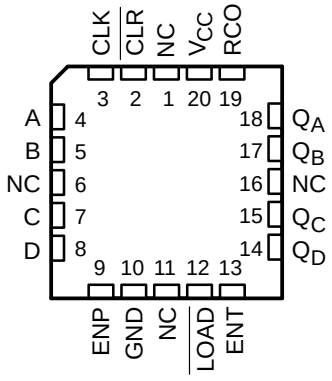
- **Operating Range 2-V to 5.5-V V_{CC}**
- ***EPIC***™ **(Enhanced-Performance Implanted CMOS) Process**
- **Internal Look-Ahead for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Synchronous Counting**
- **Synchronously Programmable**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHC163 . . . J OR W PACKAGE
SN74AHC163 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AHC163 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The ’AHC163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when instructed by the count-enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes normally associated with synchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, they can be preset to any number between 0 and 9 or 15. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable inputs.

The clear function for the ’AHC163 is synchronous. A low level at the clear ($\overline{\text{CLR}}$) input sets all four of the flip-flop outputs low after the next low-to-high transition of CLK, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily by decoding the Q outputs for the maximum count desired. The active-low output of the gate used for decoding is connected to $\overline{\text{CLR}}$ to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. ENP, ENT, and a ripple-carry output (RCO) are instrumental in accomplishing this function. Both ENP and ENT must be high to count, and ENT is fed forward to enable RCO. Enabling RCO produces a high-level pulse while the count is maximum (9 or 15 with Q_A high). This high-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed, regardless of the level of CLK.

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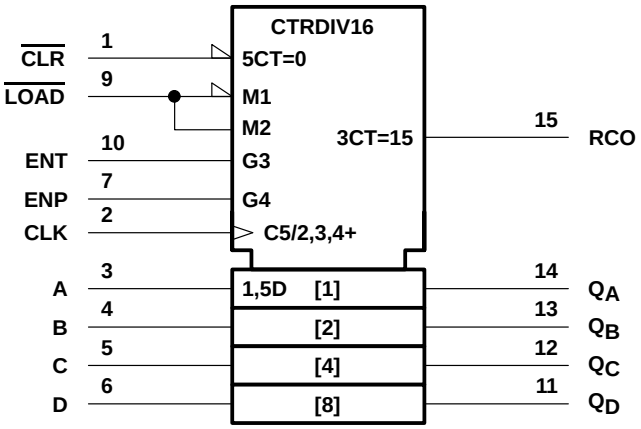
description (continued)

These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or $\overline{\text{LOAD}}$) that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.

The SN54AHC163 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC163 is characterized for operation from –40°C to 85°C.

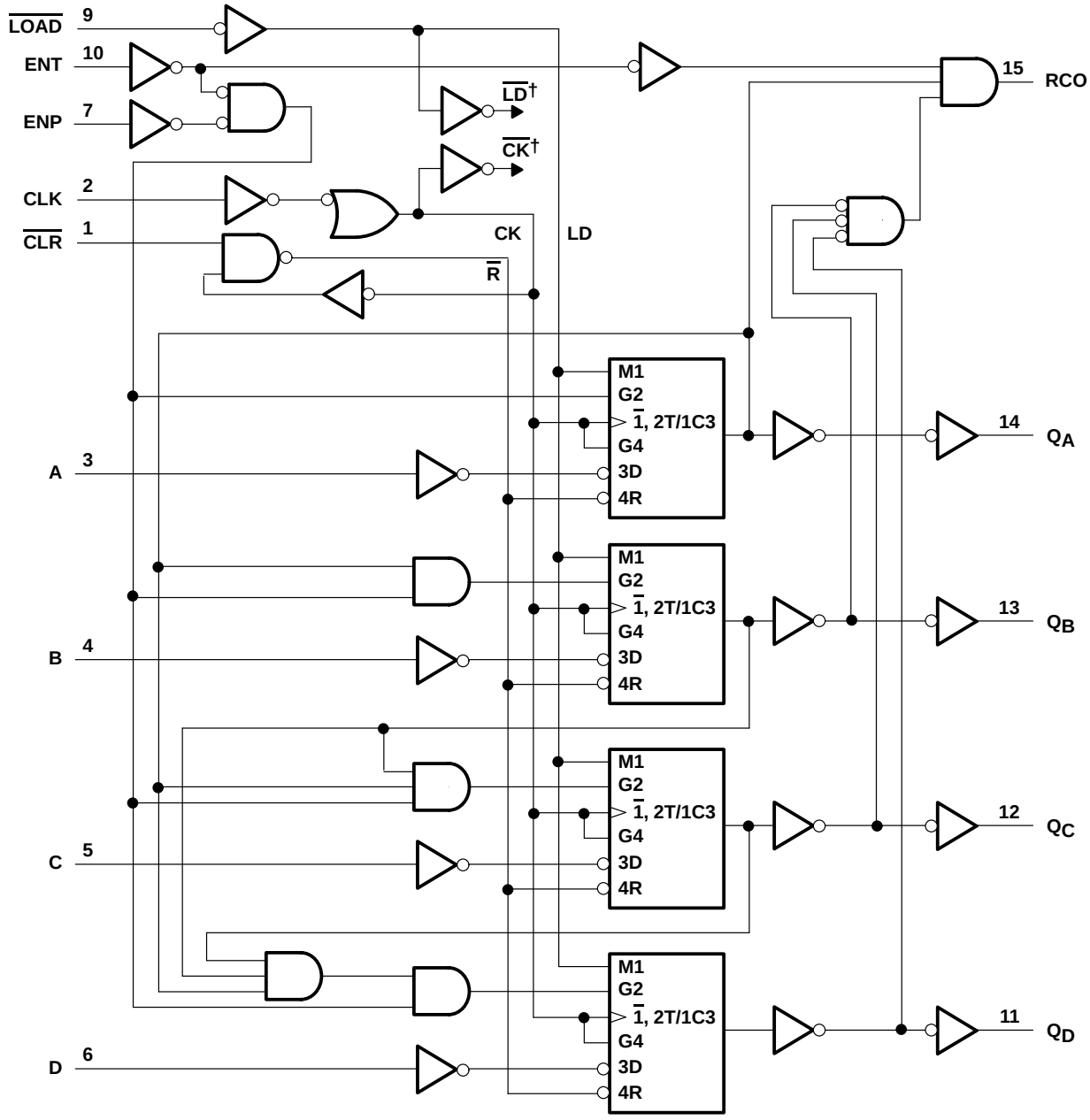
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

PRODUCT PREVIEW

logic diagram (positive logic)



† For simplicity, routing of complementary signals $\overline{LD}$ and $\overline{CK}$ is not shown on this overall logic diagram. The uses of these signals are shown on the logic diagram of the D/T flip-flops.

Pin numbers shown are for the D, DB, J, N, PW, and W packages.

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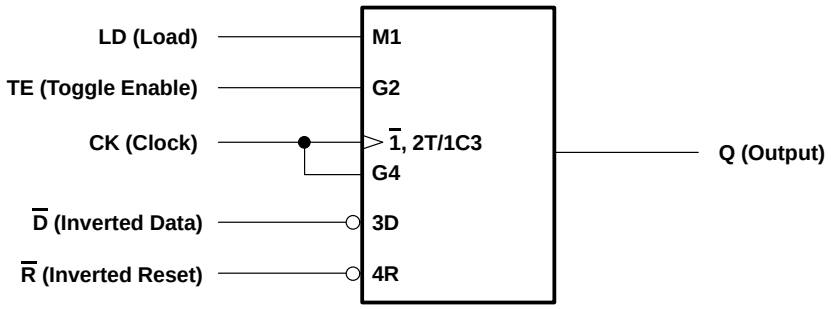
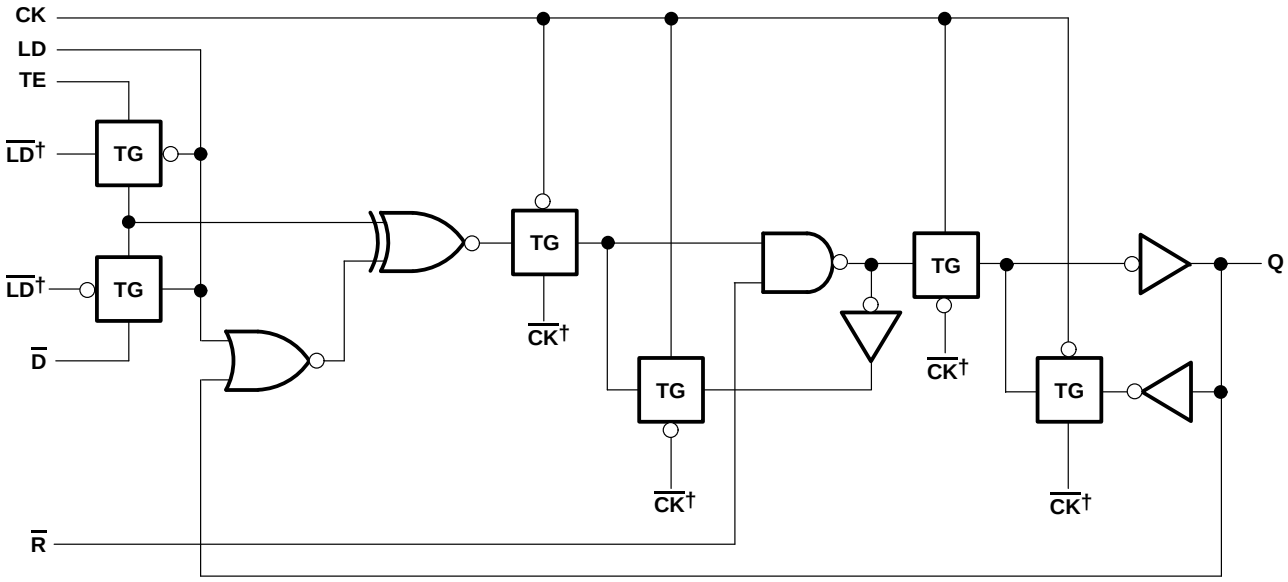
logic symbol, each D/T flip-flop



logic diagram, each D/T flip-flop (positive logic)

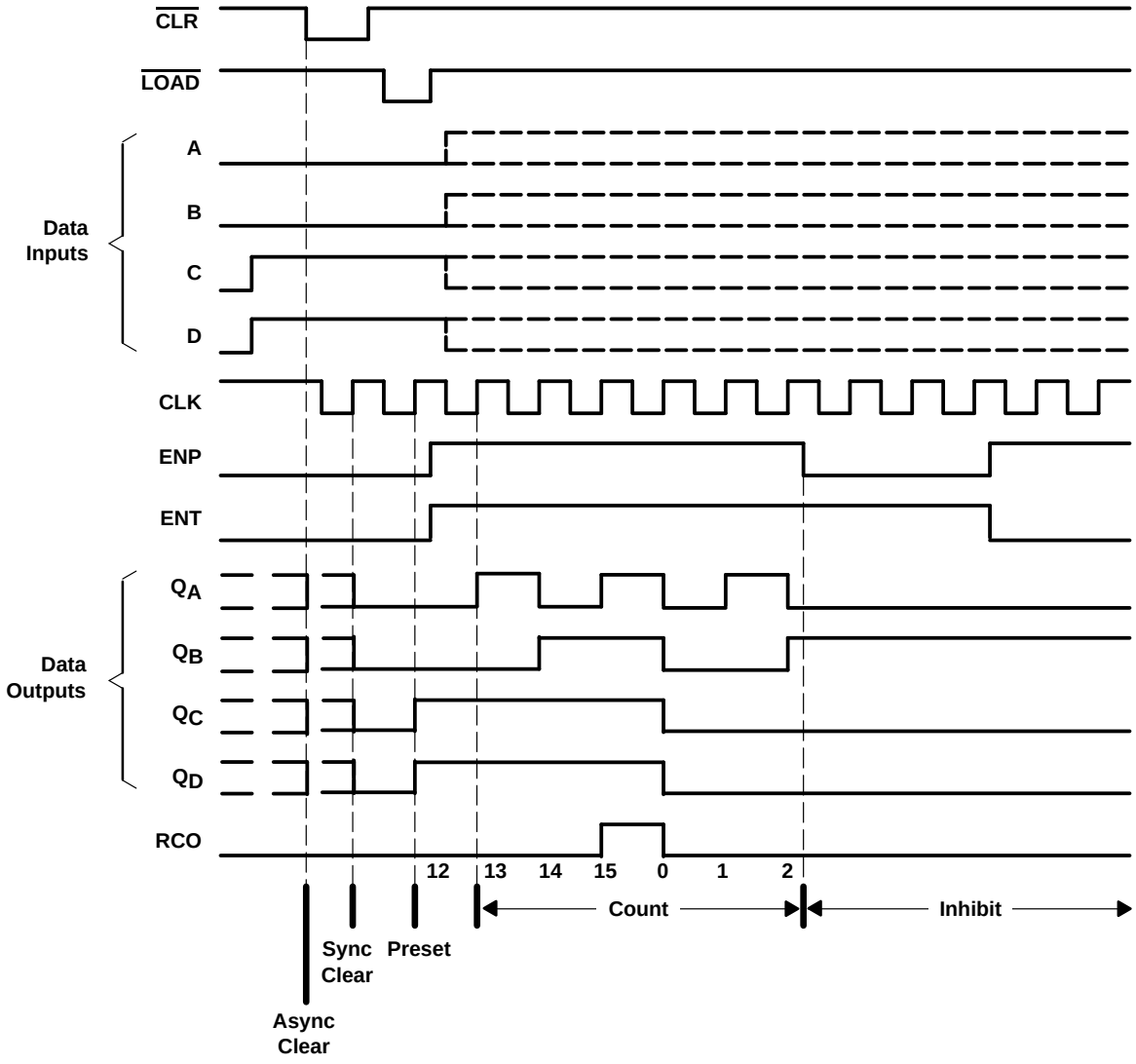


† The origins of $\overline{LD}$ and $\overline{CK}$ are shown in the logic diagram of the overall device.

typical clear, preset, count, and inhibit sequence

The following sequence is illustrated below:

1. Clear outputs to zero (synchronous)
2. Preset to binary 12
3. Count to 13, 14, 15, 0, 1, and 2
4. Inhibit



absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . –20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . . 113°C/W
DB package . . . . . 131°C/W
N package . . . . . 78°C/W
PW package . . . . . 149°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

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recommended operating conditions (see Note 3)

			SN54AHC163		SN74AHC163		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50		–50	μA
		V_{CC} = 3.3 V ± 0.3 V		–4		–4	mA
		V_{CC} = 5 V ± 0.5 V		–8		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4		4	mA
		V_{CC} = 5 V ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20		20	
T_A	Operating free-air temperature		–55	125	– 40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHC163		SN74AHC163		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	2 V	1.9	2		1.9		1.9		V
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	I_{OH} = –4 mA	3 V	2.58			2.48		2.48		
	I_{OH} = –8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}	I_{OL} = 50 μA	2 V			0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
	I_{OL} = 4 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			4		40		40	μA
C_i	$V_I = V_{CC}$ or GND	5 V		2	10				10	pF

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		SN54AHC163		SN74AHC163		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, CLK high or low		5		5		5		ns
t_{su}	Setup time before CLK↑	$\overline{CLR}$	4		4		4		ns
		Data (A, B, C, and D)	5.5		6.5		6.5		
		ENP, ENT	7.5		9		9		
		$\overline{LOAD}$ low	8		9.5		9.5		
t_h	Hold time, all synchronous inputs after CLK↑		1		1		1		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		SN54AHC163		SN74AHC163		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, CLK high or low		5		5		5		ns
t_{su}	Setup time before CLK↑	$\overline{CLR}$	3.5		3.5		3.5		ns
		Data (A, B, C, and D)	4.5		4.5		4.5		
		ENP, ENT	5		6		6		
		$\overline{LOAD}$ low	5		6		6		
t_h	Hold time, all synchronous inputs after CLK↑		1		1		1		ns

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switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHC163					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f_{max}			C_L = 15 pF*		130	80		70	MHz
			C_L = 50 pF		85	55		50	
t_{PLH}*	CLK	Q	C_L = 15 pF		8.3	12.8	1	15	ns
t_{PHL}*					8.3	12.8	1	15	
t_{PLH}*	CLK	RCO (count mode)	C_L = 15 pF		8.7	13.6	1	16	ns
t_{PHL}*					8.7	13.6	1	16	
t_{PLH}*	CLK	RCO (preset mode)	C_L = 15 pF		11	17.2	1	20	ns
t_{PHL}*					11	17.2	1	20	
t_{PLH}*	ENT	RCO	C_L = 15 pF		7.5	12.3	1	14.5	ns
t_{PHL}*					7.5	12.3	1	14.5	
t_{PLH}	CLK	Q	C_L = 50 pF		10.8	16.3	1	18.5	ns
t_{PHL}					10.8	16.3	1	18.5	
t_{PLH}	CLK	RCO (count mode)	C_L = 50 pF		11.2	17.1	1	19.5	ns
t_{PHL}					11.2	17.1	1	19.5	
t_{PLH}	CLK	RCO (preset mode)	C_L = 50 pF		13.5	20.7	1	23.5	ns
t_{PHL}					13.5	20.7	1	23.5	
t_{PLH}	ENT	RCO	C_L = 50 pF		10.5	15.8	1	18	ns
t_{PHL}					10.5	15.8	1	18	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHC163					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f_{max}			C_L = 15 pF		130	80		70	MHz
			C_L = 50 pF		85	55		50	
t_{PLH}	CLK	Q	C_L = 15 pF		8.3	12.8	1	15	ns
t_{PHL}					8.3	12.8	1	15	
t_{PLH}	CLK	RCO (count mode)	C_L = 15 pF		8.7	13.6	1	16	ns
t_{PHL}					8.7	13.6	1	16	
t_{PLH}	CLK	RCO (preset mode)	C_L = 15 pF		11	17.2	1	20	ns
t_{PHL}					11	17.2	1	20	
t_{PLH}	ENT	RCO	C_L = 15 pF		7.5	12.3	1	14.5	ns
t_{PHL}					7.5	12.3	1	14.5	
t_{PLH}	CLK	Q	C_L = 50 pF		10.8	16.3	1	18.5	ns
t_{PHL}					10.8	16.3	1	18.5	
t_{PLH}	CLK	RCO (count mode)	C_L = 50 pF		11.2	17.1	1	19.5	ns
t_{PHL}					11.2	17.1	1	19.5	
t_{PLH}	CLK	RCO (preset mode)	C_L = 50 pF		13.5	20.7	1	23.5	ns
t_{PHL}					13.5	20.7	1	23.5	
t_{PLH}	ENT	RCO	C_L = 50 pF		10.5	15.8	1	18	ns
t_{PHL}					10.5	15.8	1	18	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHC163					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f_{max}			C_L = 15 pF*		185	135		115	MHz
			C_L = 50 pF		125	95		85	
t_{PLH}*	CLK	Q	C_L = 15 pF		4.9	8.1	1	9.5	ns
t_{PHL}*					4.9	8.1	1	9.5	
t_{PLH}*	CLK	RCO (count mode)	C_L = 15 pF		4.9	8.1	1	9.5	ns
t_{PHL}*					4.9	8.1	1	9.5	
t_{PLH}*	CLK	RCO (preset mode)	C_L = 15 pF		6.2	10.3	1	12	ns
t_{PHL}*					6.2	10.3	1	12	
t_{PLH}*	ENT	RCO	C_L = 15 pF		4.9	8.1	1	9.5	ns
t_{PHL}*					4.9	8.1	1	9.5	
t_{PLH}	CLK	Q	C_L = 50 pF		6.4	10.1	1	11.5	ns
t_{PHL}					6.4	10.1	1	11.5	
t_{PLH}	CLK	RCO (count mode)	C_L = 50 pF		6.4	10.1	1	11.5	ns
t_{PHL}					6.4	10.1	1	11.5	
t_{PLH}	CLK	RCO (preset mode)	C_L = 50 pF		7.7	12.3	1	14	ns
t_{PHL}					7.7	12.3	1	14	
t_{PLH}	ENT	RCO	C_L = 50 pF		6.4	10.1	1	11.5	ns
t_{PHL}					6.4	10.1	1	11.5	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHC163					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f_{max}			C_L = 15 pF		185	135		115	MHz
			C_L = 50 pF		125	95		85	
t_{PLH}	CLK	Q	C_L = 15 pF		4.9	8.1	1	9.5	ns
t_{PHL}					4.9	8.1	1	9.5	
t_{PLH}	CLK	RCO (count mode)	C_L = 15 pF		4.9	8.1	1	9.5	ns
t_{PHL}					4.9	8.1	1	9.5	
t_{PLH}	CLK	RCO (preset mode)	C_L = 15 pF		6.2	10.3	1	12	ns
t_{PHL}					6.2	10.3	1	12	
t_{PLH}	ENT	RCO	C_L = 15 pF		4.9	8.1	1	9.5	ns
t_{PHL}					4.9	8.1	1	9.5	
t_{PLH}	CLK	Q	C_L = 50 pF		6.4	10.1	1	11.5	ns
t_{PHL}					6.4	10.1	1	11.5	
t_{PLH}	CLK	RCO (count mode)	C_L = 50 pF		6.4	10.1	1	11.5	ns
t_{PHL}					6.4	10.1	1	11.5	
t_{PLH}	CLK	RCO (preset mode)	C_L = 50 pF		7.7	12.3	1	14	ns
t_{PHL}					7.7	12.3	1	14	
t_{PLH}	ENT	RCO	C_L = 50 pF		6.4	10.1	1	11.5	ns
t_{PHL}					6.4	10.1	1	11.5	

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

PARAMETER		SN74AHC163			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.4	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.4	–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}				V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	23	pF

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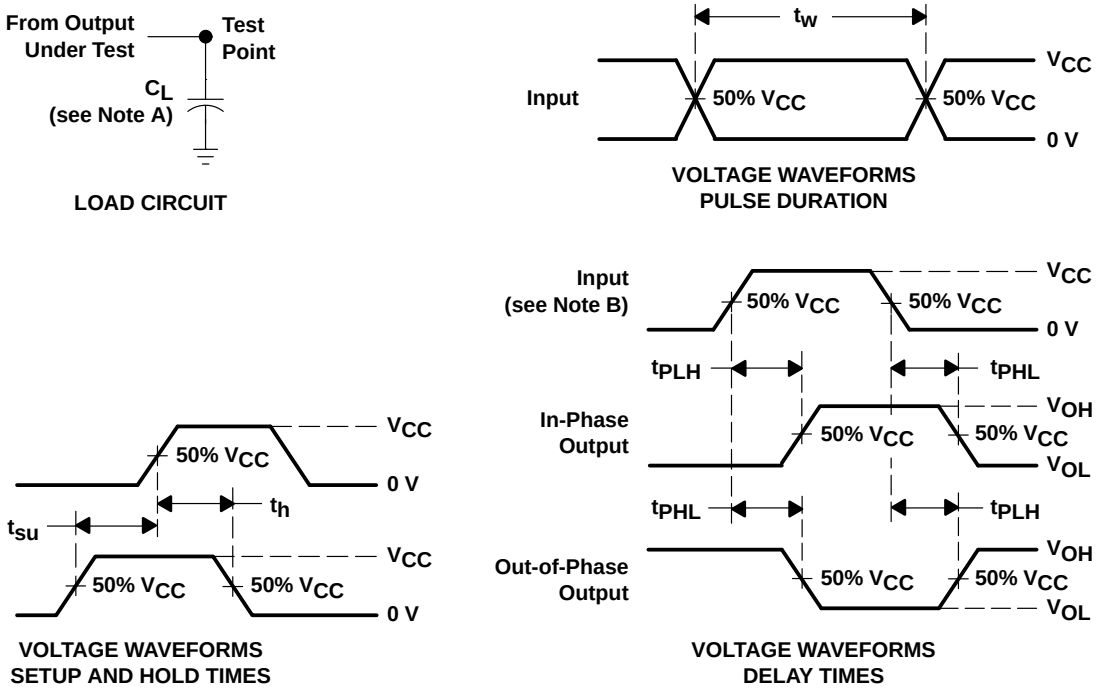
PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

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