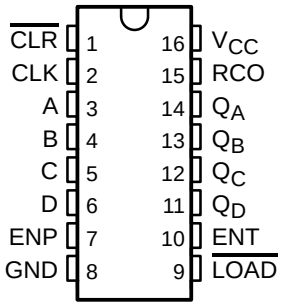
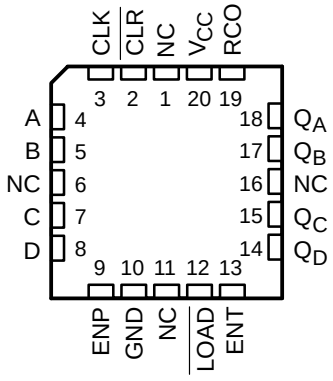
- **Inputs Are TTL-Voltage Compatible**
- ***EPIC***™ **(Enhanced-Performance Implanted CMOS) Process**
- **Internal Look-Ahead for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Synchronous Counting**
- **Synchronously Programmable**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHCT161 . . . J OR W PACKAGE
SN74AHCT161 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AHCT161 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The ’AHCT161 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with synchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, they can be preset to any number between 0 and 9 or 15. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable inputs.

The clear function for the ’AHCT161 is asynchronous. A low level at the clear ($\overline{\text{CLR}}$) input sets all four of the flip-flop outputs low, regardless of the levels of the CLK, load ($\overline{\text{LOAD}}$), or enable inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are ENP, ENT, and a ripple-carry (RCO) output. Both ENP and ENT must be high to count, and ENT is fed forward to enable RCO. Enabling RCO produces a high-level pulse while the count is maximum (9 or 15 with Q_A high). This high-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed, regardless of the level of CLK.

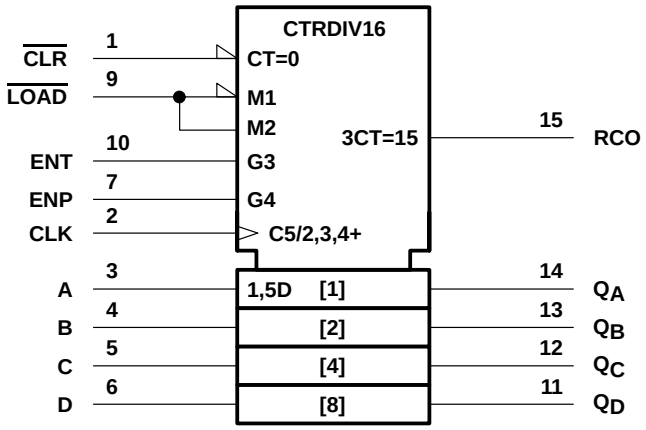
These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or $\overline{\text{LOAD}}$) that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.

PRODUCT PREVIEW

description (continued)

The SN54AHCT161 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT161 is characterized for operation from –40°C to 85°C.

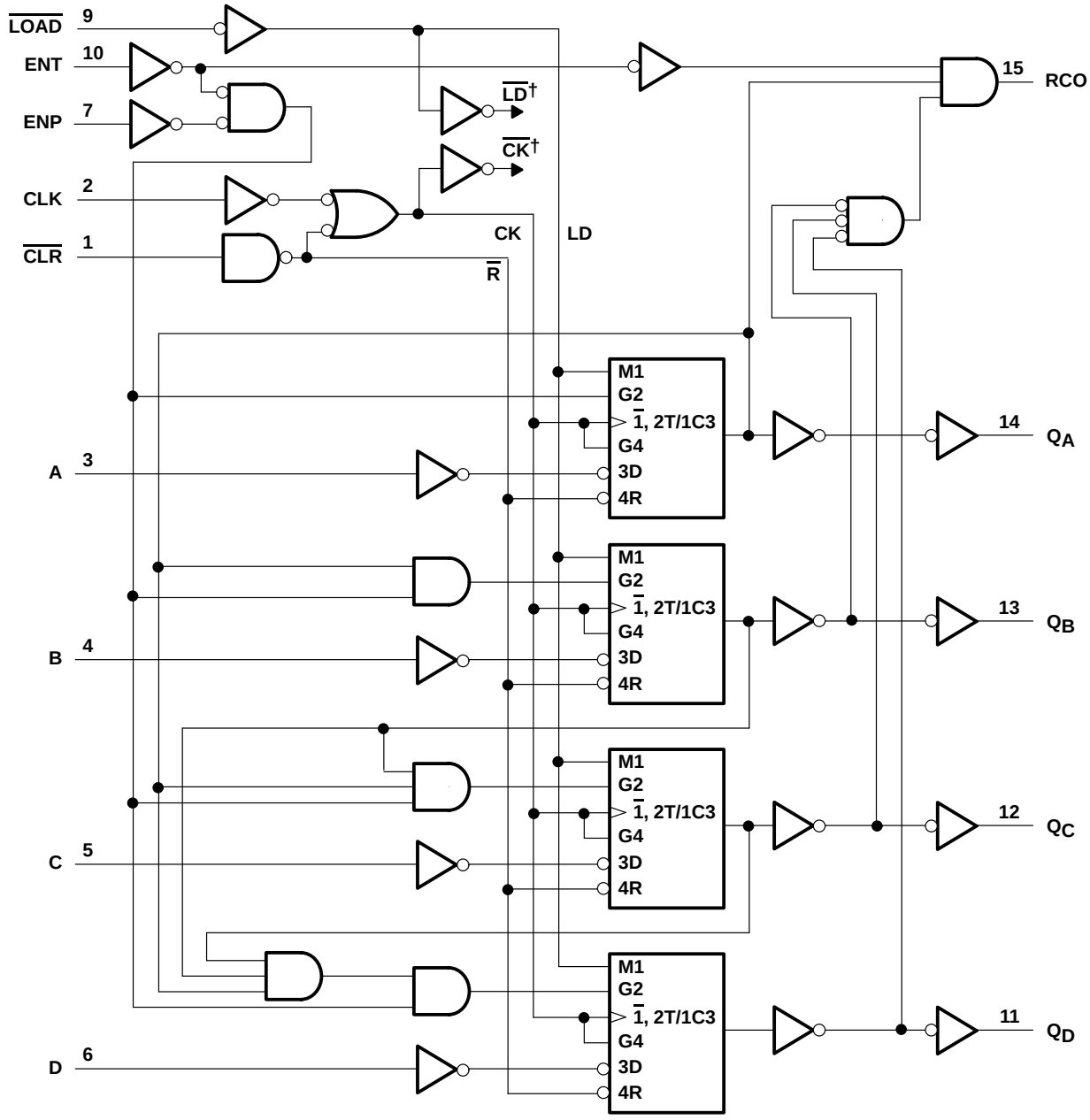
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

PRODUCT PREVIEW

logic diagram (positive logic)

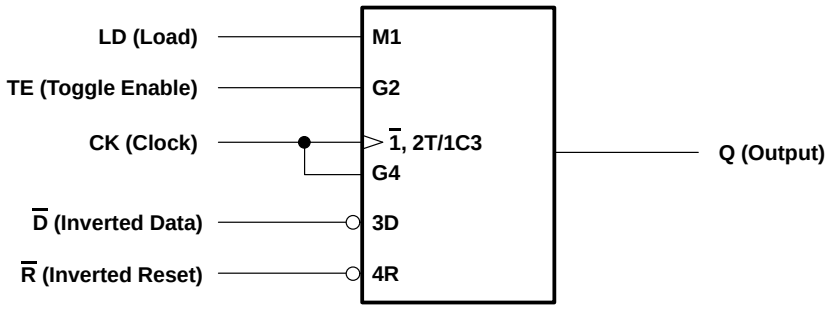


† For simplicity, routing of complementary signals $\overline{LD}$ and $\overline{CK}$ is not shown on this overall logic diagram. The uses of these signals are shown on the logic diagram of the D/T flip-flops.

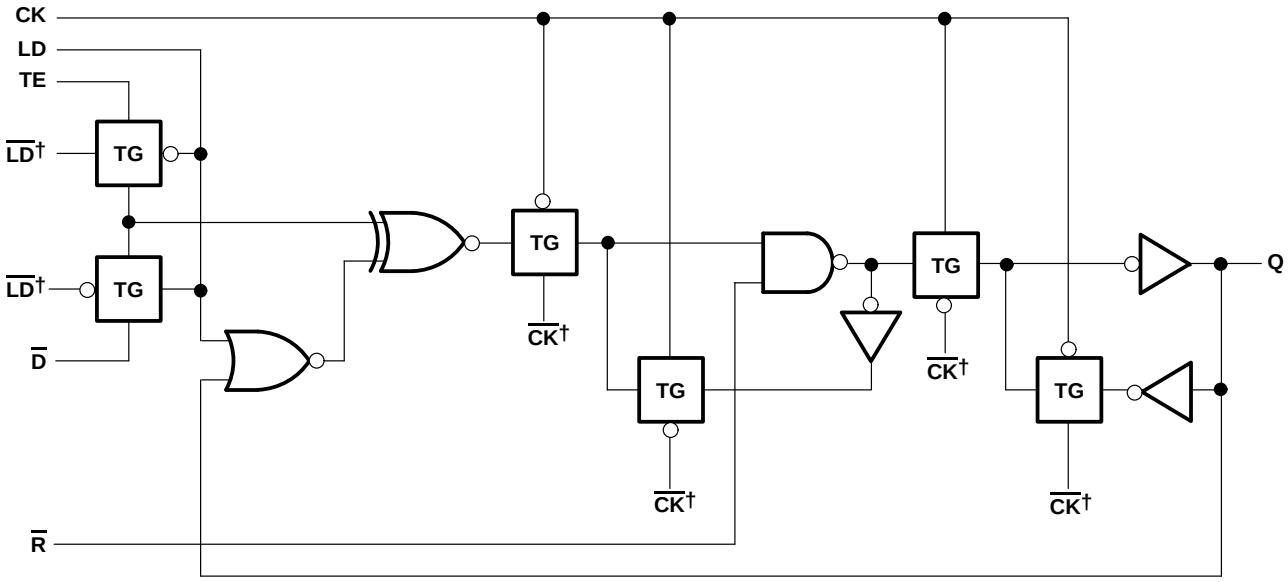
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

PRODUCT PREVIEW

logic symbol, each D/T flip-flop



logic diagram, each D/T flip-flop (positive logic)

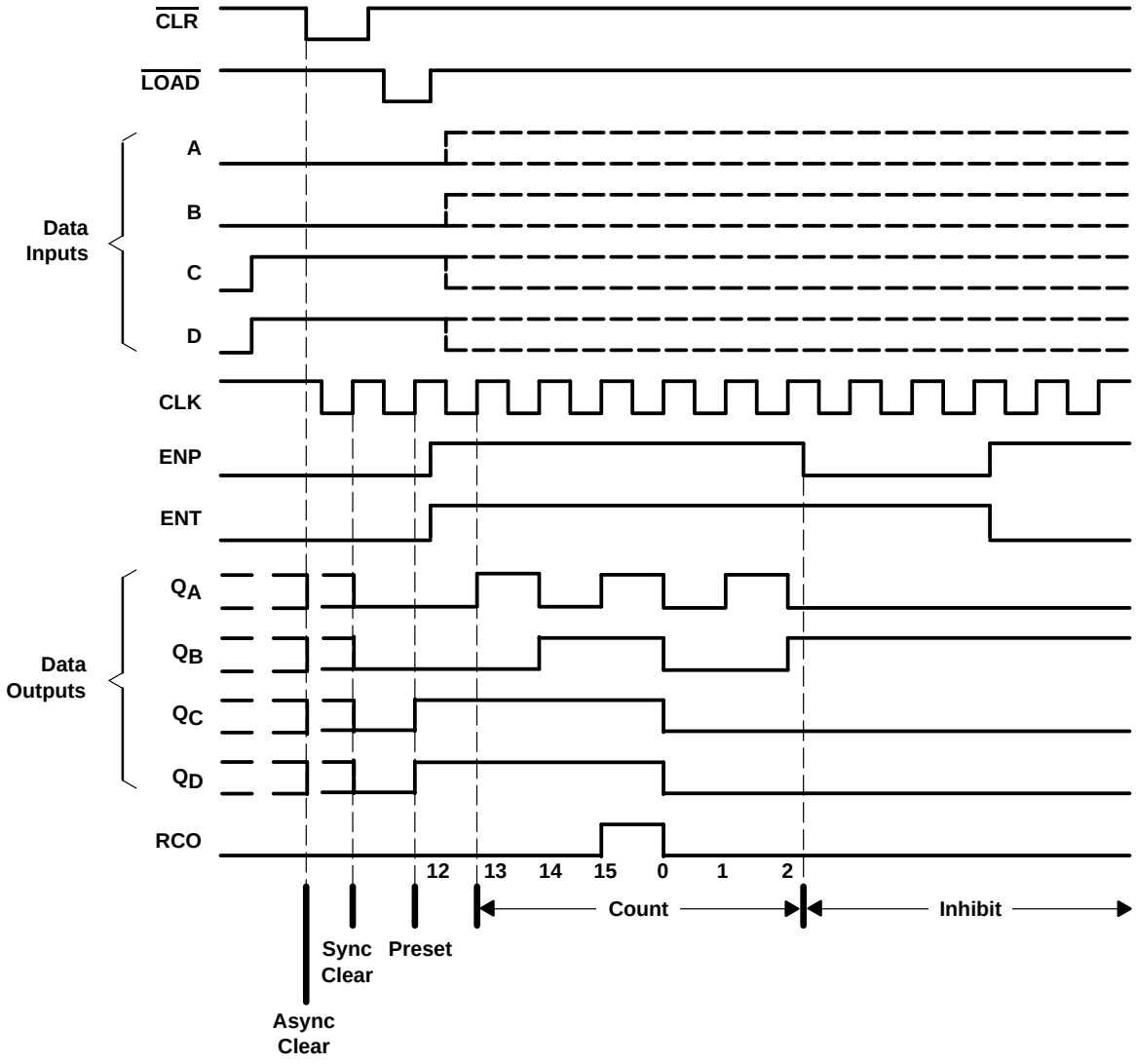


† The origins of $\overline{LD}$ and $\overline{CK}$ are shown in the logic diagram of the overall device.

typical clear, preset, count, and inhibit sequence

The following sequence is illustrated below:

1. Clear outputs to zero (asynchronous)
2. Preset to binary 12
3. Count to 13, 14, 15, 0, 1, and 2
4. Inhibit



absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . –20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . . 113°C/W
DB package . . . . . 131°C/W
N package . . . . . 78°C/W
PW package . . . . . 149°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

PRODUCT PREVIEW

recommended operating conditions (see Note 3)

		SN54AHCT161		SN74AHCT161		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–8		–8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20		20	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHCT161		SN74AHCT161		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	4.5 V	4.4	4.5		4.4		4.4		V
	I_{OH} = –8 mA		3.94			3.8		3.8		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
	I_{OL} = 8 mA				0.36		0.44		0.44	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40		40	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5		1.5	mA
C_i	V_I = V_{CC} or GND	5 V		2	10				10	pF

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		SN54AHCT161		SN74AHCT161		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high or low	5		5		5		ns
		$\overline{CLR}$ low	5		5		5		
t_{su}	Setup time before CLK↑	$\overline{CLR}$	1.5		1.5		1.5		ns
		Data (A, B, C, and D)	4.5		4.5		4.5		
		ENP, ENT	5		6		6		
		$\overline{LOAD}$ low	5		6		6		
t_h	Hold time, all synchronous inputs after CLK↑		1		1		1		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHCT161					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f_{max}			C_L = 15 pF*		185	135		115	MHz
			C_L = 50 pF		125	95		85	
t_{PLH}*	CLK	Q	C_L = 15 pF		4.9	8.1	1	9.5	ns
t_{PHL}*					4.9	8.1	1	9.5	
t_{PLH}*	CLK	RCO (count mode)	C_L = 15 pF		4.9	8.1	1	9.5	ns
t_{PHL}*					4.9	8.1	1	9.5	
t_{PLH}*	CLK	RCO (preset mode)	C_L = 15 pF		6.2	10.3	1	12	ns
t_{PHL}*					6.2	10.3	1	12	
t_{PLH}*	ENT	RCO	C_L = 15 pF		4.9	8.1	1	9.5	ns
t_{PHL}*					4.9	8.1	1	9.5	
t_{PHL}*	$\overline{CLR}$	Q	C_L = 15 pF		5.5	9	1	10.5	ns
		RCO			5	8.6	1	10	
t_{PLH}	CLK	Q	C_L = 50 pF		6.4	10.1	1	11.5	ns
t_{PHL}					6.4	10.1	1	11.5	
t_{PLH}	CLK	RCO (count mode)	C_L = 50 pF		6.4	10.1	1	11.5	ns
t_{PHL}					6.4	10.1	1	11.5	
t_{PLH}	CLK	RCO (preset mode)	C_L = 50 pF		7.7	12.3	1	14	ns
t_{PHL}					7.7	12.3	1	14	
t_{PLH}	ENT	RCO	C_L = 50 pF		6.4	10.1	1	11.5	ns
t_{PHL}					6.4	10.1	1	11.5	
t_{PHL}	$\overline{CLR}$	Q	C_L = 50 pF		7	11	1	12.5	ns
		RCO			6.5	10.6	1	12	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHCT161					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f_{max}			C_L = 15 pF		185	135		115	MHz
			C_L = 50 pF		125	95		85	
t_{PLH}	CLK	Q	C_L = 15 pF		4.9	8.1	1	9.5	ns
t_{PHL}					4.9	8.1	1	9.5	
t_{PLH}	CLK	RCO (count mode)	C_L = 15 pF		4.9	8.1	1	9.5	ns
t_{PHL}					4.9	8.1	1	9.5	
t_{PLH}	CLK	RCO (preset mode)	C_L = 15 pF		6.2	10.3	1	12	ns
t_{PHL}					6.2	10.3	1	12	
t_{PLH}	ENT	RCO	C_L = 15 pF		4.9	8.1	1	9.5	ns
t_{PHL}					4.9	8.1	1	9.5	
t_{PHL}	$\overline{CLR}$	Q	C_L = 15 pF		5.5	9	1	10.5	ns
		RCO			5	8.6	1	10	
t_{PLH}	CLK	Q	C_L = 50 pF		6.4	10.1	1	11.5	ns
t_{PHL}					6.4	10.1	1	11.5	
t_{PLH}	CLK	RCO (count mode)	C_L = 50 pF		6.4	10.1	1	11.5	ns
t_{PHL}					6.4	10.1	1	11.5	
t_{PLH}	CLK	RCO (preset mode)	C_L = 50 pF		7.7	12.3	1	14	ns
t_{PHL}					7.7	12.3	1	14	
t_{PLH}	ENT	RCO	C_L = 50 pF		6.4	10.1	1	11.5	ns
t_{PHL}					6.4	10.1	1	11.5	
t_{PHL}	$\overline{CLR}$	Q	C_L = 50 pF		7	11	1	12.5	ns
		RCO			6.5	10.6	1	12	

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

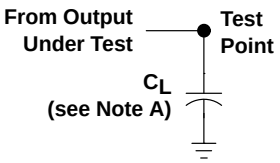
PARAMETER		SN74AHCT161			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.4	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.4	–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}				V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

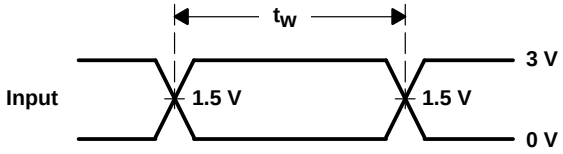
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	23	pF

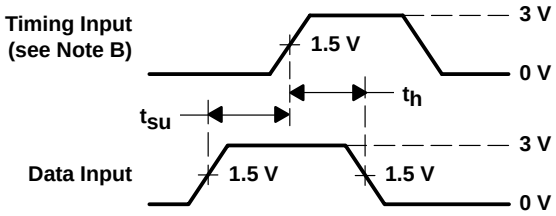
PARAMETER MEASUREMENT INFORMATION



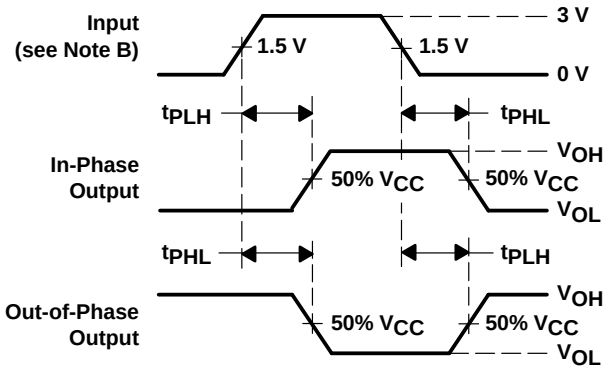
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.