

SN54AHCT257, SN74AHCT257 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

SCLS351C – MAY 1996 – REVISED JUNE 1997

- Inputs Are TTL-Voltage Compatible
- **EPIC™** (Enhanced-Performance Implanted CMOS) Process
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

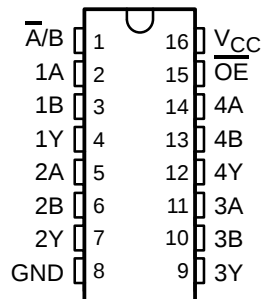
description

These quadruple 2-line to 1-line data selectors/multiplexers are designed for 4.5-V to 5.5-V V_{CC} operation.

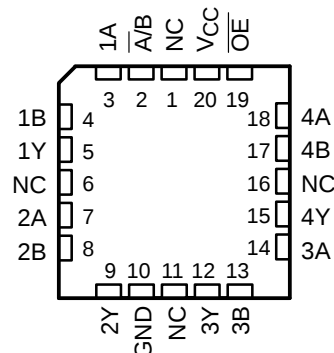
The 'AHCT257 are designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems. The 3-state outputs do not load the data lines when the output-enable ($\overline{OE}$) input is at the high logic level.

The SN54AHCT257 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AHCT257 is characterized for operation from -40°C to 85°C .

SN54AHCT257 . . . J OR W PACKAGE
SN74AHCT257 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AHCT257 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

INPUTS				OUTPUT Y
$\overline{OE}$	$\overline{A/B}$	A	B	
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H



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PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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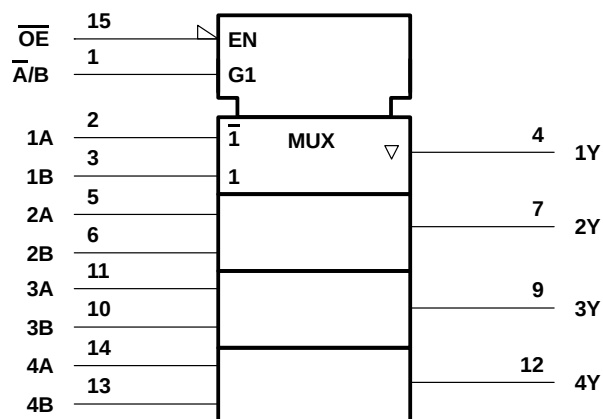
SN54AHCT257, SN74AHCT257

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WITH 3-STATE OUTPUTS

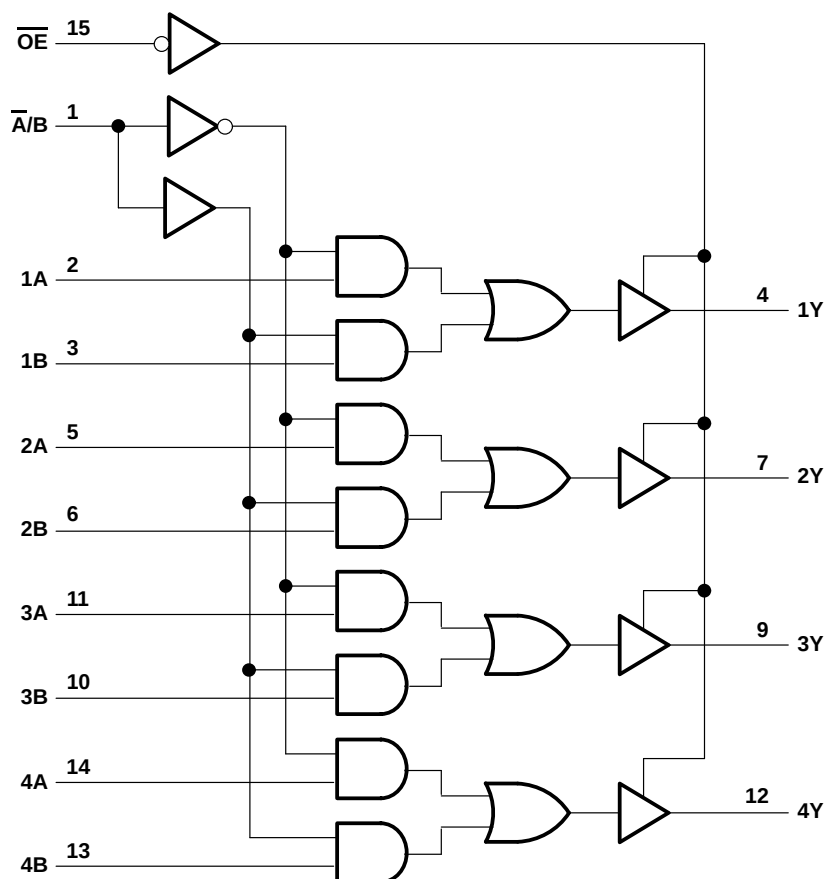
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, PW, and W packages.

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SN54AHCT257, SN74AHCT257

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SCLS351C – MAY 1996 – REVISED JUNE 1997

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	113°C/W
DB package	131°C/W
N package	78°C/W
PW package	149°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JEDEC 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions (see Note 3)

		SN54AHCT257		SN74AHCT257		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–8		–8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall time		20		20	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			SN54AHCT257		SN74AHCT257		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$I_{OH} = -50 \mu\text{A}$	4.5 V	4.4	4.5		4.4		4.4		V
	$I_{OH} = -8 \text{ mA}$		3.94			3.8		3.8		
V_{OL}	$I_{OL} = 50 \mu\text{A}$	4.5 V			0.1		0.1		0.1	V
	$I_{OL} = 8 \text{ mA}$				0.36		0.44		0.44	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			4		40		40	μA
$\Delta I_{CC}^\ddagger$	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5		1.5	mA
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.25		±2.5		±2.5	μA
C_i	$V_I = V_{CC}$ or GND	5 V		2	10				10	pF

[‡] This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC} .



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SCLS351C – MAY 1996 – REVISED JUNE 1997

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHCT257				UNIT
				$T_A = 25^\circ\text{C}$			MIN	MAX
				MIN	TYP	MAX		
t_{PLH}^*	A or B	Y	$C_L = 15\text{ pF}$	4.1	6.4	1	7.5	ns
t_{PHL}^*				4.1	6.4	1	7.5	
t_{PLH}^*	$\bar{A}/B$	Y	$C_L = 15\text{ pF}$	5.3	8.1	1	9.5	ns
t_{PHL}^*				5.3	8.1	1	9.5	
t_{PZH}^*	$\overline{OE}$	Y	$C_L = 15\text{ pF}$	5.6	8.6	1	10	ns
t_{PZL}^*				5.6	8.6	1	10	
t_{PHZ}^*	$\overline{OE}$	Y	$C_L = 15\text{ pF}$					ns
t_{PLZ}^*								
t_{PLH}	A or B	Y	$C_L = 50\text{ pF}$	5.6	8.4	1	9.5	ns
t_{PHL}				5.6	8.4	1	9.5	
t_{PLH}	$\bar{A}/B$	Y	$C_L = 50\text{ pF}$	6.8	10.1	1	11.5	ns
t_{PLH}				6.8	10.1	1	11.5	
t_{PZH}	$\overline{OE}$	Y	$C_L = 50\text{ pF}$	7.1	10.6	1	12	ns
t_{PZL}				7.1	10.6	1	12	
t_{PHZ}	$\overline{OE}$	Y	$C_L = 50\text{ pF}$					ns
t_{PLZ}								

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHCT257				UNIT
				$T_A = 25^\circ\text{C}$			MIN	MAX
				MIN	TYP	MAX		
t_{PLH}	A or B	Y	$C_L = 15\text{ pF}$	4.1	6.4	1	7.5	ns
t_{PHL}				4.1	6.4	1	7.5	
t_{PLH}	$\bar{A}/B$	Y	$C_L = 15\text{ pF}$	5.3	8.1	1	9.5	ns
t_{PHL}				5.3	8.1	1	9.5	
t_{PZH}	$\overline{OE}$	Y	$C_L = 15\text{ pF}$	5.6	8.6	1	10	ns
t_{PZL}				5.6	8.6	1	10	
t_{PHZ}	$\overline{OE}$	Y	$C_L = 15\text{ pF}$					ns
t_{PLZ}								
t_{PLH}	A or B	Y	$C_L = 50\text{ pF}$	5.6	8.4	1	9.5	ns
t_{PHL}				5.6	8.4	1	9.5	
t_{PLH}	$\bar{A}/B$	Y	$C_L = 50\text{ pF}$	6.8	10.1	1	11.5	ns
t_{PLH}				6.8	10.1	1	11.5	
t_{PZH}	$\overline{OE}$	Y	$C_L = 50\text{ pF}$	7.1	10.6	1	12	ns
t_{PZL}				7.1	10.6	1	12	
t_{PHZ}	$\overline{OE}$	Y	$C_L = 50\text{ pF}$					ns
t_{PLZ}								

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noise characteristics $V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 4)

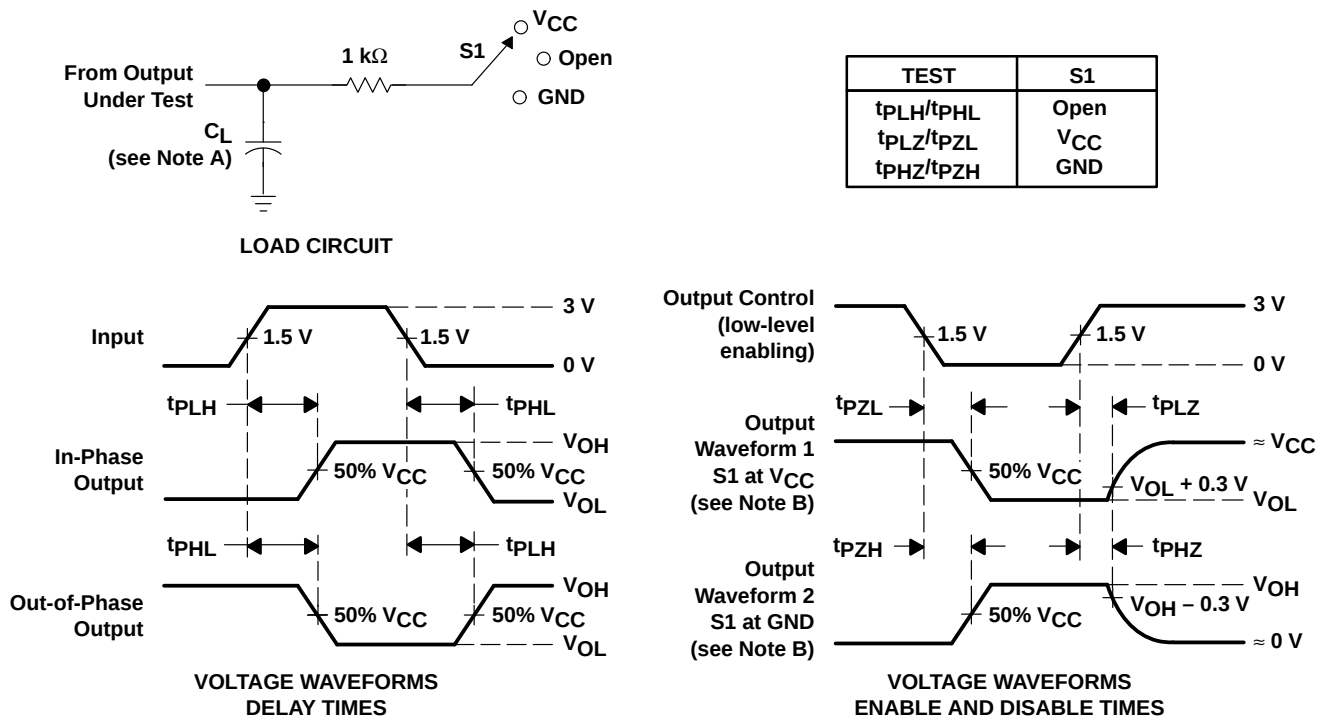
PARAMETER	SN74AHCT257		UNIT
	MIN	MAX	
$V_{OL(P)}$ Quiet output, maximum dynamic V_{OL}		0.8	V
$V_{OL(V)}$ Quiet output, minimum dynamic V_{OL}		-0.8	V
$V_{OH(V)}$ Quiet output, minimum dynamic V_{OH}			V
$V_{IH(D)}$ High-level dynamic input voltage	2		V
$V_{IL(D)}$ Low-level dynamic input voltage	0.8		V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load, $f = 1\text{ MHz}$	20	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r = 3\text{ ns}$, $t_f = 3\text{ ns}$.

D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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