PRODUCT PREVIEW

- **Members of the Texas Instruments** *Widebus*™ **Family**
- **Inputs Are TTL-Voltage Compatible**
- *EPIC*™ **(Enhanced-Performance Implanted CMOS) Process**
- **Distributed V$_{CC}$ and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54AHCT16374 . . . WD PACKAGE
SN74AHCT16374 . . . DGG OR DL PACKAGE
(TOP VIEW)

1$\overline{OE}$	1		48	1CLK
1Q1	2		47	1D1
1Q2	3		46	1D2
GND	4		45	GND
1Q3	5		44	1D3
1Q4	6		43	1D4
V$_{CC}$	7		42	V$_{CC}$
1Q5	8		41	1D5
1Q6	9		40	1D6
GND	10		39	GND
1Q7	11		38	1D7
1Q8	12		37	1D8
2Q1	13		36	2D1
2Q2	14		35	2D2
GND	15		34	GND
2Q3	16		33	2D3
2Q4	17		32	2D4
V$_{CC}$	18		31	V$_{CC}$
2Q5	19		30	2D5
2Q6	20		29	2D6
GND	21		28	GND
2Q7	22		27	2D7
2Q8	23		26	2D8
2$\overline{OE}$	24		25	2CLK

description

The 'AHCT16374 are 16-bit edge-triggered D-type flip-flops with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.
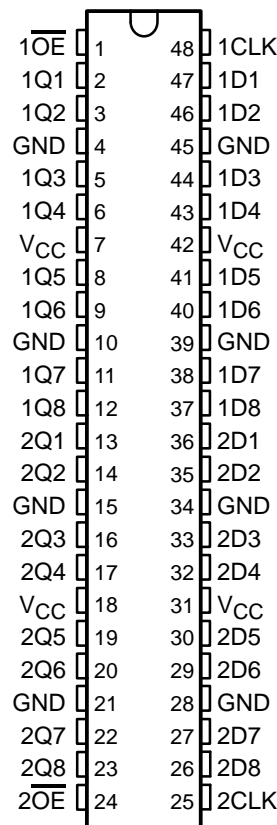
These devices can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels at the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$ does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54AHCT16374 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT16374 is characterized for operation from –40°C to 85°C.

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TEXAS INSTRUMENTS

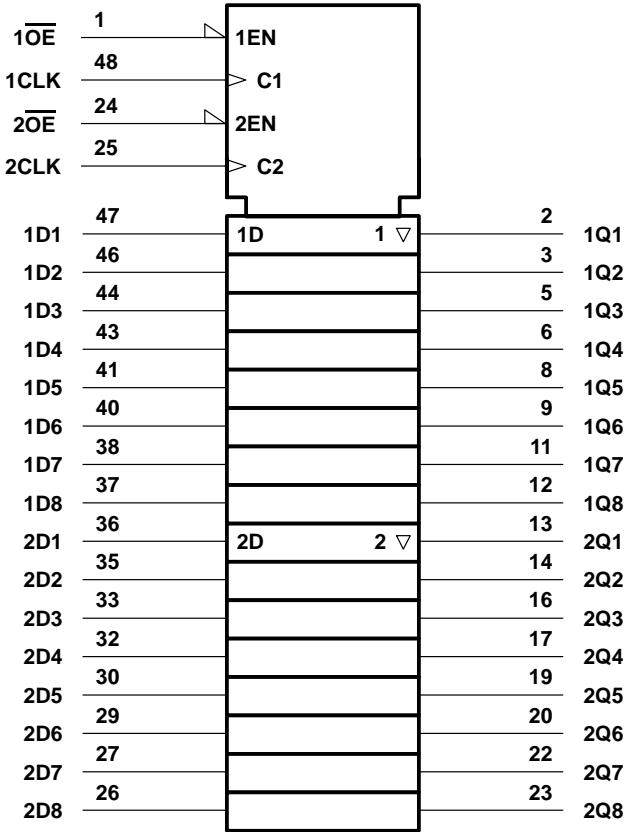POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

1

SN54AHCT16374, SN74AHCT16374
16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH 3-STATE OUTPUTS
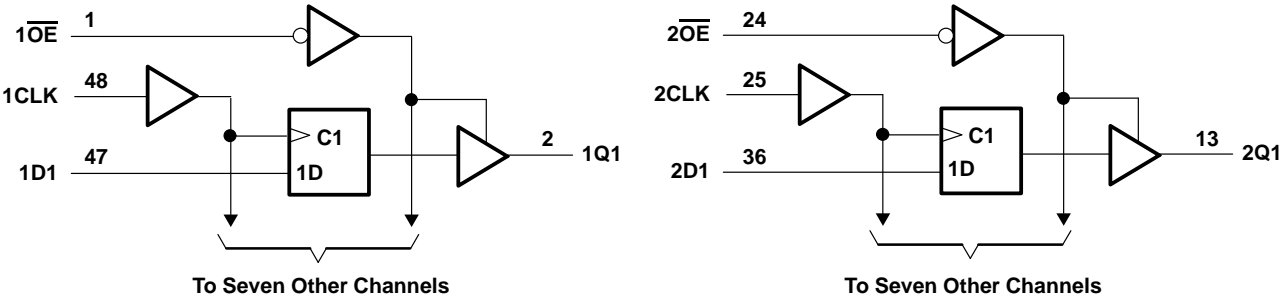SCLS337C – MARCH 1996 – REVISED JUNE 1997

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

PRODUCT PREVIEW

logic symbol[†]

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

To Seven Other Channels

To Seven Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) .... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) .... −20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) .... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) .... ±25 mA
Continuous current through each V_{CC} or GND .... ±75 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package .... 89°C/W
                                                     DL package .... 94°C/W
Storage temperature range, T_{stg} .... −65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		SN54AHCT16374		SN74AHCT16374		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IO}	Input/output voltage, A or B pins	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−8		−8	mA
I_{OL}	Low-level output current		8		8	mA
Δt/Δv	Input transition rise or fall rate		20		20	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHCT16374		SN74AHCT16374		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4	4.5		4.4		4.4		V
	I_{OH} = −8 mA		3.94			3.8		3.8		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
	I_{OL} = 8 mA				0.36		0.44		0.44	
I_{OZ}	V_O = V_{CC} or GND, V_I = V_{IH} or V_{IL}	5.5 V			±0.25		±2.5		±2.5	μA
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40		40	μA
ΔI_{CC}[‡]	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5		1.5	mA
C_i	V_I = V_{CC} or GND	5 V		4	10				10	pF
C_o	V_O = V_{CC} or GND	5 V		6						pF

[‡] This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

PRODUCT PREVIEW

TEXAS INSTRUMENTS

SN54AHCT16374, SN74AHCT16374
16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH 3-STATE OUTPUTS
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timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		SN54AHCT16374		SN74AHCT16374		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, CLK high or low	6.5		6.5		6.5		ns
t_{su}	Setup time, data before CLK↑	2.5		2.5		2.5		ns
t_h	Hold time, data after CLK↑	2.5		2.5		2.5		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54AHCT16374		SN74AHCT16374		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF*	90	140		80		110		MHz
			C_L = 50 pF	85	130		75		75		
t_{PLH}*	CLK	Q	C_L = 15 pF		5.6	9.4	1	10.5	1	10.5	ns
t_{PHL}*					5.6	9.4	1	10.5	1	10.5	
t_{PZH}*	$\overline{OE}$	Q	C_L = 15 pF		6.5	10.2	1	11.5	1	11.5	ns
t_{PZL}*					6.5	10.2	1	11.5	1	11.5	
t_{PHZ}*	$\overline{OE}$	Q	C_L = 15 pF		6.2	10.2	1	11	1	11	ns
t_{PLZ}*					6.2	10.2	1	11	1	11	
t_{PLH}	CLK	Q	C_L = 50 pF		6.4	10.4	1	11.5	1	11.5	ns
t_{PHL}					6.4	10.4	1	11.5	1	11.5	
t_{PZH}	$\overline{OE}$	Q	C_L = 50 pF		7.3	11.2	1	12.5	1	12.5	ns
t_{PZL}					7.3	11.2	1	12.5	1	12.5	
t_{PHZ}	$\overline{OE}$	Q	C_L = 50 pF		7	11.2	1	12	1	12	ns
t_{PLZ}					7	11.2	1	12	1	12	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER		V_{CC}	SN74AHCT16374				UNIT
			T_A = 25°C		MIN	MAX	
			MIN	MAX			
$t_{sk(o)}$	Output skew	5 V $\pm$ 0.5 V		1		1	ns

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

PARAMETER		SN74AHCT16374			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8	1.2	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.8	−1.2	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	3.8			V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

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operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	27	pF

PARAMETER MEASUREMENT INFORMATION
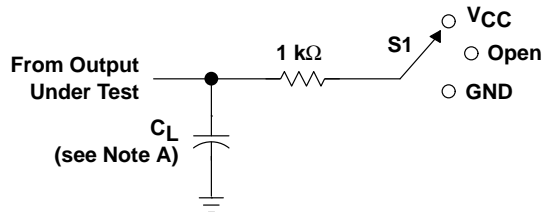
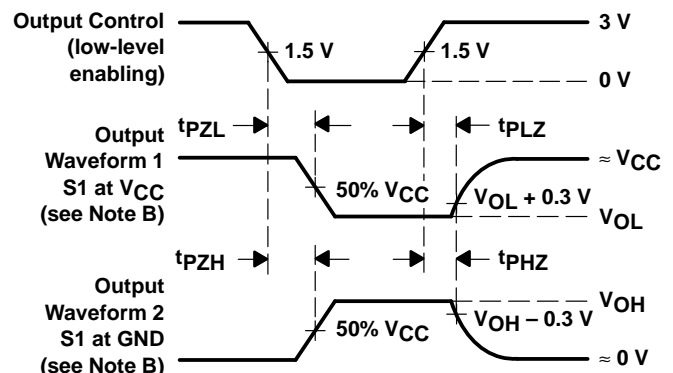| TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT
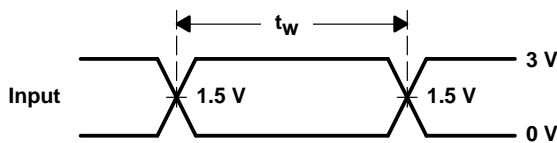
**VOLTAGE WAVEFORMS
PULSE DURATION**
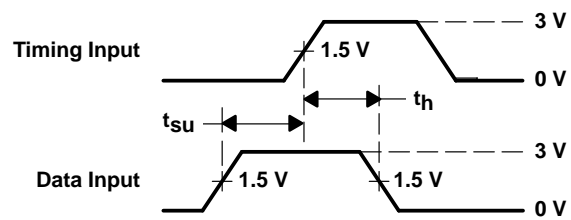
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**
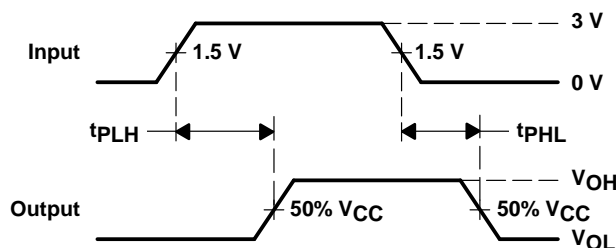
**VOLTAGE WAVEFORMS
DELAY TIMES**

**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES**

NOTES: A. C_L includes probe and jig capacitance.
      B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
        Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
      C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
      D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

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