- **Members of the Texas Instruments**
  Widebus™ **Family**

- **Operating Range 2-V to 5.5-V V_{CC}**

- ***EPIC***™ **(Enhanced-Performance Implanted CMOS) Process**

- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**

- **Flow-Through Architecture Optimizes PCB Layout**

- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

description

The 'AHC16541 are noninverting 16-bit buffers composed of two 8-bit sections with separate output-enable signals. For either 8-bit buffer section, the two output-enable (1$\overline{OE1}$ and 1$\overline{OE2}$ or 2$\overline{OE1}$ and 2$\overline{OE2}$) inputs must be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 8-bit buffer section are in the high-impedance state.

The SN54AHC16541 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC16541 is characterized for operation from –40°C to 85°C.

SN54AHC16541 . . . WD PACKAGE
SN74AHC16541 . . . DGG OR DL PACKAGE
(TOP VIEW)

Pin			Pin
1$\overline{OE1}$	1	48	1$\overline{OE2}$
1Y1	2	47	1A1
1Y2	3	46	1A2
GND	4	45	GND
1Y3	5	44	1A3
1Y4	6	43	1A4
V_{CC}	7	42	V_{CC}
1Y5	8	41	1A5
1Y6	9	40	1A6
GND	10	39	GND
1Y7	11	38	1A7
1Y8	12	37	1A8
2Y1	13	36	2A1
2Y2	14	35	2A2
GND	15	34	GND
2Y3	16	33	2A3
2Y4	17	32	2A4
V_{CC}	18	31	V_{CC}
2Y5	19	30	2A5
2Y6	20	29	2A6
GND	21	28	GND
2Y7	22	27	2A7
2Y8	23	26	2A8
2$\overline{OE1}$	24	25	2$\overline{OE2}$

PRODUCT PREVIEW

FUNCTION TABLE
(each 8-bit section)

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

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logic symbol†

Pin	Signal				Pin	Signal
1	1OE1		&	EN1		
48	1OE2					
24	2OE1		&	EN2		
25	2OE2					

1A1	47	1 1 ▽	2	1Y1
1A2	46		3	1Y2
1A3	44		5	1Y3
1A4	43		6	1Y4
1A5	41		8	1Y5
1A6	40		9	1Y6
1A7	38		11	1Y7
1A8	37		12	1Y8
2A1	36	1 2 ▽	13	2Y1
2A2	35		14	2Y2
2A3	33		16	2Y3
2A4	32		17	2Y4
2A5	30		19	2Y5
2A6	29		20	2Y6
2A7	27		22	2Y7
2A8	26		23	2Y8
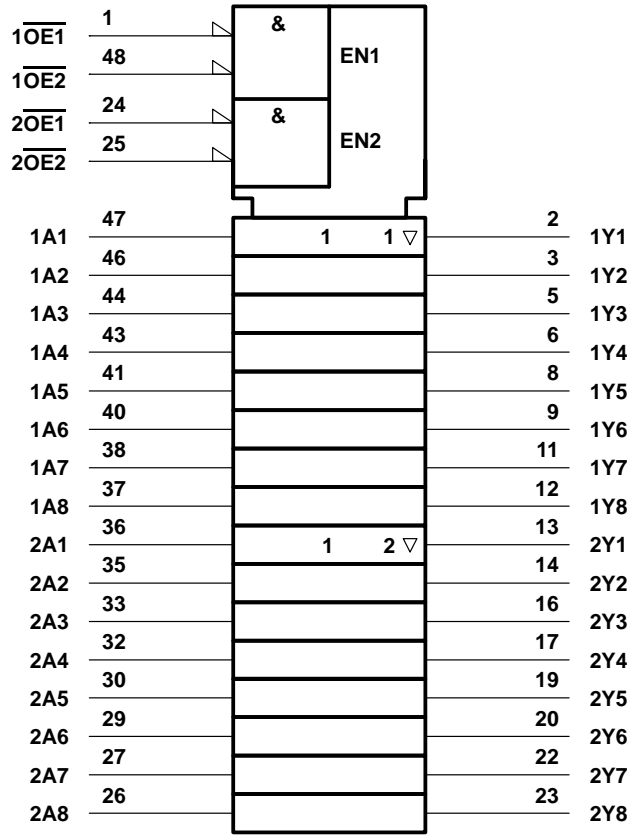
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)
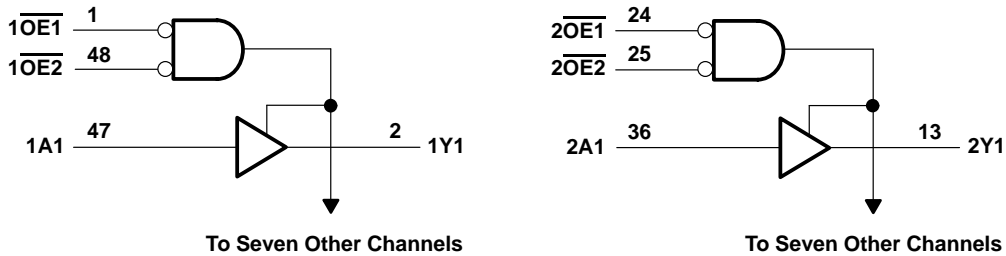
1OE1 1
1OE2 48
1A1 47 ──▷── 2 1Y1

To Seven Other Channels

2OE1 24
2OE2 25
2A1 36 ──▷── 13 2Y1

To Seven Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} . . . . −0.5 V to 7 V

Input voltage range, V_I (see Note 1) . . . . −0.5 V to 7 V

Output voltage range, V_O (see Note 1) . . . . −0.5 V to V_{CC} + 0.5 V

Input clamp current, I_{IK} (V_I < 0) . . . . −20 mA

Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . ±20 mA

Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . ±25 mA

Continuous current through each V_{CC} or GND . . . . ±75 mA

Package thermal impedance, θ_{JA} (see Note 2): DGG package . . . . 89°C/W

DL package . . . . 94°C/W

Storage temperature range, T_{stg} . . . . −65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

			SN54AHC16541		SN74AHC16541		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		−50		−50	μA
		V_{CC} = 3.3 V ± 0.3 V		−4		−4	mA
		V_{CC} = 5 V ± 0.5 V		−8		−8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4		4	mA
		V_{CC} = 5 V ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20		20	
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

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PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHC16541		SN74AHC16541		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = −50 µA	2 V	1.9	2		1.9		1.9		V
			3 V	2.9	3		2.9		2.9		
			4.5 V	4.4	4.5		4.4		4.4		
		I_{OH} = −4 mA	3 V	2.58			2.48		2.48		
		I_{OH} = −8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}		I_{OL} = 50 µA	2 V			0.1		0.1		0.1	V
			3 V			0.1		0.1		0.1	
			4.5 V			0.1		0.1		0.1	
		I_{OL} = 4 mA	3 V			0.36		0.5		0.44	
		I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I_I	Data inputs	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	µA
	Control inputs					±0.1		±1		±1	
I_{OZ}		V_O = V_{CC} or GND, V_I ($\overline{OE}$) = V_{IL} or V_{IH}	5.5 V			±0.25		±2.5		±2.5	µA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40		40	µA
C_i		V_I = V_{CC} or GND	5 V		2	10				10	pF
C_o		V_O = V_{CC} or GND	5 V		4						pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54AHC16541		SN74AHC16541		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}*	A	Y	C_L = 15 pF		5	7	1	8.5	1	8.5	ns
t_{PHL}*					5	7	1	8.5	1	8.5	
t_{PZH}*	$\overline{OE}$	Y	C_L = 15 pF		6	10.5	1	11	1	11	ns
t_{PZL}*					6	10.5	1	11	1	11	
t_{PHZ}*	$\overline{OE}$	Y	C_L = 15 pF		7	11	1	12	1	12	ns
t_{PLZ}*					7	11	1	12	1	12	
t_{PLH}	A	Y	C_L = 50 pF		7.5	10.5	1	12	1	12	ns
t_{PHL}					7.5	10.5	1	12	1	12	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		8	14	1	16	1	16	ns
t_{PZL}					8	14	1	16	1	16	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		9	15.4	1	17.5	1	17.5	ns
t_{PLZ}					9	15.4	1	17.5	1	17.5	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

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switching characteristics over recommended operating free-air temperature range,
V_{CC} = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54AHC16541		SN74AHC16541		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}*	A	Y	C_L = 15 pF		3.5	5	1	6	1	6	ns
t_{PHL}*					3.5	5	1	6	1	6	
t_{PZH}*	$\overline{OE}$	Y	C_L = 15 pF		4.7	7.2	1	8.5	1	8.5	ns
t_{PZL}*					4.7	7.2	1	8.5	1	8.5	
t_{PHZ}*	$\overline{OE}$	Y	C_L = 15 pF		5	7.5	1	8	1	8	ns
t_{PLZ}*					5	7.5	1	8	1	8	
t_{PLH}	A	Y	C_L = 50 pF		5	7	1	8	1	8	ns
t_{PHL}					5	7	1	8	1	8	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		6.2	9.2	1	10.5	1	10.5	ns
t_{PZL}					6.2	9.2	1	10.5	1	10.5	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		6	8.8	1	10	1	10	ns
t_{PLZ}					6	8.8	1	10	1	10	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	SN74AHC16541				UNIT
				T_A = 25°C		MIN	MAX	
				MIN	MAX			
$t_{sk(o)}$	A	Y	3.3 V $\pm$ 0.3 V		1.5		1.5	ns
			5 V $\pm$ 0.5 V		1		1	

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

PARAMETER		SN74AHC16541		UNIT
		MIN	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.7		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5		V
$V_{IL(D)}$	Low-level dynamic input voltage		1.5	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	12	pF

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PARAMETER MEASUREMENT INFORMATION
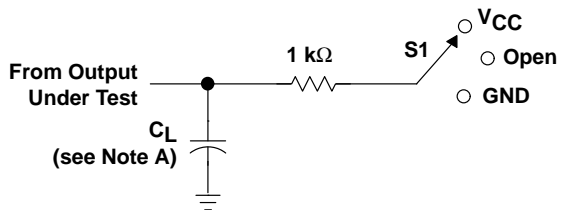
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

VOLTAGE WAVEFORMS
DELAY TIMES

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
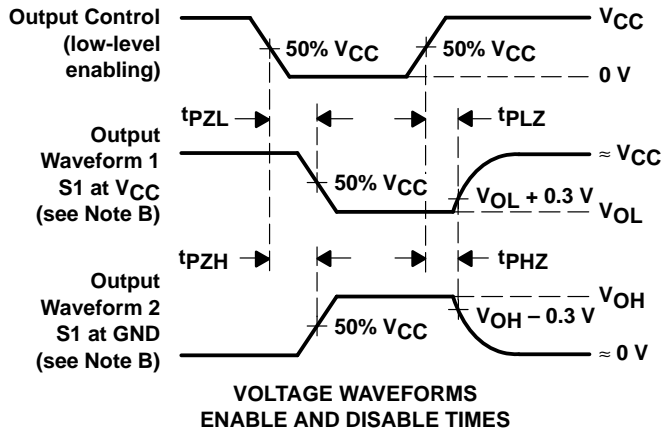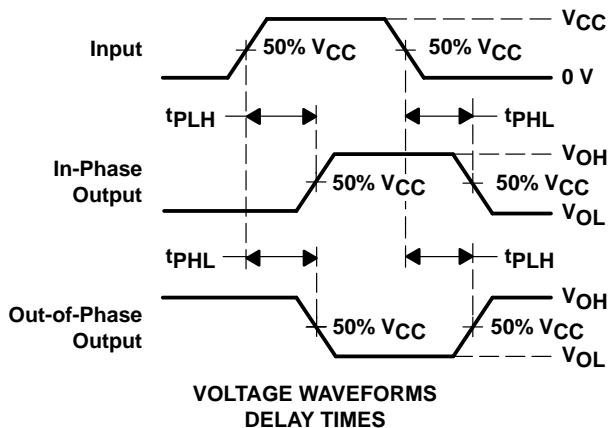
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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