

# SN54AHC16244, SN74AHC16244 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCLS327B – MARCH 1996 – REVISED JUNE 1997

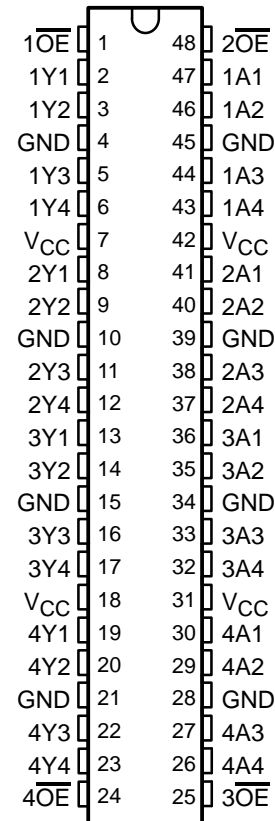
- Members of the Texas Instruments *Widebus*™ Family
- Operating Range 2-V to 5.5-V  $V_{CC}$
- *EPIC*™ (Enhanced-Performance Implanted CMOS) Process
- Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

## description

The 'AHC16244 are 16-bit buffers and line drivers designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide true outputs and symmetrical active-low output-enable ( $\overline{OE}$ ) inputs.

The SN54AHC16244 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74AHC16244 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

SN54AHC16244 . . . WD PACKAGE  
SN74AHC16244 . . . DGG OR DL PACKAGE  
(TOP VIEW)



FUNCTION TABLE  
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z



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PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



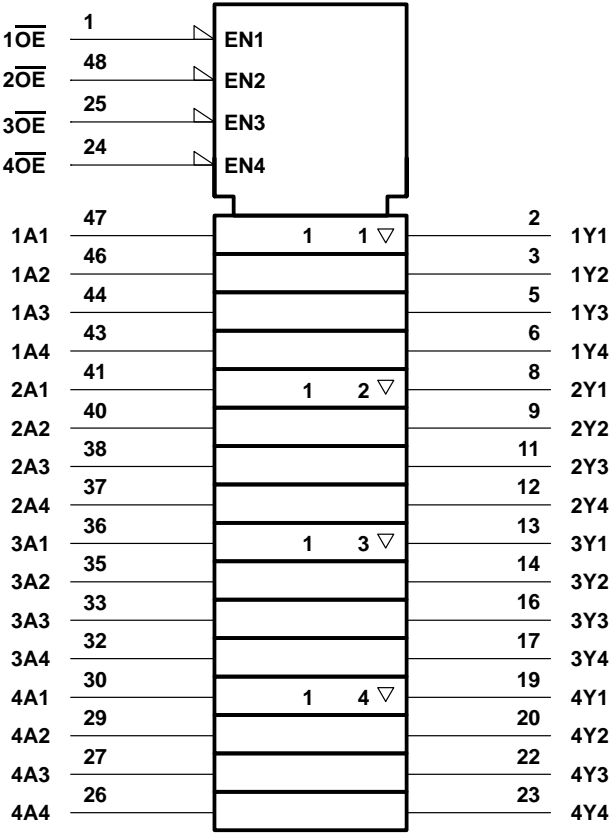
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PRODUCT PREVIEW

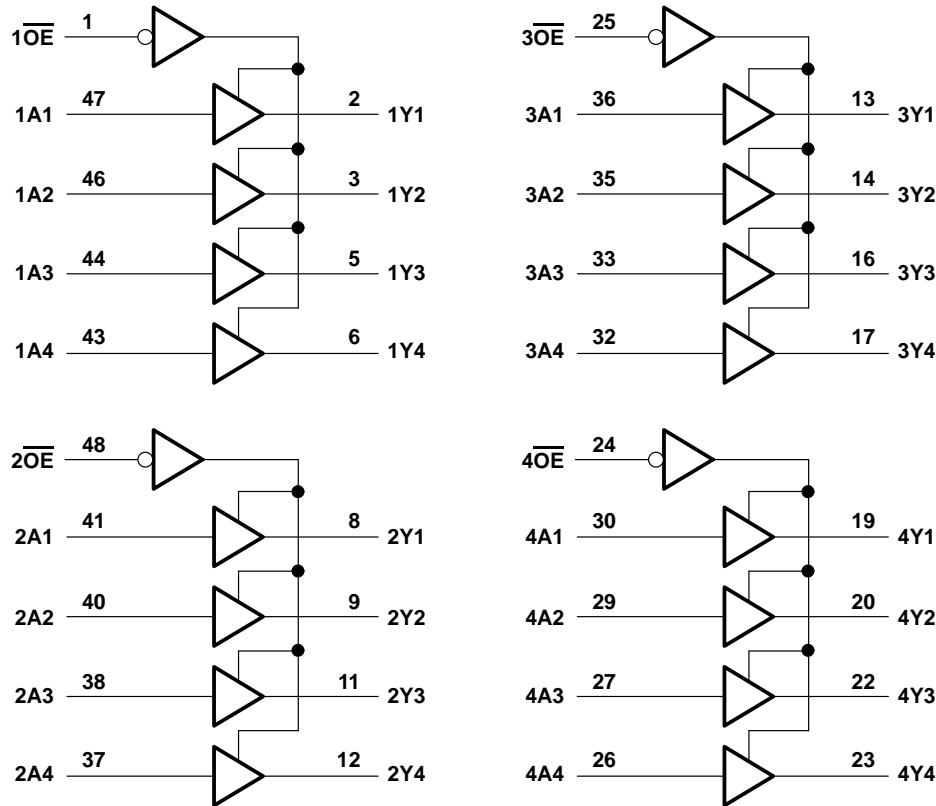
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16-BIT BUFFERS/DRIVERS  
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through each $V_{CC}$ or GND	±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package	89°C/W
DL package	94°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51.

# SN54AHC16244, SN74AHC16244

## 16-BIT BUFFERS/DRIVERS

### WITH 3-STATE OUTPUTS

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#### recommended operating conditions (see Note 3)

			SN54AHC16244		SN74AHC16244		UNIT
			MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage		2	5.5	2	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5		1.5		V
		V <sub>CC</sub> = 3 V	2.1		2.1		
		V <sub>CC</sub> = 5.5 V	3.85		3.85		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V		0.5		0.5	V
		V <sub>CC</sub> = 3 V		0.9		0.9	
		V <sub>CC</sub> = 5.5 V		1.65		1.65	
V <sub>I</sub>	Input voltage		0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2 V		–50		–50	μA
		V <sub>CC</sub> = 3.3 ± 0.3 V		–4		–4	
		V <sub>CC</sub> = 5 ± 0.5 V		–8		–8	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2 V		50		50	μA
		V <sub>CC</sub> = 3.3 ± 0.3 V		4		4	
		V <sub>CC</sub> = 5 ± 0.5 V		8		8	
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 3.3 ± 0.3 V		100		100	ns/V
		V <sub>CC</sub> = 5 ± 0.5 V		20		20	
T <sub>A</sub>	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54AHC16244		SN74AHC16244		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>		I <sub>OH</sub> = –50 μA	2 V	1.9	2		1.9		1.9		V
			3 V	2.9	3		2.9		2.9		
			4.5 V	4.4	4.5		4.4		4.4		
		I <sub>OH</sub> = –4 mA	3 V	2.58			2.48		2.48		
			4.5 V	3.94			3.8		3.8		
V <sub>OL</sub>		I <sub>OL</sub> = 50 μA	2 V			0.1			0.1		V
			3 V			0.1			0.1		
			4.5 V			0.1			0.1		
		I <sub>OL</sub> = 4 mA	3 V			0.36			0.5		
			4.5 V			0.36			0.5		
I <sub>I</sub>	Data inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			±0.1			±1		μA
	Control inputs					±0.1			±1		
I <sub>OZ</sub>		V <sub>O</sub> = V <sub>CC</sub> or GND, V <sub>I</sub> (OE) = V <sub>IL</sub> or V <sub>IH</sub>	5.5 V			±0.25			±2.5		μA
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			4			40		μA
C <sub>i</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		2	10				10	pF
C <sub>O</sub>		V <sub>O</sub> = V <sub>CC</sub> or GND	5 V		3.5						pF



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switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC16244		SN74AHC16244		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}^*$	A	Y	$C_L = 15\text{ pF}$		5.8	8.4	1	10	1	10	ns
$t_{PHL}^*$					5.8	8.4	1	10	1	10	
$t_{PZH}^*$	$\overline{OE}$	Y	$C_L = 15\text{ pF}$		6.6	10.6	1	12.5	1	12.5	ns
$t_{PZL}^*$					6.6	10.6	1	12.5	1	12.5	
$t_{PHZ}^*$	$\overline{OE}$	Y	$C_L = 15\text{ pF}$		5	9.7	1	11	1	11	ns
$t_{PLZ}^*$					5	9.7	1	11	1	11	
$t_{PLH}$	A	Y	$C_L = 50\text{ pF}$		8.3	11.9	1	13.5	1	13.5	ns
$t_{PHL}$					8.3	11.9	1	13.5	1	13.5	
$t_{PZH}$	$\overline{OE}$	Y	$C_L = 50\text{ pF}$		9.1	14.1	1	16	1	16	ns
$t_{PZL}$					9.1	14.1	1	16	1	16	
$t_{PHZ}$	$\overline{OE}$	Y	$C_L = 50\text{ pF}$		10.3	14	1	16	1	16	ns
$t_{PLZ}$					10.3	14	1	16	1	16	

\* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC16244		SN74AHC16244		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}^*$	A	Y	$C_L = 15\text{ pF}$		3.9	5.5	1	6.5	1	6.5	ns
$t_{PHL}^*$					3.9	5.5	1	6.5	1	6.5	
$t_{PZH}^*$	$\overline{OE}$	Y	$C_L = 15\text{ pF}$		4.7	7.3	1	8.5	1	8.5	ns
$t_{PZL}^*$					4.7	7.3	1	8.5	1	8.5	
$t_{PHZ}^*$	$\overline{OE}$	Y	$C_L = 15\text{ pF}$		5	7.2	1	8.5	1	8.5	ns
$t_{PLZ}^*$					5	7.2	1	8.5	1	8.5	
$t_{PLH}$	A	Y	$C_L = 50\text{ pF}$		5.4	7.5	1	8.5	1	8.5	ns
$t_{PHL}$					5.4	7.5	1	8.5	1	8.5	
$t_{PZH}$	$\overline{OE}$	Y	$C_L = 50\text{ pF}$		6.2	9.3	1	10.5	1	10.5	ns
$t_{PZL}$					6.2	9.3	1	10.5	1	10.5	
$t_{PHZ}$	$\overline{OE}$	Y	$C_L = 50\text{ pF}$		6.7	9.2	1	10.5	1	10.5	ns
$t_{PLZ}$					6.7	9.2	1	10.5	1	10.5	

\* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

output-skew characteristics,  $C_L = 50\text{ pF}$  (see Note 4)

PARAMETER	VCC	SN74AHC16244				UNIT
		TA = 25°C		MIN	MAX	
		MIN	MAX			
t <sub>sk(o)</sub> Output skew	3.3 V ± 0.3 V	1.5		1.5		ns
	5 V ± 0.5 V	1		1		

NOTE 4: Characteristics are determined during product characterization and ensured by design.

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noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 5)

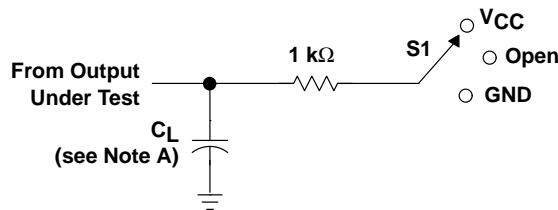
PARAMETER	SN74AHC16244			UNIT
	MIN	TYP	MAX	
$V_{OL(P)}$ Quiet output, maximum dynamic $V_{OL}$		0.5		V
$V_{OL(V)}$ Quiet output, minimum dynamic $V_{OL}$		-0.2		V
$V_{OH(V)}$ Quiet output, minimum dynamic $V_{OH}$		4.8		V
$V_{IH(D)}$ High-level dynamic input voltage	3.5			V
$V_{IL(D)}$ Low-level dynamic input voltage			1.5	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

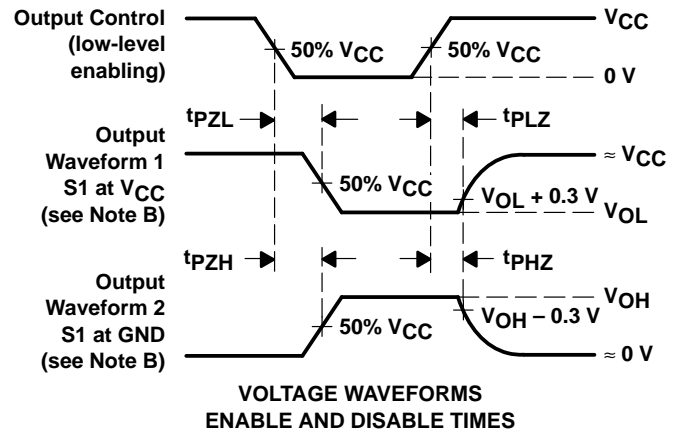
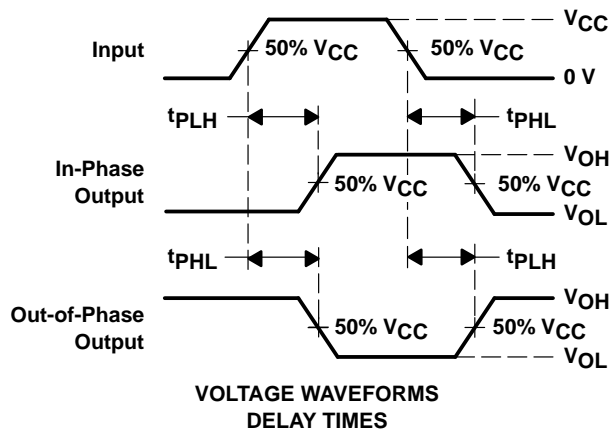
PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	No load, $f = 1\text{ MHz}$	8.6	pF

## PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



NOTES: A.  $C_L$  includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r = 3\text{ ns}$ ,  $t_f = 3\text{ ns}$ .

D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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