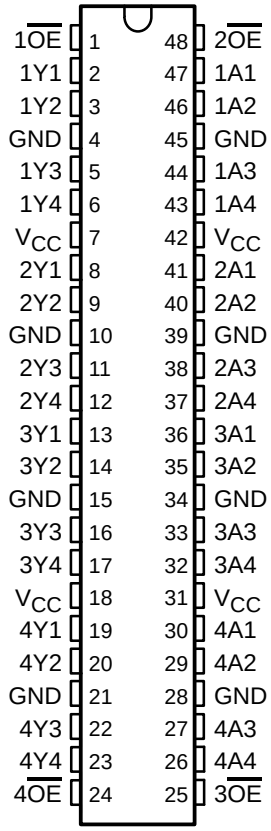
- **Members of the Texas Instruments *Widebus*™ Family**
- **Operating Range 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54AHC16240 . . . WD PACKAGE
SN74AHC16240 . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)



description

The ’AHC16240 are 16-bit buffers and line drivers designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide inverting outputs and symmetrical active-low output-enable ($\overline{OE}$) inputs.

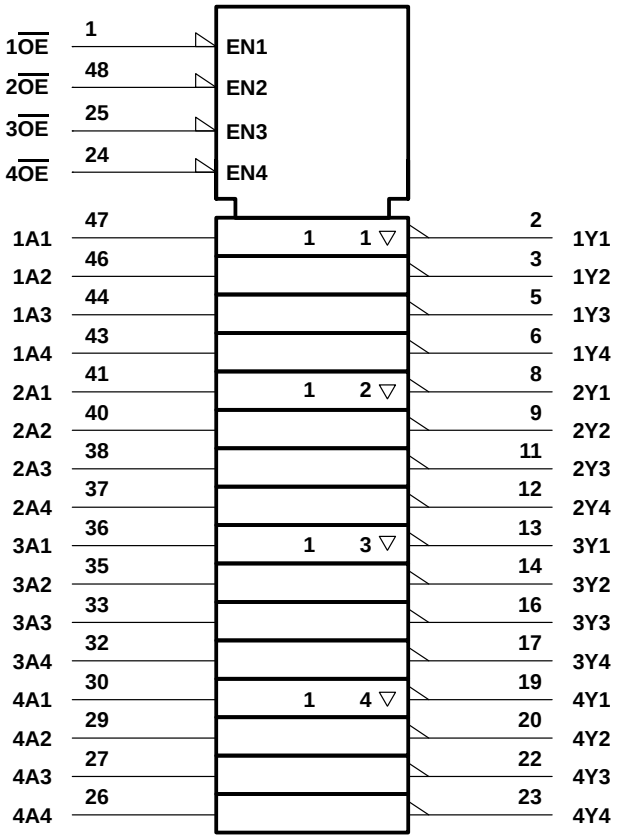
The SN54AHC16240 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC16240 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 4-bit buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

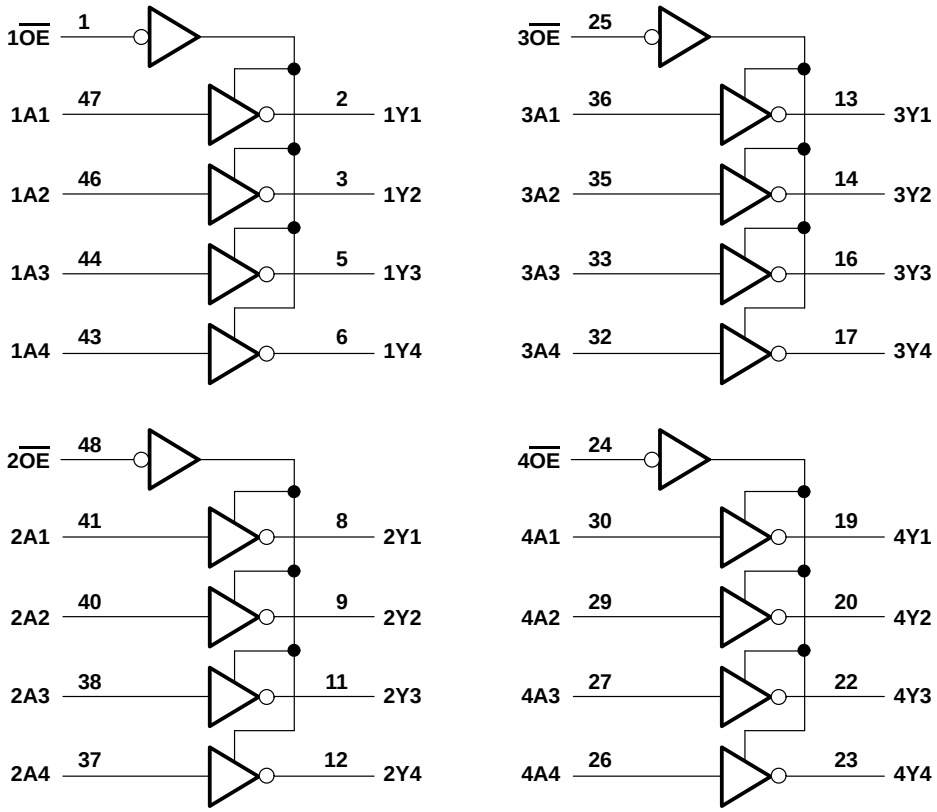
PRODUCT PREVIEW

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . –20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through each V_{CC} or GND . . . . . ±75 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package . . . . . 89°C/W
DGV package . . . . . 93°C/W
DL package . . . . . 94°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

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recommended operating conditions (see Note 3)

			SN54AHC16240		SN74AHC16240		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50		–50	μA
		V_{CC} = 3.3 ± 0.3 V		–4		–4	mA
		V_{CC} = 5 ± 0.5 V		–8		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 3.3 ± 0.3 V		4		4	mA
		V_{CC} = 5 ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 ± 0.3 V		100		100	ns/V
		V_{CC} = 5 ± 0.5 V		20		20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHC16240		SN74AHC16240		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = –50 μA	2 V	1.9	2		1.9		1.9		V
			3 V	2.9	3		2.9		2.9		
			4.5 V	4.4	4.5		4.4		4.4		
		I_{OH} = –4 mA	3 V	2.58			2.48		2.48		
		I_{OH} = –8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}		I_{OL} = 50 μA	2 V			0.1		0.1		0.1	V
			3 V			0.1		0.1		0.1	
			4.5 V			0.1		0.1		0.1	
		I_{OL} = 4 mA	3 V			0.36		0.5		0.44	
		I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I_I	Data inputs	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
	Control inputs					±0.1		±1		±1	
I_{OZ}		V_O = V_{CC} or GND, V_I ($\overline{OE}$) = V_{IL} or V_{IH}	5.5 V			±0.25		±2.5		±2.5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40		40	μA
C_i		V_I = V_{CC} or GND	5 V		2.5	10				10	pF
C_o		V_O = V_{CC} or GND	5 V		3.5						pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54AHC16240		SN74AHC16240		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}*	A	Y	C_L = 15 pF		5.3	7.5	1	9	1	9	ns
t_{PHL}*					5.3	7.5	1	9	1	9	
t_{PZH}*	$\overline{OE}$	Y	C_L = 15 pF		6.6	10.6	1	12.5	1	12.5	ns
t_{PZL}*					6.6	10.6	1	12.5	1	12.5	
t_{PHZ}*	$\overline{OE}$	Y	C_L = 15 pF		7.8	11.5	1	12.5	1	12.5	ns
t_{PLZ}*					7.8	11.5	1	12.5	1	12.5	
t_{PLH}	A	Y	C_L = 50 pF		7.8	11	1	12.5	1	12.5	ns
t_{PHL}					7.8	11	1	12.5	1	12.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		9.1	14.1	1	16	1	16	ns
t_{PZL}					9.1	14.1	1	16	1	16	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		10.3	14	1	16	1	16	ns
t_{PLZ}					10.3	14	1	16	1	16	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54AHC16240		SN74AHC16240		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}*	A	Y	C_L = 15 pF		3.6	5.5	1	6.5	1	6.5	ns
t_{PHL}*					3.6	5.5	1	6.5	1	6.5	
t_{PZH}*	$\overline{OE}$	Y	C_L = 15 pF		4.7	7.3	1	8.5	1	8.5	ns
t_{PZL}*					4.7	7.3	1	8.5	1	8.5	
t_{PHZ}*	$\overline{OE}$	Y	C_L = 15 pF		5.2	7.2	1	8.5	1	8.5	ns
t_{PLZ}*					5.2	7.2	1	8.5	1	8.5	
t_{PLH}	A	Y	C_L = 50 pF		5.1	7.5	1	8.5	1	8.5	ns
t_{PHL}					5.1	7.5	1	8.5	1	8.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		6.2	9.3	1	10.5	1	10.5	ns
t_{PZL}					6.2	9.3	1	10.5	1	10.5	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		6.7	9.2	1	10.5	1	10.5	ns
t_{PLZ}					6.7	9.2	1	10.5	1	10.5	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER		V_{CC}	SN74AHC16240				UNIT
			T_A = 25°C		MIN	MAX	
			MIN	MAX			
$t_{sk(o)}$	Output skew	3.3 V ± 0.3 V		1.5		1.5	ns
		5 V ± 0.5 V		1		1	

NOTE 4: Characteristics are determined during product characterization and ensured by design.

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noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

PARAMETER		SN74AHC16240			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.6		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.6		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.6		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

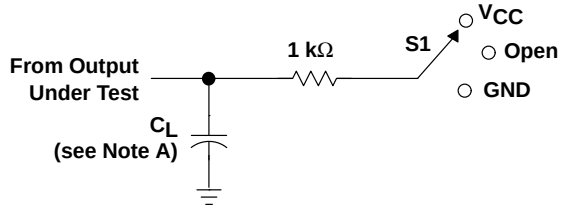
NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	10	pF

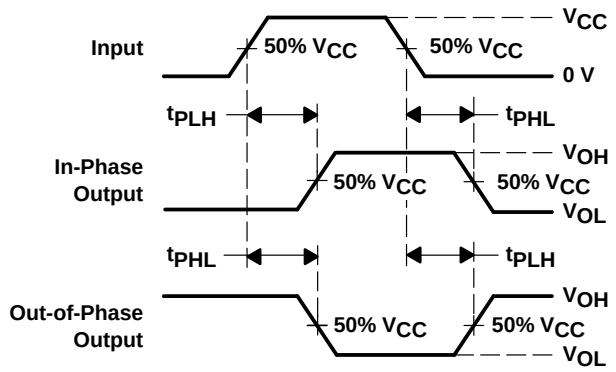
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

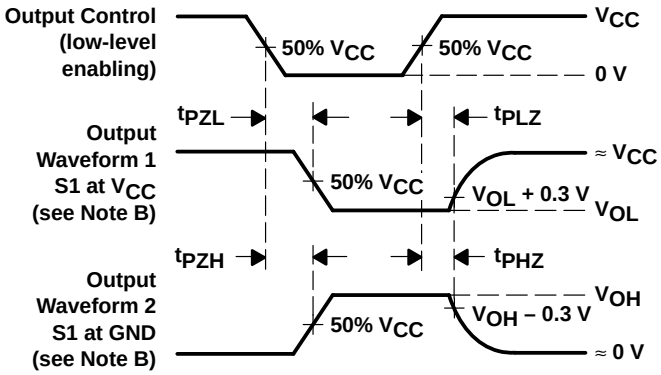


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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