

SN54HC377, SN74HC377 OCTAL D-TYPE FLIP-FLOPS WITH CLOCK ENABLE

SCLS307A – JANUARY 1996 – REVISED MAY 1997

- Eight Flip-Flops With Single-Rail Outputs
- Clock Enable Latched to Avoid False Clocking
- Applications Include:
 - Buffer/Storage Registers
 - Shift Registers
 - Pattern Generators
- Package Options Include Plastic Small-Outline (DW) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

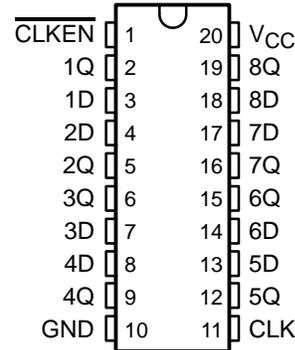
description

These devices are positive-edge-triggered octal D-type flip-flops with an enable input. The 'HC377 are similar to the 'HC273 but feature a latched clock-enable ($\overline{\text{CLKEN}}$) input instead of a common clear.

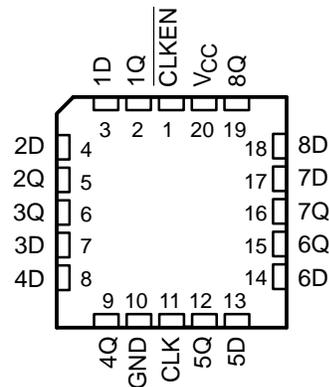
Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock (CLK) pulse if $\overline{\text{CLKEN}}$ is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When CLK is at either the high or low level, the D input has no effect at the output. These devices are designed to prevent false clocking by transitions at $\overline{\text{CLKEN}}$.

The SN54HC377 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74HC377 is characterized for operation from -40°C to 85°C .

SN54HC377 . . . J OR W PACKAGE
SN74HC377 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC377 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{\text{CLKEN}}$	CLK	D	Q
H	X	X	Q_0
L	\uparrow	H	H
L	\uparrow	L	L
X	L	X	Q_0



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

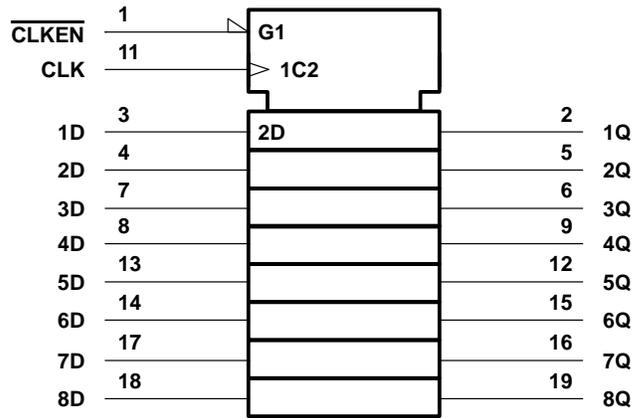
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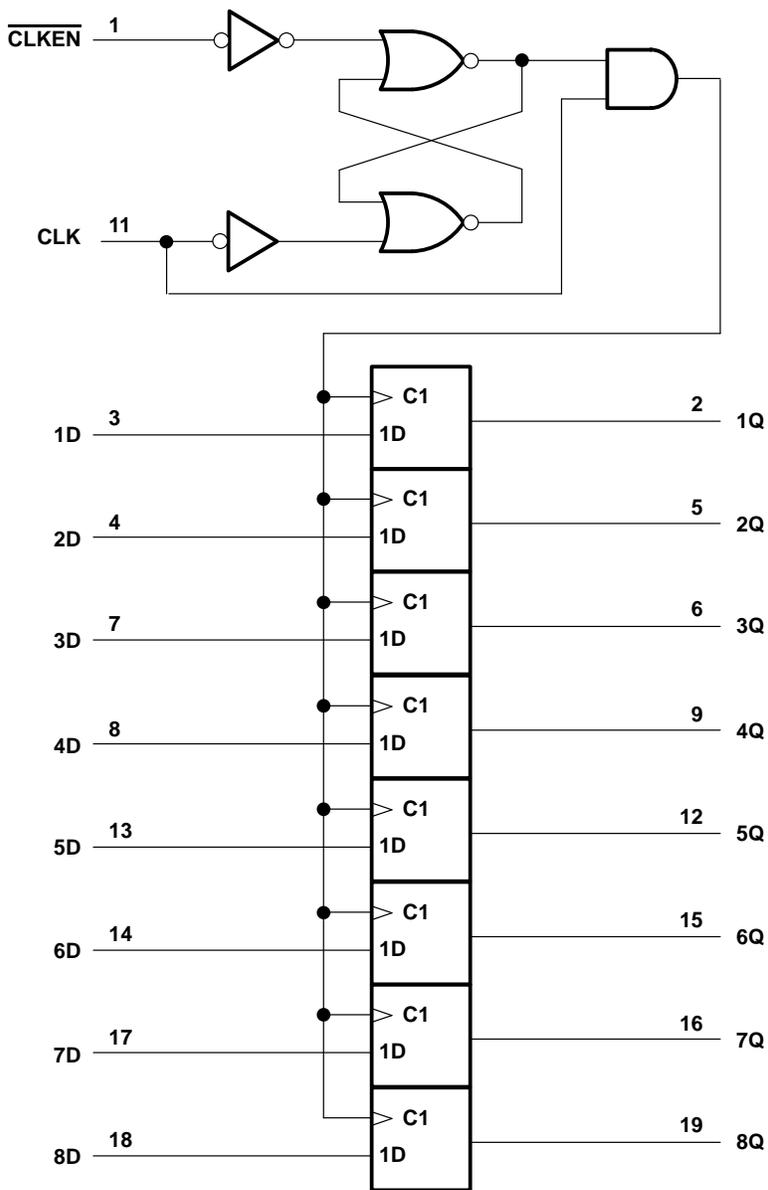
SCLS307A – JANUARY 1996 – REVISED MAY 1997

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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SCLS307A – JANUARY 1996 – REVISED MAY 1997

absolute maximum ratings over operating free-air temperature†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 50 mA
Package thermal impedance, θ_{JA} (see Note 2): DW package	97°C/W
N package	67°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		SN54HC377			SN74HC377			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	2	5	6	2	5	6	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V		1.5	1.5		V	
		$V_{CC} = 4.5$ V		3.15	3.15			
		$V_{CC} = 6$ V		4.2	4.2			
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V		0	0.5	0	0.5	V
		$V_{CC} = 4.5$ V		0	1.35	0	1.35	
		$V_{CC} = 6$ V		0	1.8	0	1.8	
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	$V_{CC} = 2$ V		0	1000	0	1000	ns
		$V_{CC} = 4.5$ V		0	500	0	500	
		$V_{CC} = 6$ V		0	400	0	400	
T_A	Operating free-air temperature	-55		125	-40		85	°C



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SCLS307A – JANUARY 1996 – REVISED MAY 1997

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	T _A = 25°C			SN54HC377		SN74HC377		UNIT	
				MIN	TYP	MAX	MIN	MAX	MIN	MAX		
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = -20 μA	2 V	1.9	1.998		1.9		1.9	V		
			4.5 V	4.4	4.499		4.4		4.4			
			6 V	5.9	5.999		5.9		5.9			
		I _{OH} = -4 mA	4.5 V	3.98	4.3		3.7		3.84			
		I _{OH} = -5.2 mA	6 V	5.48	5.8		5.2		5.34			
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V	
			4.5 V		0.001	0.1		0.1		0.1		
			6 V		0.001	0.1		0.1		0.1		
		I _{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33		
		I _{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33		
I _I	V _I = V _{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA	
I _{CC}	V _I = V _{CC} or 0, I _O = 0		6 V				8		160		80	μA
C _i			2 V to 6 V			3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

	V _{CC}	T _A = 25°C		SN54HC377		SN74HC377		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock} Clock frequency	2 V	0	5	0	3	0	4	MHz
	4.5 V	0	25	0	16	0	20	
	6 V	0	29	0	19	0	23	
t _w Pulse duration, CLK high or low	2 V	100		150		125		ns
	4.5 V	20		30		25		
	6 V	17		25		21		
t _{su} Setup time before CLK↑	D	2 V	100		150		125	ns
		4.5 V	20		30		25	
		6 V	17		25		21	
	CLKEN high or low	2 V	100		150		125	
		4.5 V	20		30		25	
		6 V	17		25		21	
t _h Hold time after CLK↑	CLKEN inactive or active, data	2 V	5		5		5	ns
		4.5 V	5		5		5	
		6 V	5		5		5	



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SCLS307A – JANUARY 1996 – REVISED MAY 1997

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

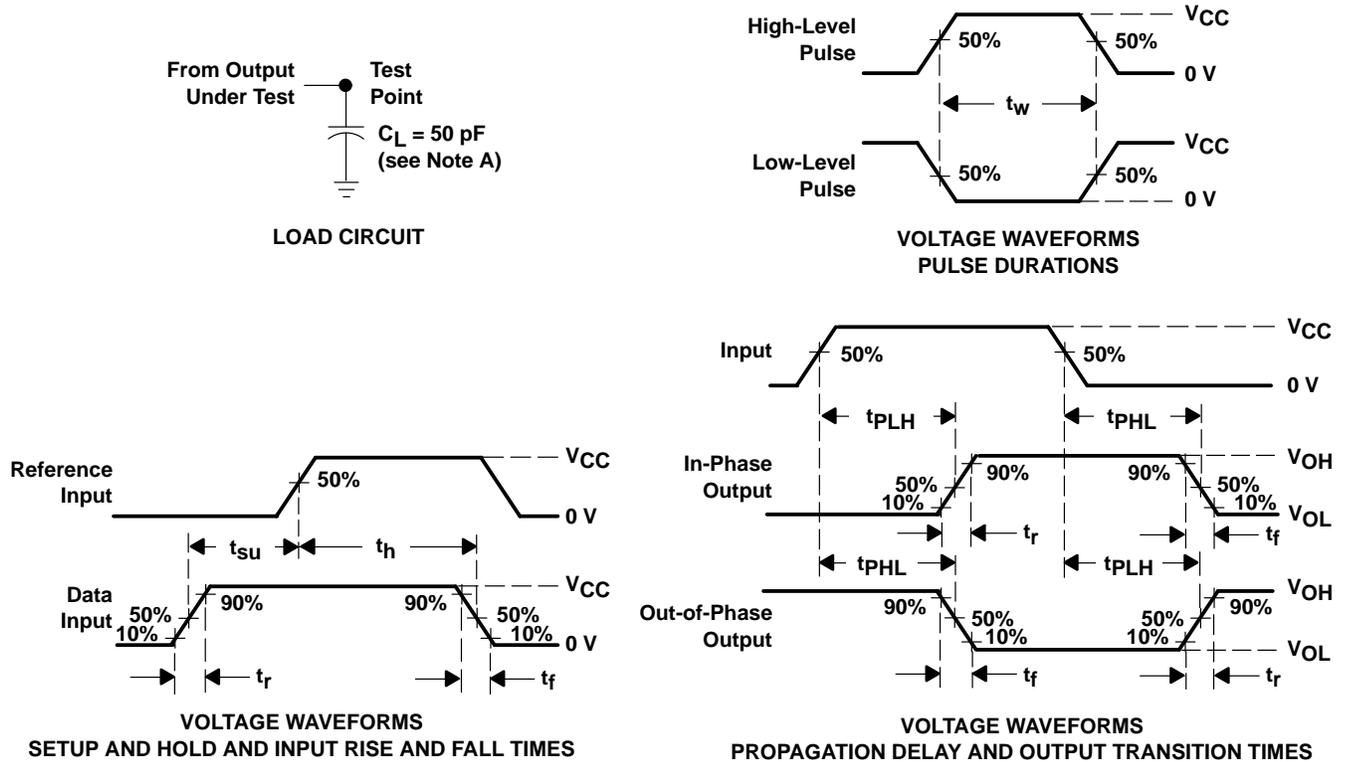
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HC377		SN74HC377		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	5	11		3		4	MHz	
			4.5 V	25	54		16		20		
			6 V	29	64		19		23		
t_{pd}	CLK	Any	2 V		56	160		240		200	ns
			4.5 V		15	32		48		40	
			6 V		12	27		41		34	
t_t		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per flip-flop	No load	30	pF



PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 6 \text{ ns}$, $t_f = 6 \text{ ns}$.
 - C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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