

SN54HC645, SN74HC645 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCLS304A – JANUARY 1996 – REVISED MAY 1997

- True Logic
- High-Current 3-State Outputs Can Drive up to 15 LSTTL Loads
- Package Options Include Plastic Small-Outline (DW) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

description

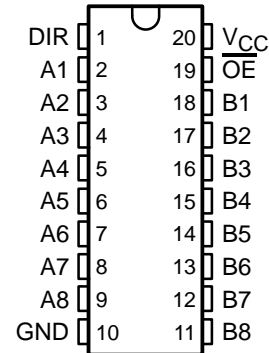
These octal bus transceivers are designed for asynchronous two-way communication between data buses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending upon the level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so the buses are effectively isolated.

The SN54HC645 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74HC645 is characterized for operation from -40°C to 85°C .

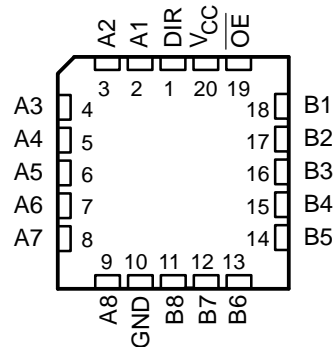
FUNCTION TABLE

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

SN54HC645 . . . J OR W PACKAGE
SN74HC645 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC645 . . . FK PACKAGE
(TOP VIEW)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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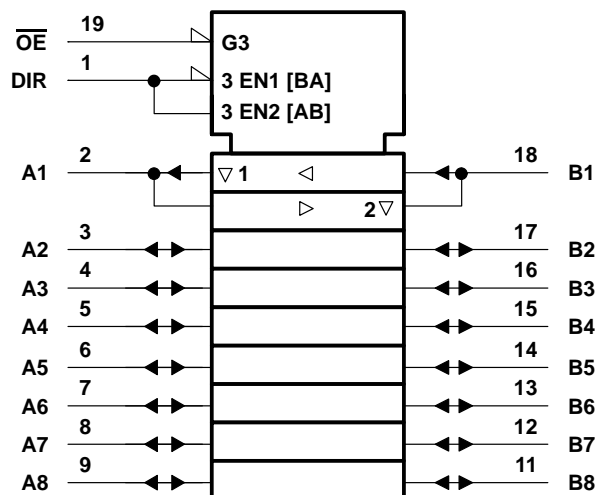
SN54HC645, SN74HC645

OCTAL BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

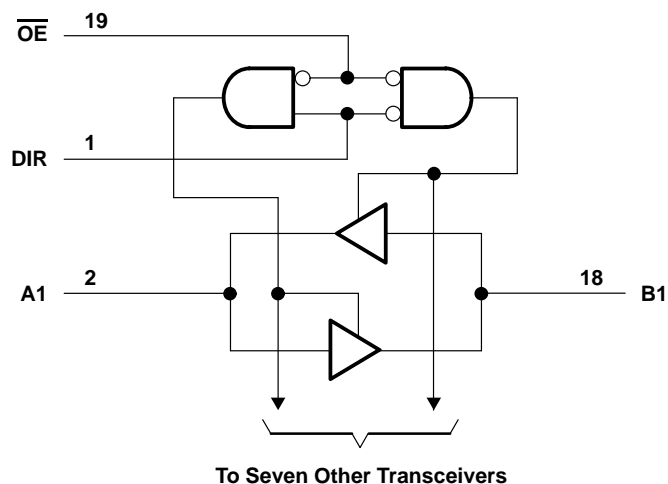
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±35 mA
Continuous current through V_{CC} or GND	±70 mA
Package thermal impedance, θ_{JA} (see Note 2): DW package	97°C/W
N package	67°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JEDEC 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

			SN54HC645			SN74HC645			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V	1.5			1.5			V
		$V_{CC} = 4.5$ V	3.15			3.15			
		$V_{CC} = 6$ V	4.2			4.2			
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V	0	0.5		0	0.5		V
		$V_{CC} = 4.5$ V	0	1.35		0	1.35		
		$V_{CC} = 6$ V	0	1.8		0	1.8		
V_I	Input voltage		0	V_{CC}		0	V_{CC}		V
V_O	Output voltage		0	V_{CC}		0	V_{CC}		V
t_t	Input transition (rise and fall) time	$V_{CC} = 2$ V	0	1000		0	1000		ns
		$V_{CC} = 4.5$ V	0	500		0	500		
		$V_{CC} = 6$ V	0	400		0	400		
T_A	Operating free-air temperature		–55	125		–40	85		°C

SN54HC645, SN74HC645

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54HC645		SN74HC645		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}		V _I = V _{IH} or V _{IL}	I _{OH} = -20 µA	2 V	1.9	1.998	1.9		1.9		V
				4.5 V	4.4	4.499	4.4		4.4		
				6 V	5.9	5.999	5.9		5.9		
			I _{OH} = -6 mA	4.5 V	3.98	4.3	3.7		3.84		
			I _{OH} = -7.8 mA	6 V	5.48	5.8	5.2		5.34		
V _{OL}		V _I = V _{IH} or V _{IL}	I _{OL} = 20 µA	2 V		0.002	0.1		0.1		V
				4.5 V		0.001	0.1		0.1		
				6 V		0.001	0.1		0.1		
			I _{OL} = 6 mA	4.5 V		0.17	0.26		0.4		
			I _{OL} = 7.8 mA	6 V		0.15	0.26		0.4		
I _I	DIR or $\overline{\text{OE}}$	V _I = V _{CC} or 0	6 V		±0.1	±100	±1000		±1000		nA
I _{OZ}	A or B	V _O = V _{CC} or 0	6 V		±0.01	±0.5	±10		±5		µA
I _{CC}		V _I = V _{CC} or 0, I _O = 0	6 V			8	160		80		µA
C _i	DIR or $\overline{\text{OE}}$		2 V to 6 V		3	10	10		10		pF

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HC645		SN74HC645		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	B or A	2 V		40	105		160		130	ns
			4.5 V		15	21		32		26	
			6 V		12	18		27		22	
t _{en}	$\overline{\text{OE}}$	A or B	2 V		125	230		340		290	ns
			4.5 V		23	46		68		58	
			6 V		20	39		58		49	
t _{dis}	$\overline{\text{OE}}$	A or B	2 V		74	200		300		250	ns
			4.5 V		25	40		60		50	
			6 V		21	34		51		43	
t _t		A or B	2 V		20	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	



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switching characteristics over recommended operating free-air temperature range, $C_L = 150 \text{ pF}$
(unless otherwise noted) (see Figure 1)

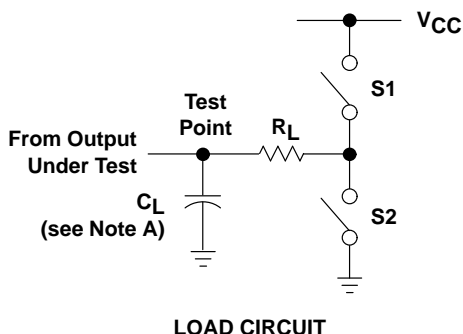
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HC645		SN74HC645		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	2 V		54	135		200		170	ns
			4.5 V		18	27		40		34	
			6 V		15	23		34		29	
t_{en}	\overline{OE}	A or B	2 V		150	270		405		335	ns
			4.5 V		31	54		81		67	
			6 V		25	46		69		56	
t_t		A or B	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

operating characteristics, $T_A = 25^\circ\text{C}$

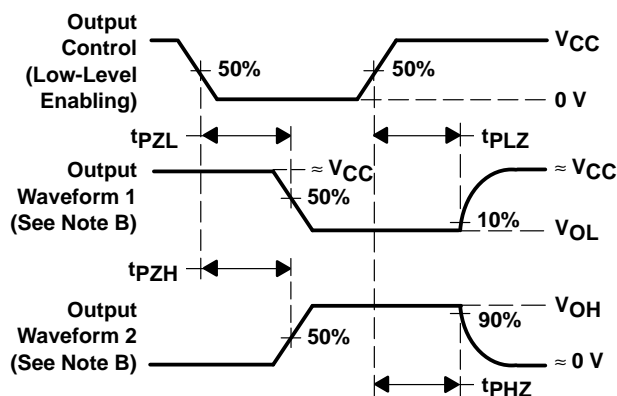
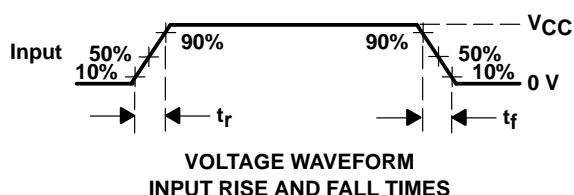
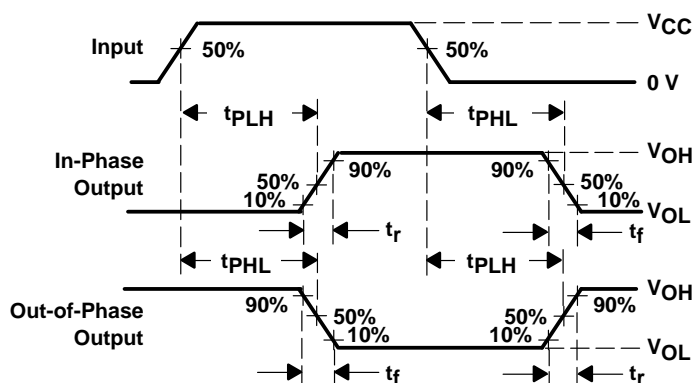
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	No load	40	pF



PARAMETER MEASUREMENT INFORMATION



PARAMETER	R_L	C_L	S1	S2
t_{en}	1 k Ω	50 pF or 150 pF	Open	Closed
			Closed	Open
t_{dis}	1 k Ω	50 pF	Open	Closed
			Closed	Open
t_{pd} or t_t	—	50 pF or 150 pF	Open	Open



- NOTES:
- C_L includes probe and test-fixture capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 - The outputs are measured one at a time with one input transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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