

SN54AHCT138, SN74AHCT138 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

SCLS266D – DECEMBER 1995 – REVISED MAY 1997

- Inputs Are TTL-Voltage Compatible
- **EPIC™** (Enhanced-Performance Implanted CMOS) Process
- Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems
- Incorporate Three Enable Inputs to Simplify Cascading and/or Data Reception
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

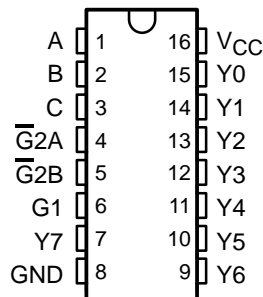
description

The 'AHCT138 3-line to 8-line decoders/demultiplexers are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

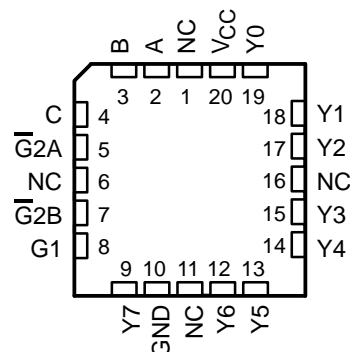
The conditions at the binary-select inputs and the three enable inputs select one of eight output lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The SN54AHCT138 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AHCT138 is characterized for operation from -40°C to 85°C .

SN54AHCT138 . . . J OR W PACKAGE
SN74AHCT138 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AHCT138 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

PRODUCT PREVIEW



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**TEXAS
INSTRUMENTS**

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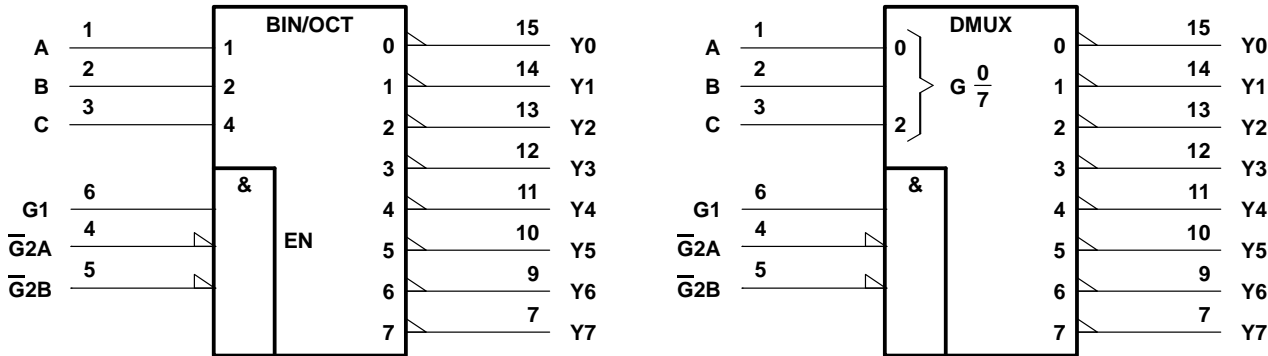
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FUNCTION TABLE

ENABLE INPUTS			SELECT INPUTS			OUTPUTS							
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

logic symbols (alternatives)†

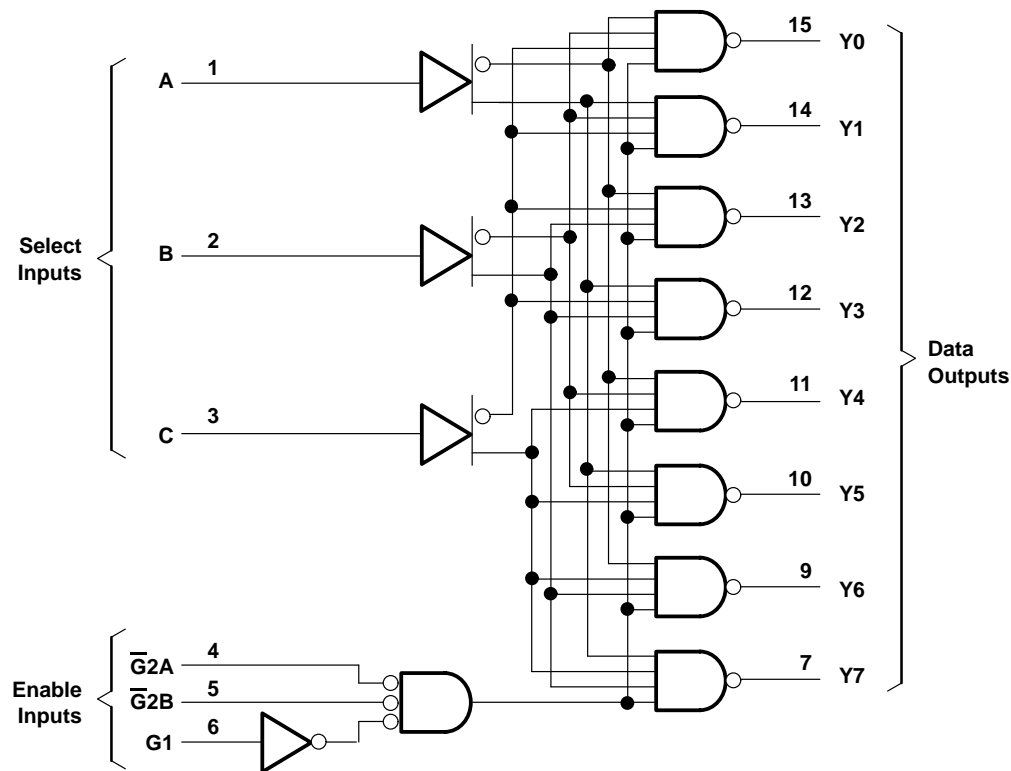


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

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logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±75 mA
Package thermal impedance, θ_{JA} (see Note 2):	
D package	113°C/W
DB package	131°C/W
N package	78°C/W
PW package	149°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

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recommended operating conditions (see Note 3)

		SN54AHCT138		SN74AHCT138		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–8		–8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20		20	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			SN54AHCT138		SN74AHCT138		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$I_{OH} = -50\ \mu\text{A}$	4.5 V	4.4	4.5		4.4		4.4		V
	$I_{OH} = -8\ \text{mA}$		3.94			3.8		3.8		
V_{OL}	$I_{OL} = 50\ \mu\text{A}$	4.5 V			0.1		0.1		0.1	V
	$I_{OL} = 8\ \text{mA}$				0.36		0.44		0.44	
I_I	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1		± 1	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			4		40		40	μA
ΔI_{CC}^\dagger	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5		1.5	mA
C_i	$V_I = V_{CC}$ or GND	5 V			4 10				10	pF

[†] This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC} .

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHCT138				UNIT	
				T _A = 25°C			MIN		MAX
				MIN	TYP	MAX			
t _{PLH} *	A, B, C	Any Y	C _L = 15 pF	7.6	10.4	1	12	ns	
t _{PHL} *				7.6	10.4	1	12		
t _{PLH} *	G1	Any Y	C _L = 15 pF	6.6	9.1	1	10.5	ns	
t _{PHL} *				6.6	9.1	1	10.5		
t _{PLH} *	$\overline{G}2A, \overline{G}2B$	Any Y	C _L = 15 pF	7	9.6	1	11	ns	
t _{PHL} *				7	9.6	1	11		
t _{PLH}	A, B, C	Any Y	C _L = 50 pF	8.1	11.4	1	13	ns	
t _{PHL}				8.1	11.4	1	13		
t _{PLH}	G1	Any Y	C _L = 50 pF	7.1	10.1	1	11.5	ns	
t _{PHL}				7.1	10.1	1	11.5		
t _{PLH}	$\overline{G}2A, \overline{G}2B$	Any Y	C _L = 50 pF	7.5	10.6	1	12	ns	
t _{PHL}				7.5	10.6	1	12		

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHCT138				UNIT	
				T _A = 25°C			MIN		MAX
				MIN	TYP	MAX			
t _{PLH}	A, B, C	Any Y	C _L = 15 pF	7.6	10.4	1	12	ns	
t _{PHL}				7.6	10.4	1	12		
t _{PLH}	G1	Any Y	C _L = 15 pF	6.6	9.1	1	10.5	ns	
t _{PHL}				6.6	9.1	1	10.5		
t _{PLH}	$\overline{G}2A, \overline{G}2B$	Any Y	C _L = 15 pF	7	9.6	1	11	ns	
t _{PHL}				7	9.6	1	11		
t _{PLH}	A, B, C	Any Y	C _L = 50 pF	8.1	11.4	1	13	ns	
t _{PHL}				8.1	11.4	1	13		
t _{PLH}	G1	Any Y	C _L = 50 pF	7.1	10.1	1	11.5	ns	
t _{PHL}				7.1	10.1	1	11.5		
t _{PLH}	$\overline{G}2A, \overline{G}2B$	Any Y	C _L = 50 pF	7.5	10.6	1	12	ns	
t _{PHL}				7.5	10.6	1	12		

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

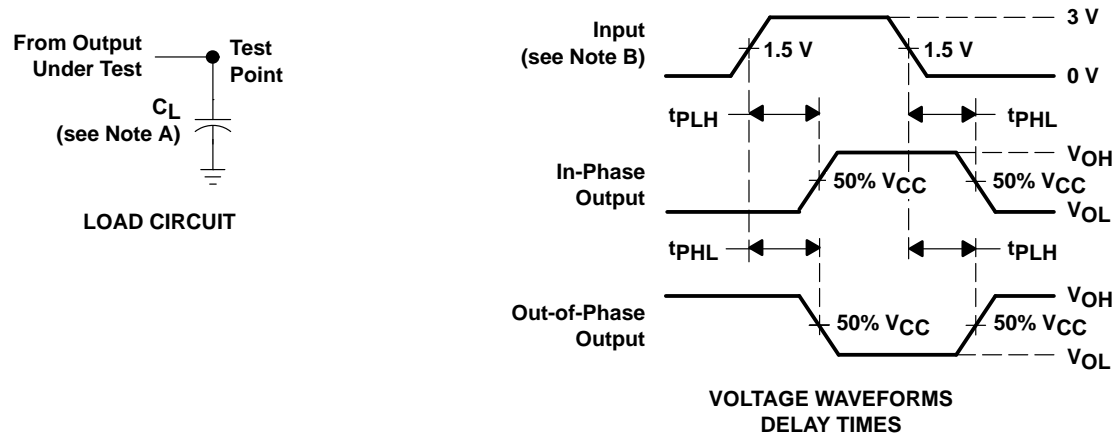
PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load, $f = 1\text{ MHz}$	49	pF



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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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APPLICATION INFORMATION

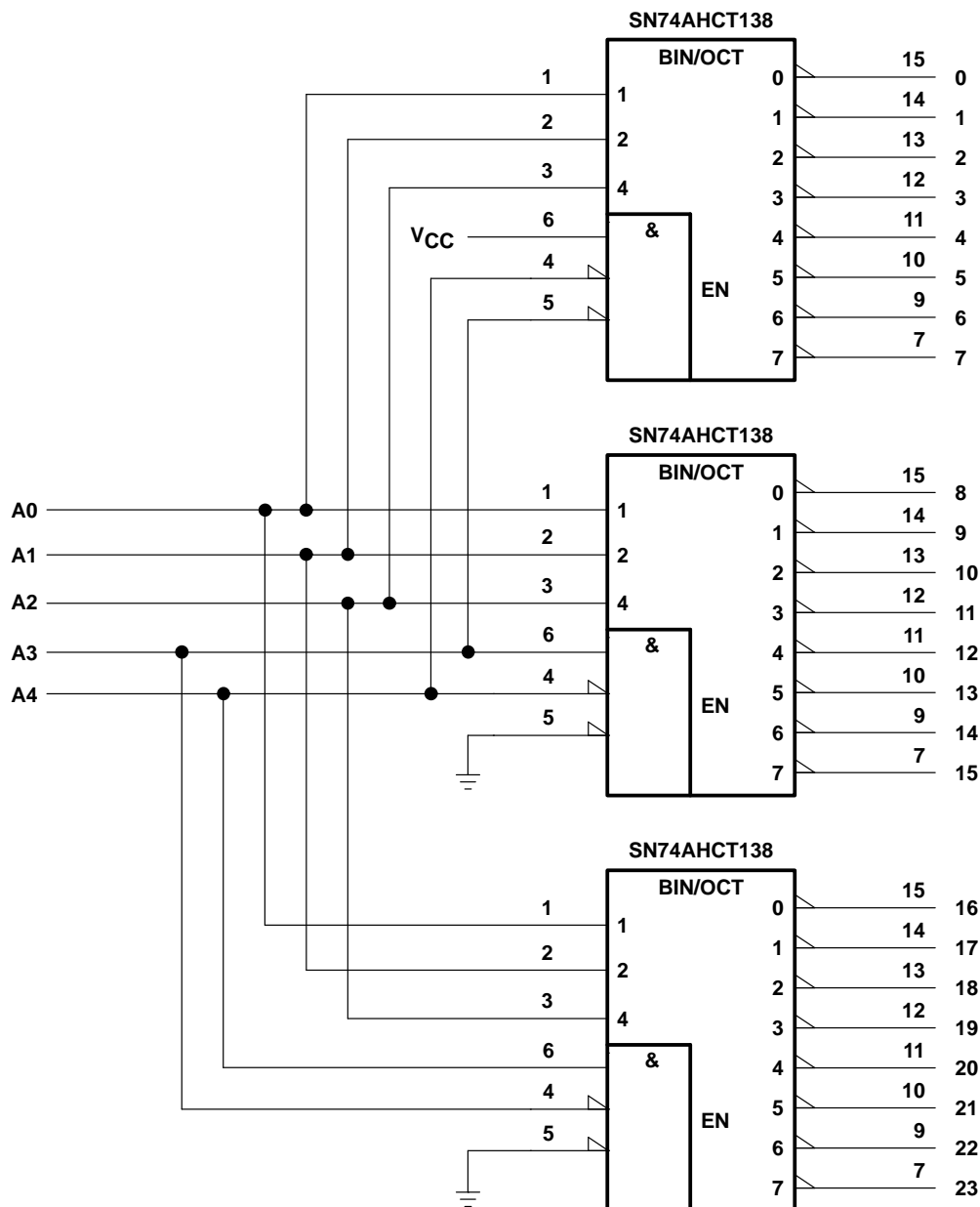


Figure 2. 24-Bit Decoding Scheme

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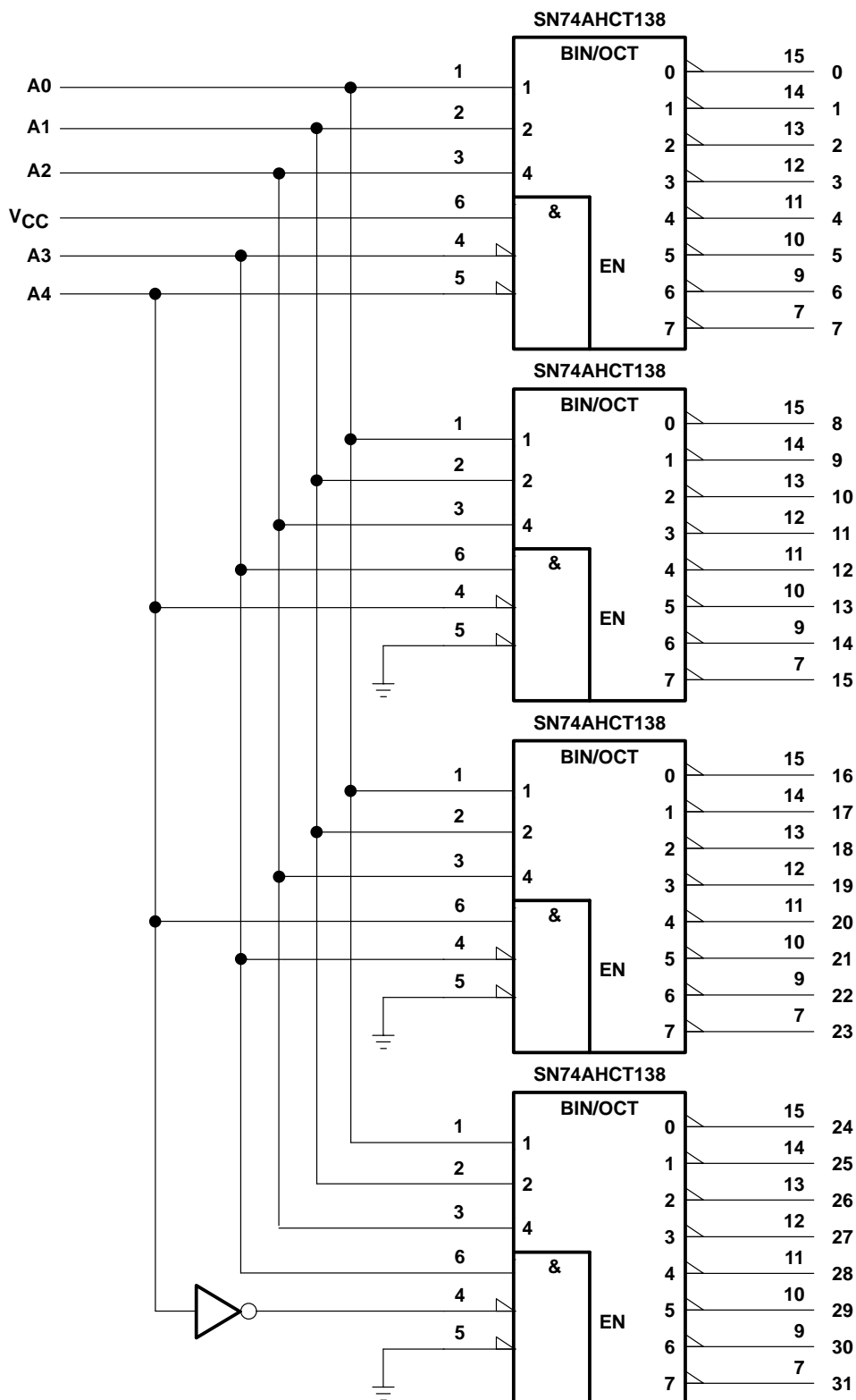


Figure 3. 32-Bit Decoding Scheme

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