- **Operating Range 2-V to 5.5-V V$_{CC}$**
- ***EPIC***™ **(Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHC540 . . . J OR W PACKAGE
SN74AHC540 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)

$\overline{OE1}$	1	20	V$_{CC}$
A1	2	19	$\overline{OE2}$
A2	3	18	Y1
A3	4	17	Y2
A4	5	16	Y3
A5	6	15	Y4
A6	7	14	Y5
A7	8	13	Y6
A8	9	12	Y7
GND	10	11	Y8

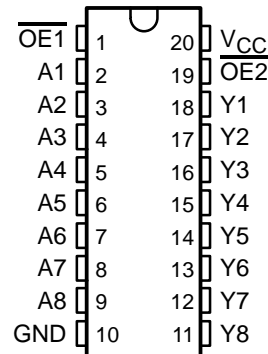**SN54AHC540 . . . FK PACKAGE**
(TOP VIEW)

description

The 'AHC540 octal buffers/drivers are ideal for driving bus lines or buffer memory address registers. These devices feature inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.
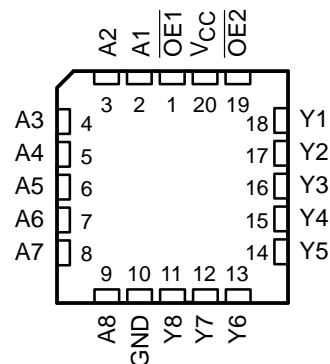
The 3-state control gate is a two-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state. The outputs provide inverted data when they are not in the high-impedance state.

The SN54AHC540 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC540 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer/driver)

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

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logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

To Seven Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} .... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) .... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) .... –20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) .... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) .... ±25 mA
Continuous current through V_{CC} or GND .... ±75 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package .... 115°C/W
　　　　　　　　　　　　　　　　　　　　　　　　DW package .... 97°C/W
　　　　　　　　　　　　　　　　　　　　　　　　N package .... 67°C/W
　　　　　　　　　　　　　　　　　　　　　　　　PW package .... 128°C/W
Storage temperature range, T_{stg} .... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
 functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
 implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES:　1.　The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
　　　　　2.　The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace
　　　　　　　length of zero.

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recommended operating conditions (see Note 3)

			SN54AHC540		SN74AHC540		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		−50		−50	µA
		V_{CC} = 3.3 V ± 0.3 V		−4		−4	mA
		V_{CC} = 5 V ± 0.5 V		−8		−8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	µA
		V_{CC} = 3.3 V ± 0.3 V		4		4	mA
		V_{CC} = 5 V ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20		20	
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHC540		SN74AHC540		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = −50 µA	2 V	1.9	2		1.9		1.9		V
			3 V	2.9	3		2.9		2.9		
			4.5 V	4.4	4.5		4.4		4.4		
		I_{OH} = −4 mA	3 V	2.58			2.48		2.48		
		I_{OH} = −8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}		I_{OL} = 50 µA	2 V			0.1		0.1		0.1	V
			3 V			0.1		0.1		0.1	
			4.5 V			0.1		0.1		0.1	
		I_{OL} = 4 mA	3 V			0.36		0.5		0.44	
		I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I_I	Data inputs	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	µA
	Control inputs					±0.1		±1		±1	
I_{OZ}†		V_O = V_{CC} or GND, V_I ($\overline{OE}$) = V_{IL} or V_{IH}	5.5 V			±0.25		±2.5		±2.5	µA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40		40	µA
C_i		V_I = V_{CC} or GND	5 V		2	10				10	pF
C_o		V_O = V_{CC} or GND	5 V		4						pF

† For I/O pins, the parameter I_{OZ} includes the input leakage current.

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3

switching characteristics over recommended operating free-air temperature range,
$V_{CC} = 3.3$ V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHC540					UNIT
				$T_A = 25°C$			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A	Y	$C_L = 15$ pF		4.8	7	1	8.5	ns
t_{PHL}*					4.8	7	1	8.5	
t_{PZH}*	$\overline{OE}$	Y	$C_L = 15$ pF		6.8	10.5	1	12.5	ns
t_{PZL}*					6.8	10.5	1	12.5	
t_{PHZ}*	$\overline{OE}$	Y	$C_L = 15$ pF		6.8	10.5	1	12.5	ns
t_{PLZ}*					6.8	10.5	1	12.5	
t_{PLH}	A	Y	$C_L = 50$ pF		7.3	10.5	1	12	ns
t_{PHL}					7.3	10.5	1	12	
t_{PZH}	$\overline{OE}$	Y	$C_L = 50$ pF		8	14	1	16	ns
t_{PZL}					8	14	1	16	
t_{PHZ}	$\overline{OE}$	Y	$C_L = 50$ pF		8	15.4	1	17.5	ns
t_{PLZ}					8	15.4	1	17.5	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range,
$V_{CC} = 3.3$ V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHC540					UNIT
				$T_A = 25°C$			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A	Y	$C_L = 15$ pF		4.8	7	1	8.5	ns
t_{PHL}					4.8	7	1	8.5	
t_{PZH}	$\overline{OE}$	Y	$C_L = 15$ pF		6.8	10.5	1	12.5	ns
t_{PZL}					6.8	10.5	1	12.5	
t_{PHZ}	$\overline{OE}$	Y	$C_L = 15$ pF		6.8	10.5	1	12.5	ns
t_{PLZ}					6.8	10.5	1	12.5	
t_{PLH}	A	Y	$C_L = 50$ pF		7.3	10.5	1	12	ns
t_{PHL}					7.3	10.5	1	12	
t_{PZH}	$\overline{OE}$	Y	$C_L = 50$ pF		8	14	1	16	ns
t_{PZL}					8	14	1	16	
t_{PHZ}	$\overline{OE}$	Y	$C_L = 50$ pF		8	15.4	1	17.5	ns
t_{PLZ}					8	15.4	1	17.5	

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switching characteristics over recommended operating free-air temperature range,
V_{CC} **= 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHC540 $T_A = 25°C$					UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{PLH}*	A	Y	C_L = 15 pF		3.7	5	1	6	ns
t_{PHL}*					3.7	5	1	6	
t_{PZH}*	$\overline{OE}$	Y	C_L = 15 pF		4.7	7.2	1	8.5	ns
t_{PZL}*					4.7	7.2	1	8.5	
t_{PHZ}*	$\overline{OE}$	Y	C_L = 15 pF		4.5	6.8	1	8	ns
t_{PLZ}*					4.5	6.8	1	8	
t_{PLH}	A	Y	C_L = 50 pF		5.2	7	1	8	ns
t_{PHL}					5.2	7	1	8	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		6.2	9.2	1	10.5	ns
t_{PZL}					6.2	9.2	1	10.5	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		6	8.8	1	10	ns
t_{PLZ}					6	8.8	1	10	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range,
V_{CC} **= 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHC540 $T_A = 25°C$					UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A	Y	C_L = 15 pF		3.7	5	1	6	ns
t_{PHL}					3.7	5	1	6	
t_{PZH}	$\overline{OE}$	Y	C_L = 15 pF		4.7	7.2	1	8.5	ns
t_{PZL}					4.7	7.2	1	8.5	
t_{PHZ}	$\overline{OE}$	Y	C_L = 15 pF		4.5	6.8	1	8	ns
t_{PLZ}					4.5	6.8	1	8	
t_{PLH}	A	Y	C_L = 50 pF		5.2	7	1	8	ns
t_{PHL}					5.2	7	1	8	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		6.2	9.2	1	10.5	ns
t_{PZL}					6.2	9.2	1	10.5	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		6	8.8	1	10	ns
t_{PLZ}					6	8.8	1	10	

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	SN74AHC540 $T_A = 25°C$		MIN	MAX	UNIT
				MIN	MAX			
$t_{sk(o)}$	A	Y	3.3 V $\pm$ 0.3 V		1.5		1.5	ns
			5 V $\pm$ 0.5 V		1		1	

NOTE 4:   Characteristics are determined during product characterization and ensured by design.

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noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

PARAMETER		SN74AHC540 MIN	SN74AHC540 MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.7		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5		V
$V_{IL(D)}$	Low-level dynamic input voltage		1.5	V

NOTE 5:   Characteristics are determined during product characterization and ensured by design for surface-mount packages only.
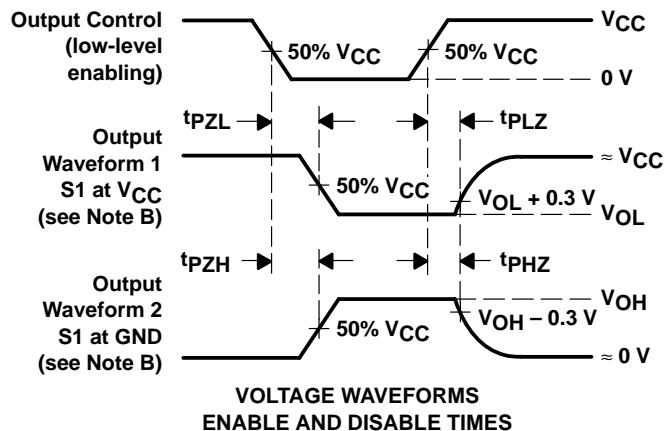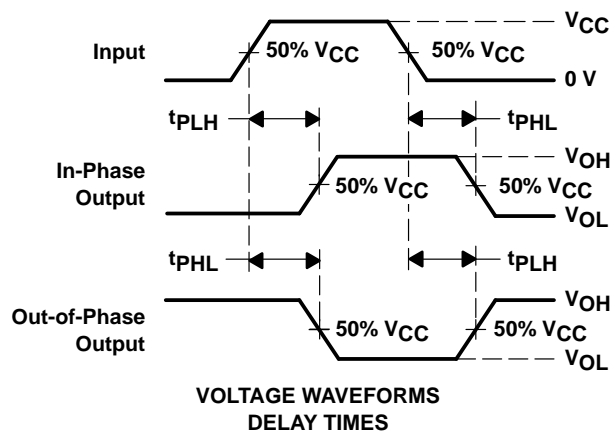
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	12	pF

PARAMETER MEASUREMENT INFORMATION
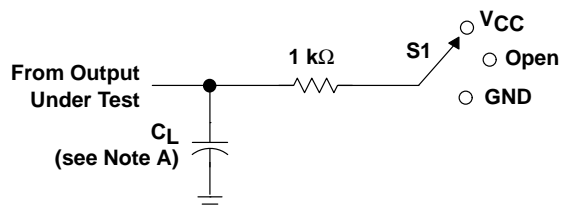
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

VOLTAGE WAVEFORMS
DELAY TIMES

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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