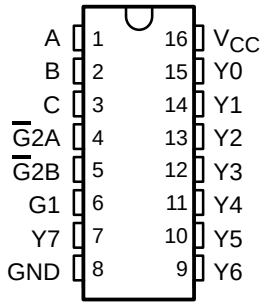
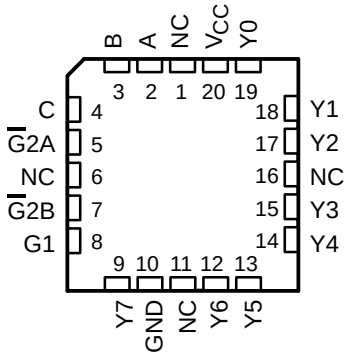
- **Operating Range 2-V to 5.5-V V_{CC}**
- ***EPIC***™ **(Enhanced-Performance Implanted CMOS) Process**
- **Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems**
- **Incorporate Three Enable Inputs to Simplify Cascading and/or Data Reception**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHC138 . . . J OR W PACKAGE
SN74AHC138 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AHC138 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The ’AHC138 decoders/demultiplexers are designed for high-performance memory-decoding or data-routing applications requiring very short propagation-delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

The conditions at the binary-select inputs and the three enable inputs select one of eight output lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

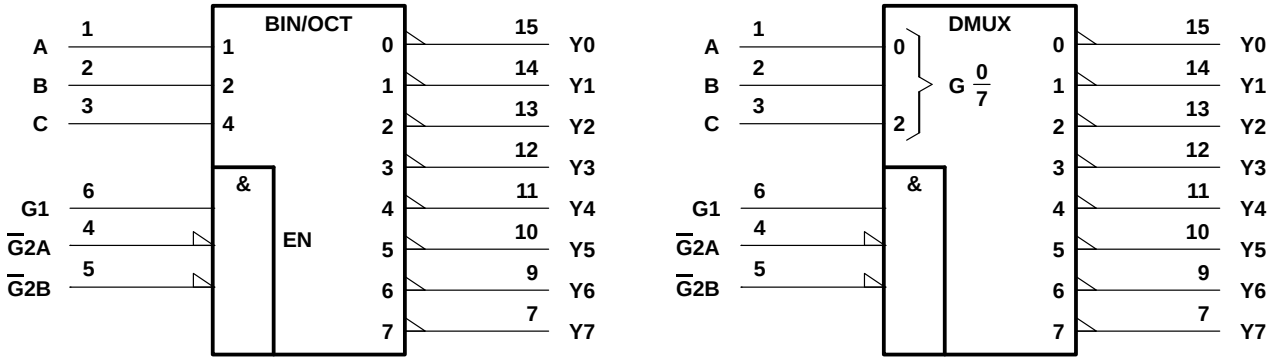
The SN54AHC138 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC138 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

FUNCTION TABLE

ENABLE INPUTS			SELECT INPUTS			OUTPUTS							
G1	$\overline{G}$2A	$\overline{G}$2B	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

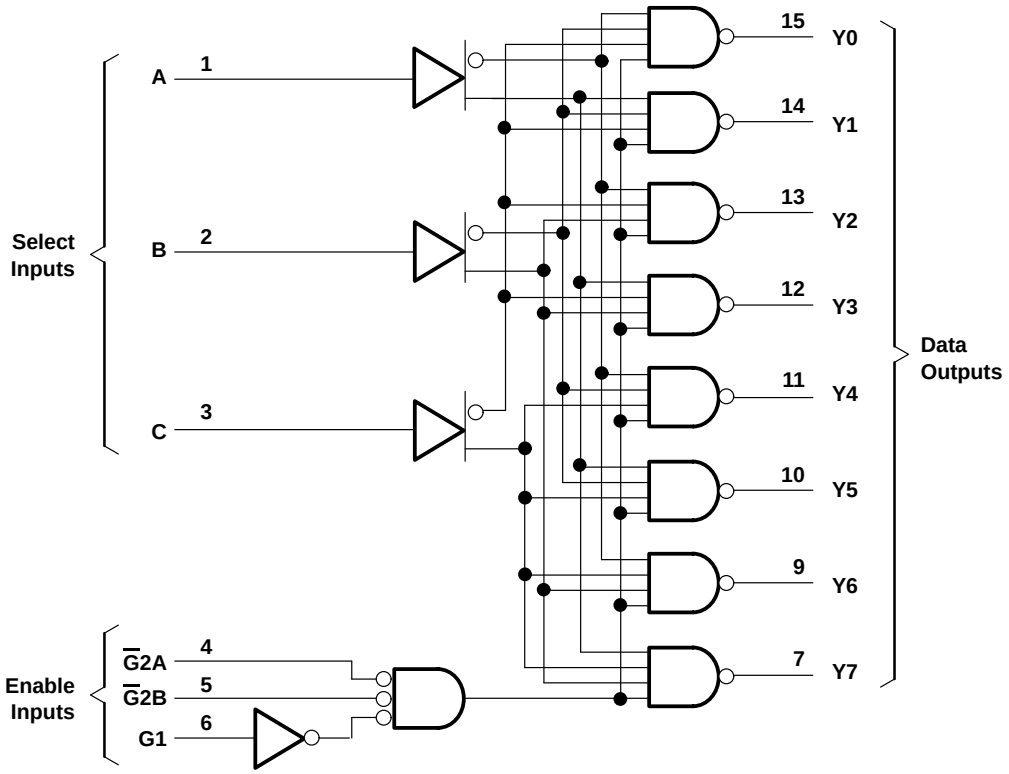
logic symbols (alternatives)†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

PRODUCT PREVIEW

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . –20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . . ±75 mA
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . . 113°C/W
DB package . . . . . 131°C/W
N package . . . . . 78°C/W
PW package . . . . . 149°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

PRODUCT PREVIEW

recommended operating conditions (see Note 3)

			SN54AHC138		SN74AHC138		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50		–50	μA
		V_{CC} = 3.3 V ± 0.3 V		–4		–4	mA
		V_{CC} = 5 V ± 0.5 V		–8		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4		4	mA
		V_{CC} = 5 V ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20		20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHC138		SN74AHC138		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	2 V	1.9	2		1.9		1.9		V
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	I_{OH} = –4 mA	3 V	2.58			2.48		2.48		
	I_{OH} = –8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}	I_{OL} = 50 μA	2 V			0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
	I_{OL} = 4 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40		40	μA
C_i	V_I = V_{CC} or GND	5 V		4	10				10	pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHC138					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A, B, C	Any Y	C_L = 15 pF		8.2	11.4	1	13	ns
t_{PHL}*					8.2	11.4	1	13	
t_{PLH}*	G1	Any Y	C_L = 15 pF		8.1	12.8	1	15	ns
t_{PHL}*					8.1	12.8	1	15	
t_{PLH}*	$\overline{G}$2A, $\overline{G}$2B	Any Y	C_L = 15 pF		8.2	11.4	1	13.5	ns
t_{PHL}*					8.2	11.4	1	13.5	
t_{PLH}	A, B, C	Any Y	C_L = 50 pF		10	15.8	1	18	ns
t_{PHL}					10	15.8	1	18	
t_{PLH}	G1	Any Y	C_L = 50 pF		10.6	16.3	1	18.5	ns
t_{PHL}					10.6	16.3	1	18.5	
t_{PLH}	$\overline{G}$2A, $\overline{G}$2B	Any Y	C_L = 50 pF		10.7	14.9	1	17	ns
t_{PHL}					10.7	14.9	1	17	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHC138					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A, B, C	Any Y	C_L = 15 pF		8.2	11.4	1	13	ns
t_{PHL}					8.2	11.4	1	13	
t_{PLH}	G1	Any Y	C_L = 15 pF		8.1	12.8	1	15	ns
t_{PHL}					8.1	12.8	1	15	
t_{PLH}	$\overline{G}$2A, $\overline{G}$2B	Any Y	C_L = 15 pF		8.2	11.4	1	13.5	ns
t_{PHL}					8.2	11.4	1	13.5	
t_{PLH}	A, B, C	Any Y	C_L = 50 pF		10	15.8	1	18	ns
t_{PHL}					10	15.8	1	18	
t_{PLH}	G1	Any Y	C_L = 50 pF		10.6	16.3	1	18.5	ns
t_{PHL}					10.6	16.3	1	18.5	
t_{PLH}	$\overline{G}$2A, $\overline{G}$2B	Any Y	C_L = 50 pF		10.7	14.9	1	17	ns
t_{PHL}					10.7	14.9	1	17	

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switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHC138					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A, B, C	Any Y	C_L = 15 pF		5.7	8.1	1	9.5	ns
t_{PHL}*					5.7	8.1	1	9.5	
t_{PLH}*	G1	Any Y	C_L = 15 pF		5.6	8.1	1	9.5	ns
t_{PHL}*					5.6	8.1	1	9.5	
t_{PLH}*	$\overline{G}$2A, $\overline{G}$2B	Any Y	C_L = 15 pF		5.8	8.1	1	9.5	ns
t_{PHL}*					5.8	8.1	1	9.5	
t_{PLH}	A, B, C	Any Y	C_L = 50 pF		7.2	10.1	1	11.5	ns
t_{PHL}					7.2	10.1	1	11.5	
t_{PLH}	G1	Any Y	C_L = 50 pF		7.1	10.1	1	11.5	ns
t_{PHL}					7.1	10.1	1	11.5	
t_{PLH}	$\overline{G}$2A, $\overline{G}$2B	Any Y	C_L = 50 pF		7.3	10.1	1	11.5	ns
t_{PHL}					7.3	10.1	1	11.5	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

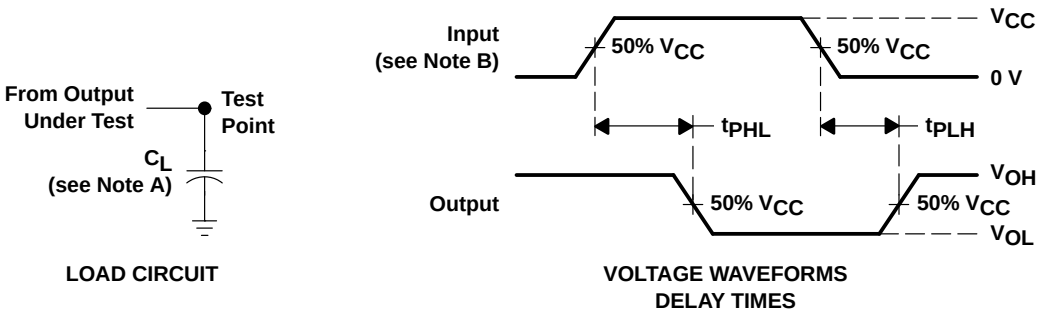
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHC138					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A, B, C	Any Y	C_L = 15 pF		5.7	8.1	1	9.5	ns
t_{PHL}					5.7	8.1	1	9.5	
t_{PLH}	G1	Any Y	C_L = 15 pF		5.6	8.1	1	9.5	ns
t_{PHL}					5.6	8.1	1	9.5	
t_{PLH}	$\overline{G}$2A, $\overline{G}$2B	Any Y	C_L = 15 pF		5.8	8.1	1	9.5	ns
t_{PHL}					5.8	8.1	1	9.5	
t_{PLH}	A, B, C	Any Y	C_L = 50 pF		7.2	10.1	1	11.5	ns
t_{PHL}					7.2	10.1	1	11.5	
t_{PLH}	G1	Any Y	C_L = 50 pF		7.1	10.1	1	11.5	ns
t_{PHL}					7.1	10.1	1	11.5	
t_{PLH}	$\overline{G}$2A, $\overline{G}$2B	Any Y	C_L = 50 pF		7.3	10.1	1	11.5	ns
t_{PHL}					7.3	10.1	1	11.5	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	34	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

APPLICATION INFORMATION

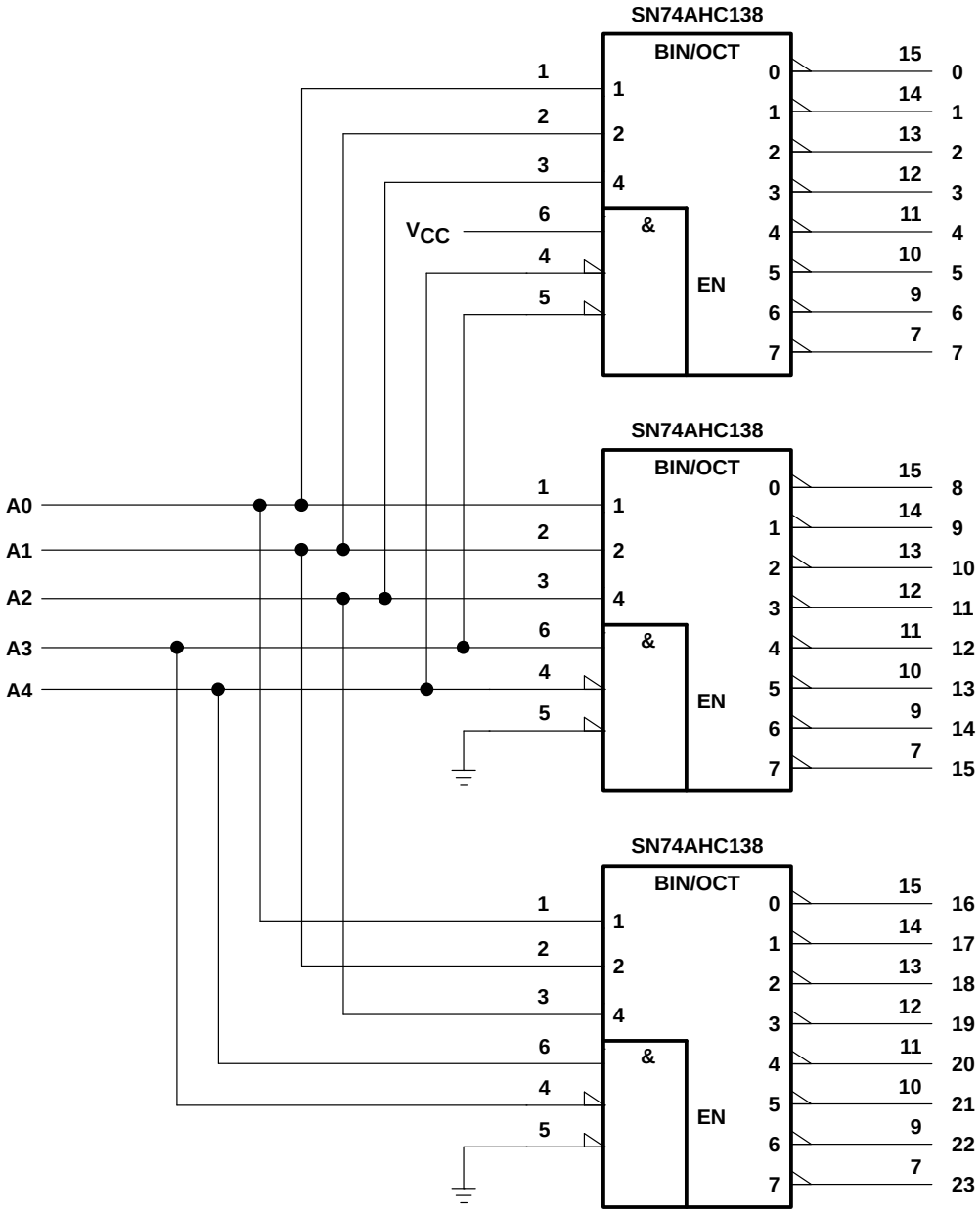


Figure 2. 24-Bit Decoding Scheme

APPLICATION INFORMATION

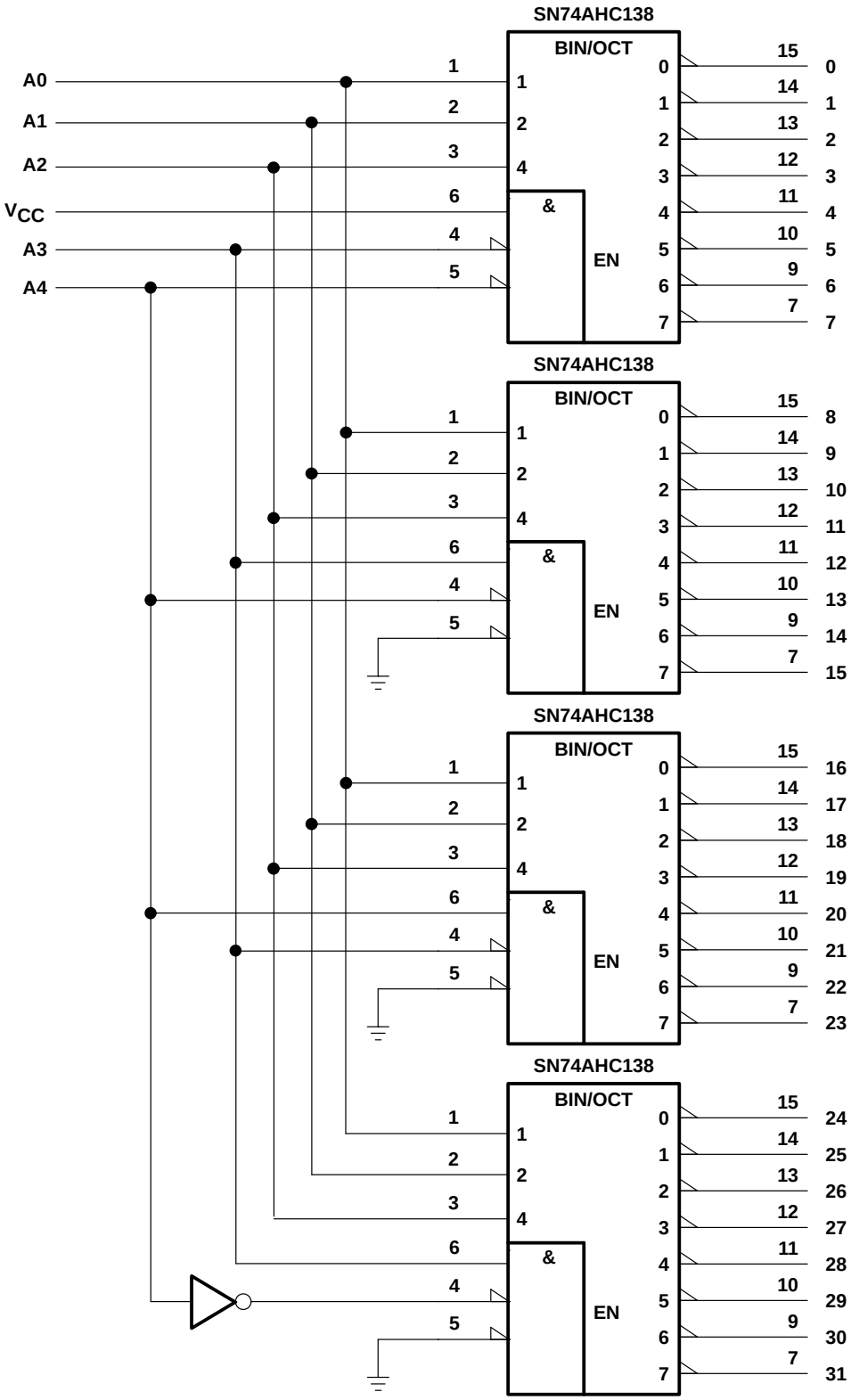


Figure 3. 32-Bit Decoding Scheme

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