

SN54AHCT240, SN74AHCT240 OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCLS252E – OCTOBER 1995 – REVISED JULY 1997

- Inputs Are TTL-Voltage Compatible
- **EPIC™** (Enhanced-Performance Implanted CMOS) Process
- High Latch-Up Immunity Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs

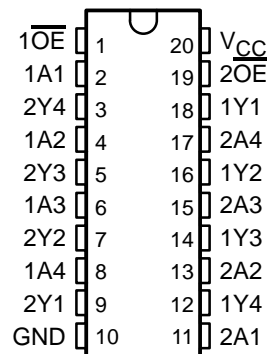
description

These octal buffers/drivers are designed specifically to improve the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

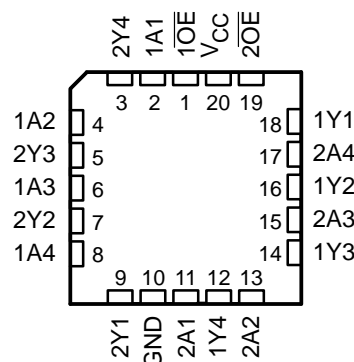
The 'AHCT240 are organized as two 4-bit buffers/line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

The SN54AHCT240 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AHCT240 is characterized for operation from -40°C to 85°C .

SN54AHCT240 . . . J OR W PACKAGE
SN74AHCT240 . . . DB, DGV, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54AHCT240 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each buffer/driver)

INPUTS		OUTPUT Y
\overline{OE}	A	
L	H	L
L	L	H
H	X	Z



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**TEXAS
INSTRUMENTS**

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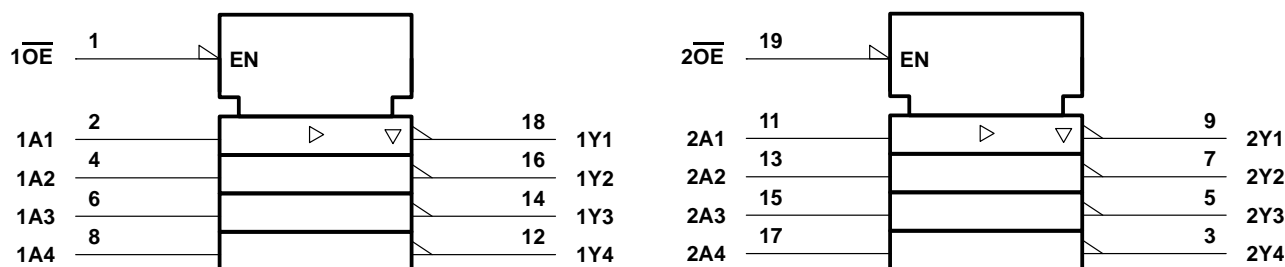
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OCTAL BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

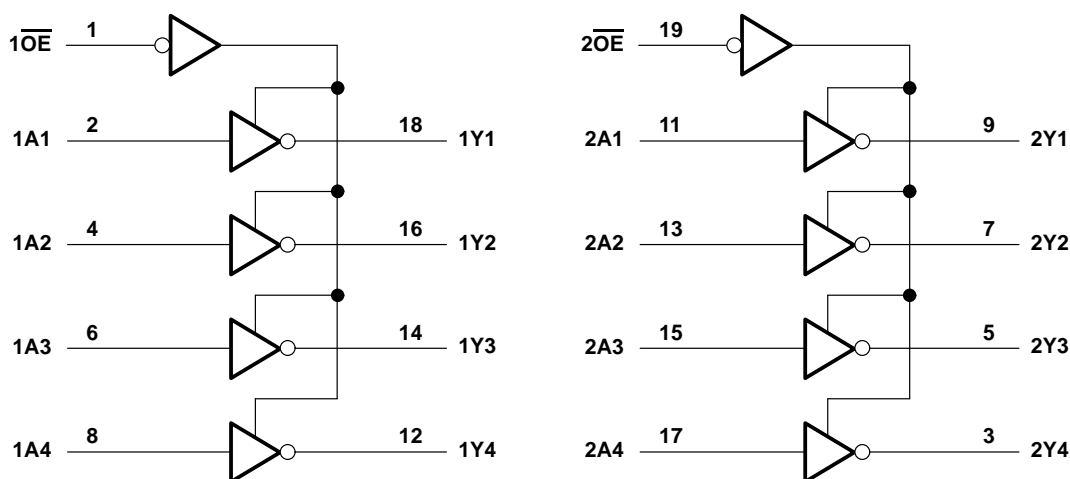
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±75 mA
Package thermal impedance, θ_{JA} (see Note 2):	
DB package	115°C/W
DGV package	146°C/W
DW package	97°C/W
N package	67°C/W
PW package	128°C/W

Storage temperature range, T_{stg} –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

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recommended operating conditions (see Note 3)

		SN54AHCT240		SN74AHCT240		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–8		–8	mA
I_{OL}	Low-level output current		8		8	mA
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			SN54AHCT240		SN74AHCT240		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$I_{OH} = -50\ \mu\text{A}$	4.5 V	4.4	4.5		4.4		4.4		V
	$I_{OH} = -8\ \text{mA}$		3.94			3.8		3.8		
V_{OL}	$I_{OL} = 50\ \mu\text{A}$	4.5 V			0.1		0.1		0.1	V
	$I_{OL} = 8\ \text{mA}$				0.36		0.44		0.44	
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			± 0.25		± 2.5		± 2.5	μA
I_I	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1		± 1	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			4		40		40	μA
ΔI_{CC}^\dagger	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5		1.5	mA
C_i	$V_I = V_{CC}$ or GND	5 V		2.5	10				10	pF
C_o	$V_O = V_{CC}$ or GND	5 V		3						pF

[†] This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC} .

SN54AHCT240, SN74AHCT240

OCTAL BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHCT240				UNIT	
				T _A = 25°C			MIN		MAX
				MIN	TYP	MAX			
t _{PLH} *	A	Y	C _L = 15 pF	5.4	7.4	1	8.5	ns	
t _{PHL} *				5.4	7.4	1	8.5		
t _{PZH} *	\overline{OE}	Y	C _L = 15 pF	7.7	10.4	1	12	ns	
t _{PZL} *				7.7	10.4	1	12		
t _{PHZ} *	\overline{OE}	Y	C _L = 15 pF	8.3	10.4	1	12	ns	
t _{PLZ} *				8.3	10.4	1	12		
t _{PLH}	A	Y	C _L = 50 pF	5.9	8.4	1	9.5	ns	
t _{PHL}				5.9	8.4	1	9.5		
t _{PZH}	\overline{OE}	Y	C _L = 50 pF	8.2	11.4	1	13	ns	
t _{PZL}				8.2	11.4	1	13		
t _{PHZ}	\overline{OE}	Y	C _L = 50 pF	8.8	11.4	1	13	ns	
t _{PLZ}				8.8	11.4	1	13		

* On products compliant to MIL-PRF-38535, this parameter is warranted but not production tested.

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHCT240				UNIT	
				T _A = 25°C			MIN		MAX
				MIN	TYP	MAX			
t _{PLH}	A	Y	C _L = 15 pF	5.4	7.4	1	8.5	ns	
t _{PHL}				5.4	7.4	1	8.5		
t _{PZH}	\overline{OE}	Y	C _L = 15 pF	7.7	10.4	1	12	ns	
t _{PZL}				7.7	10.4	1	12		
t _{PHZ}	\overline{OE}	Y	C _L = 15 pF	8.3	10.4	1	12	ns	
t _{PLZ}				8.3	10.4	1	12		
t _{PLH}	A	Y	C _L = 50 pF	5.9	8.4	1	9.5	ns	
t _{PHL}				5.9	8.4	1	9.5		
t _{PZH}	\overline{OE}	Y	C _L = 50 pF	8.2	11.4	1	13	ns	
t _{PZL}				8.2	11.4	1	13		
t _{PHZ}	\overline{OE}	Y	C _L = 50 pF	8.8	11.4	1	13	ns	
t _{PLZ}				8.8	11.4	1	13		

output-skew characteristics, $C_L = 50\text{ pF}$ (see Note 4)

PARAMETER	V _{CC}	SN74AHCT240				UNIT
		T _A = 25°C		MIN	MAX	
		MIN	MAX			
t _{sk(o)} Output skew	5 V ± 0.5 V	1		1	ns	

NOTE 4: Skew between any two outputs of the same package switching in the same direction. This parameter is warranted but not production tested.



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noise characteristics, $V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

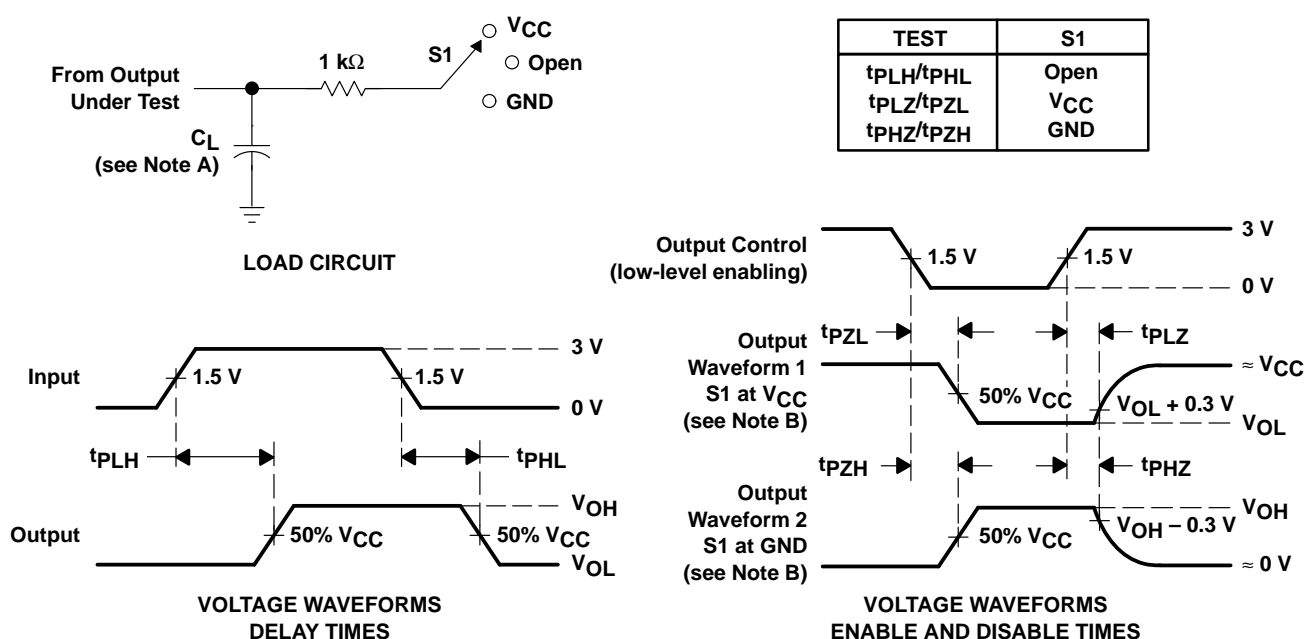
PARAMETER	SN74AHCT240			UNIT
	MIN	TYP	MAX	
$V_{OH(V)}$ Quiet output, minimum dynamic V_{OH}		4.1		V
$V_{IH(D)}$ High-level dynamic input voltage	2			V
$V_{IL(D)}$ Low-level dynamic input voltage		0.8		V

NOTE 5: Characteristics are for surface-mount packages only. These parameters are warranted but not production tested.

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load, $f = 1\text{ MHz}$	10	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r = 3\text{ ns}$, $t_f = 3\text{ ns}$.

D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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