

# SN54LV02, SN74LV02 QUADRUPLE 2-INPUT POSITIVE-NOR GATES

SCLS183B – FEBRUARY 1993 – REVISED APRIL 1996

- **EPIC™ (Enhanced-Performance Implanted CMOS) 2-μ Process**
- **Typical  $V_{OLP}$  (Output Ground Bounce)  $< 0.8$  V at  $V_{CC}$ ,  $T_A = 25^\circ\text{C}$**
- **Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $> 2$  V at  $V_{CC}$ ,  $T_A = 25^\circ\text{C}$**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ( $C = 200$  pF,  $R = 0$ )**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Ceramic (J) 300-mil DIPs**

## description

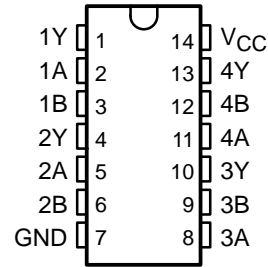
These quadruple 2-input positive-NOR gates are designed for 2.7-V to 5.5-V  $V_{CC}$  operation.

The 'LV02 perform Boolean function  $Y = \overline{A + B}$  or  $Y = \overline{A} \cdot \overline{B}$  in positive logic.

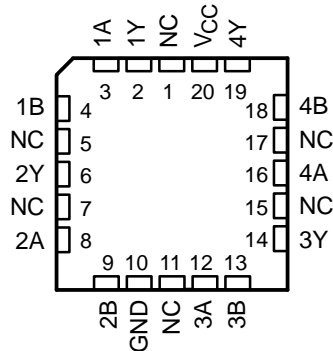
The SN74LV02 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LV02 is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74LV02 is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

SN54LV02 . . . J OR W PACKAGE  
SN74LV02 . . . D, DB, OR PW PACKAGE  
(TOP VIEW)



SN54LV02 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE  
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC is a trademark of Texas Instruments Incorporated.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

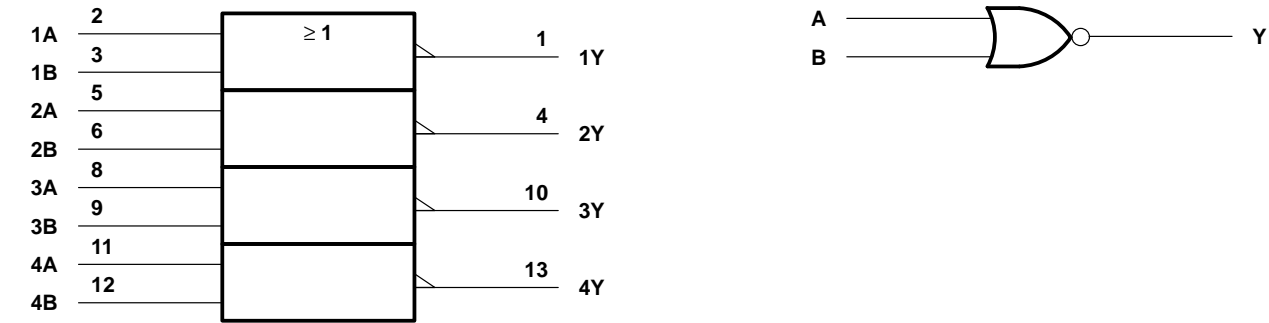
Copyright © 1996, Texas Instruments Incorporated

SN54LV02, SN74LV02  
QUADRUPLE 2-INPUT POSITIVE-NOR GATES

SCLS183B – FEBRUARY 1993 – REVISED APRIL 1996

logic symbol†

logic diagram, each gate (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for the D, DB, J, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	$\pm 50$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	$\pm 25$ mA
Continuous current through $V_{CC}$ or GND	$\pm 50$ mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): D package	1.25 W
DB or PW package	0.5 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
  2. This value is limited to 7 V maximum.
  3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

# SN54LV02, SN74LV02 QUADRUPLE 2-INPUT POSITIVE-NOR GATES

SCLS183B – FEBRUARY 1993 – REVISED APRIL 1996

## recommended operating conditions (see Note 4)

			SN54LV02		SN74LV02		UNIT
			MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage		2.7	5.5	2.7	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2		2		V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	3.15		3.15		
$V_{IL}$	Low-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		0.8		0.8	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		1.65		1.65	
$V_I$	Input voltage		0	$V_{CC}$	0	$V_{CC}$	V
$V_O$	Output voltage		0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		-6		-6	mA
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		-12		-12	
$I_{OL}$	Low-level output current	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		6		6	mA
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	100	0	100	ns/V
$T_A$	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub> <sup>†</sup>	SN54LV02			SN74LV02			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = −100 μA	MIN to MAX	V <sub>CC</sub> − 0.2			V <sub>CC</sub> − 0.2			V
	I <sub>OH</sub> = −6 mA	3 V	2.4			2.4			
	I <sub>OH</sub> = −12 mA	4.5 V	3.6			3.6			
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	MIN to MAX	0.2			0.2			V
	I <sub>OL</sub> = 6 mA	3 V	0.4			0.4			
	I <sub>OL</sub> = 12 mA	4.5 V	0.55			0.55			
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V	±1			±1			μA
		5.5 V	±1			±1			
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V	20			20			μA
		5.5 V	20			20			
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> − 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 3.6 V	500			500			μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	2.5			2.5			pF
		5 V	2.5			2.5			

$^\dagger$  For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

## switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LV02								UNIT
			$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$		
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A	Y		5	10		8	13	16	ns	

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

# SN54LV02, SN74LV02

## QUADRUPLE 2-INPUT POSITIVE-NOR GATES

SCLS183B – FEBRUARY 1993 – REVISED APRIL 1996

switching characteristics over recommended operating free-air temperature range,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LV02								UNIT
			V <sub>CC</sub> = 5 V ± 0.5 V			V <sub>CC</sub> = 3.3 V ± 0.3 V			V <sub>CC</sub> = 2.7 V		
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	510			813			16		ns

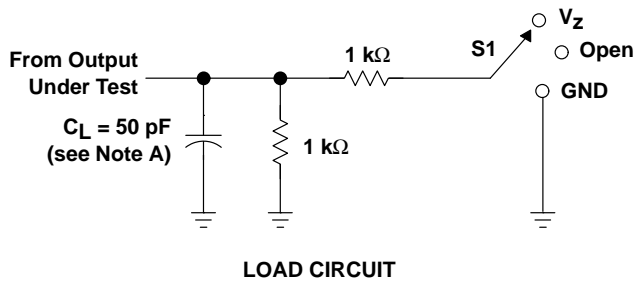
operating characteristics,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC}$	TYP	UNIT
$C_{pd}$	Power dissipation capacitance per gate	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	3.3 V	16	pF
			5 V	20	



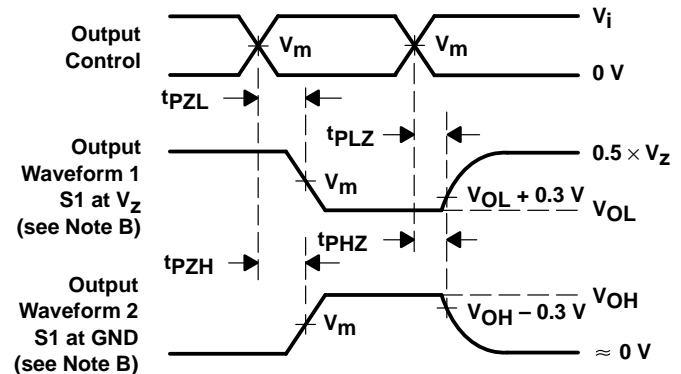
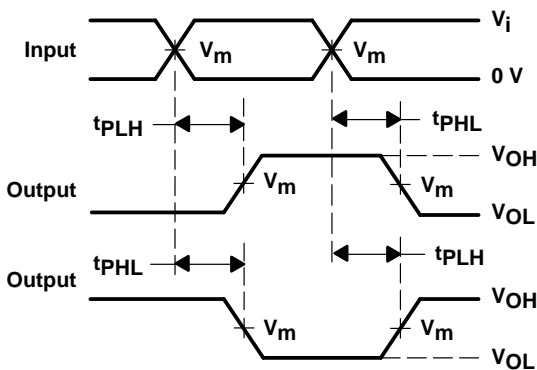
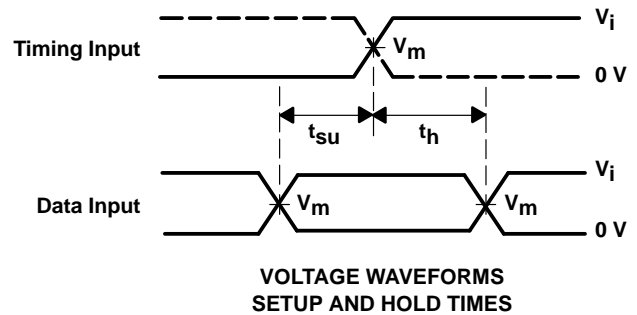
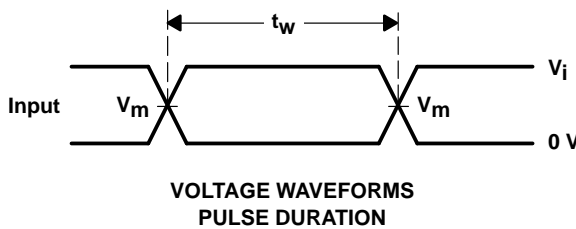
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

## PARAMETER MEASUREMENT INFORMATION



TEST	S1
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	V <sub>Z</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

WAVEFORM CONDITION	V <sub>CC</sub> = 4.5 V to 5.5 V	V <sub>CC</sub> = 2.7 V to 3.6 V
V <sub>m</sub>	0.5 × V <sub>CC</sub>	1.5 V
V <sub>i</sub>	V <sub>CC</sub>	2.7 V
V <sub>Z</sub>	2 × V <sub>CC</sub>	6 V



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
  - The outputs are measured one at a time with one transition per measurement.
  - t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
  - t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
  - t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd</sub>.

Figure 1. Load Circuit and Voltage Waveforms

## **IMPORTANT NOTICE**

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

**TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.**

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.