### SN54HC4024, SN74HC4024 ASYNCHRONOUS 7-BIT BINARY COUNTERS

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

#### description

The 'HC4024 is an asynchronous 7-stage binary counter designed with an input pulse-shaping circuit. The outputs of all stages are available externally. A high clear signal asynchronously clears the counter and resets all outputs low. The count is advanced on the high-to-low transition of the clock pulse. Applications include timedelay circuits, counter controls, and frequencydividing circuits.

The SN54HC4024 is characterized for operation over the full military temperature range of -55 °C to 125 °C. The SN74HC4024 is characterized for operation from -40 °C to 85 °C.

logic symbol<sup>†</sup>



 $^\dagger \text{This symbol}$  is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

D2804, MARCH 1984-REVISED JUNE 1989

		N PACKAGE
(		

	13 🗌 N C
QG []3	12 0A
QF []4	11 🗋 QB
	10 🗍 NC
QD [[6	9∏0C
GND 7	8 🗋 NC

SN54HC4024 . . . FK PACKAGE (TOP VIEW)

Q <sub>G</sub> NC QF NC QE	]4 ]5 ]6 ]7 ]8	18 0 QA 17 0 NC 16 0 QB 15 0 NC 14 0 NC	
		a a a a a a a a a a a a a a a a a a a	

NC-No internal connection

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## SN54HC4024, SN74HC4024 Asynchronous 7-bit binary counters

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

#### typical clear and count sequence





#### absolute maximum ratings over operating free-air temperature range<sup>†</sup>

Supply voltage, VCC
Input clamp current, $ I_{K}(V  < 0 \text{ or } V_{I} > V_{CC})$ $\pm 20 \text{ mA}$
Output clamp current, IOK ( $V_0 < 0$ or $V_0 > V_{CC}$
Continuous output current, $I_0$ (V <sub>0</sub> = 0 to V <sub>CC</sub> ) ± 25 mA
Continuous current through VCC or GND pins $\dots \dots \pm 50$ mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package 260 °C
Storage temperature range

<sup>†</sup> Stresses beyond those listed under ''absolute maximum ratings'' may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under ''recommended operating conditions'' is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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			SN54HC4024			SN74HC4024			
			MIN	MIN NOM MAX MIN NOM				MAX	UNIT
Vcc	Supply voltage		2	5	56	2	5	6	V
VIH High-level input voltage		$V_{CC} = 2 V$	1.5			1.5			
	$V_{CC} = 4.5 V$	3.15			3.15			v	
		$V_{CC} = 6 V$	4.2			4.2			
		$V_{CC} = 2 V$	0		0.3	0		0.3	
VIL	VIL Low-level input voltage	$V_{CC} = 4.5 V$	0		0.9	0		0.9	V V
		$V_{CC} = 6 V$	0		1.2	0		1.2	
VI.	Input voltage		0		Vcc	0		Vcc	V
٧o	Output voltage		0		Vcc	0		Vcc	V
		$V_{CC} = 2 V$	0		1000	0		1000	1
t <sub>t</sub> Input transition (rise and fa	Input transition (rise and fall) times	$V_{CC} = 4.5 V$	0		500	0		500	ns
		$V_{CC} = 6 V$	0		400	0		400	
ТA	Operating free-air temperature		- 55		125	-40		85	°C

#### recommended operating conditions

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	Vcc	TA = 25°C			SN54HC4024		SN74HC4024		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
∨он		2 V	1.9	1.998		1.9		1.9		
	$V_{I} = V_{IH}$ or $V_{IL}$ , $I_{OH} = -20 \ \mu A$	4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		v
	$V_{I} = V_{IH}$ or $V_{IL}$ , $I_{OH} = -4 \text{ mA}$	4.5 V	3.98	4.30		3.7		3.84		
	$V_{I} = V_{IH}$ or $V_{IL}$ , $I_{OH} = -5.2 \text{ mA}$	6 V	5.48	5.80		5.2		5.34		
		2 V		0.002	0.1	1	0.1		0.1	
	$V_{I} = V_{IH}$ or $V_{IL}$ , $I_{OL} = 20 \ \mu A$	4.5 V		0.001	0.1		0.1		0.1	
VOL		6 V		0.001	0.1		0.1	Į	0.1	v
	$V_{I} = V_{IH} \text{ or } V_{IL}, I_{OL} = 4 \text{ mA}$	4.5 V		0.17	0.26		0.4	İ	0.33	
	$V_{ } = V_{  }$ or $V_{  }$ , $I_{OL} = 5.2 \text{ mA}$	6 V		0.15	0.26		0.4		0.33	
4	$V_{ } = V_{CC} \text{ or } 0$	6 V		±0.1	±100		±1000	1	± 1000	nA
lcc	$V_{I} = V_{CC} \text{ or } 0,  I_{O} = 0$	6 V			8		160		80	μA
Ci		2 to 6 V		3	10		10		10	pF



## SN54HC4024, SN74HC4024 Asynchronous 7-bit binary counters

				T <sub>A</sub> =	25 °C	SN54HC4024		SN74HC4024		
			Vcc	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
			2V	0	5.5	0	3.7	0	4.3	
f <sub>clack</sub> Clock frequency		4.5 V	0	28	0	19	0	22	MHz	
			6 V	0	33	0	22	0	25	
			2 V	90		135		115		
. '		CLK high or low	4.5 V	18		27		23		пs
	Pulse		6 V	15		23		20		
tw	duration		2 V	80		120		100		
		CLR high	4.5 V	16		24		20		пs
			6 V	14		20		17		
Setup time, CLR	Satur time CLD law		2 V	80		120		100		
	•		4.5 V	16		24		20		ns
	before CLK+		6 V	14		20		17		

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

# switching characteristics over recommended operating free-air temperature range (unless otherwise noted), $C_L = 50 \text{ pF}$ (see Note 1)

PARAMETER	FROM	то		Τį	<b>∖</b> = 25	°C	SN54HC4024		SN74HC4024		
CONCIEN	(INPUT)	(OUTPUT)	Vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
			2 V	5.5	10		3.7		4.3		
fmax		QA	4.5 V	28	50		19		22		MHz
			6 V	33	60		22		26		
<sup>t</sup> pd CL			2 V	-	56	120		180		150	
	CLK		4.5 V		16	24		36		30	ns
			6 V		12	20		31		26	
			2 V		61	130		195	[	165	
<sup>t</sup> PHL	CLR	Any	4.5 V		17	26		39		32	ns
			6 V		13	22		33	ł	28	
			2 V		28	75	1	110		95	
tt		Q <sub>A</sub>	4.5 V		8	15		22		19	ns
			6 V		6	13		19		16	
Cpd	Power dissipation capacitance				No load	$d, T_A =$	25°C		4	0 pF typ	

Note 1: Load circuits and voltage waveforms are shown in Section 1.

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