

SN54HC574, SN74HC574 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCLS148B – DECEMBER 1982 – REVISED MAY 1997

- **High-Current 3-State Noninverting Outputs**
Drive Bus Lines Directly or up to 15 LSTTL Loads
- **Bus-Structured Pinout**
- **Package Options Include Plastic Small-Outline (DW) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

These octal edge-triggered D-type flip-flops feature 3-state outputs designed specifically for bus driving. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

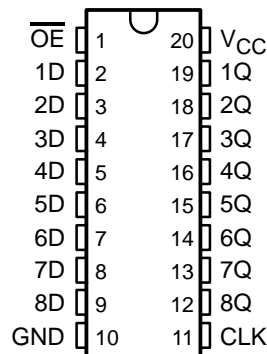
The eight flip-flops enter data on the low-to-high transition of the clock (CLK) input.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

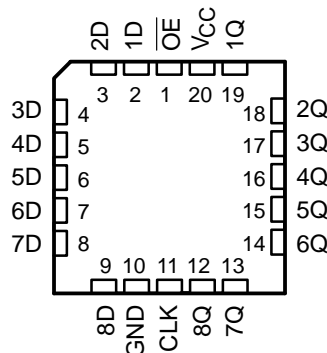
\overline{OE} does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54HC574 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74HC574 is characterized for operation from -40°C to 85°C .

SN54HC574 . . . J OR W PACKAGE
SN74HC574 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC574 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT Q
\overline{OE}	CLK	D	
L	\uparrow	H	H
L	\uparrow	L	L
L	H or L	X	Q_0
H	X	X	Z



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

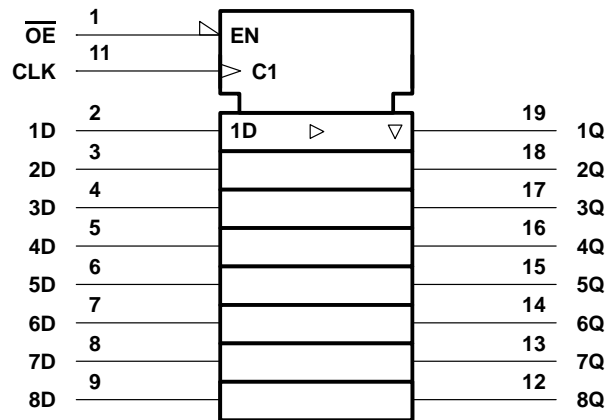
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1997, Texas Instruments Incorporated

SN54HC574, SN74HC574
OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH 3-STATE OUTPUTS

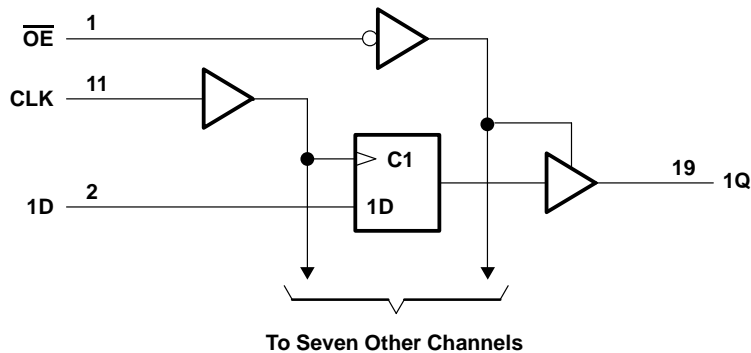
SCLS148B – DECEMBER 1982 – REVISED MAY 1997

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 35 mA
Continuous current through V_{CC} or GND	± 70 mA
Package thermal impedance, θ_{JA} (see Note 2): DW package	97°C/W
N package	67°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

SN54HC574, SN74HC574

OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS

WITH 3-STATE OUTPUTS

SCLS148B – DECEMBER 1982 – REVISED MAY 1997

recommended operating conditions

			SN54HC574			SN74HC574			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		2	5	6	2	5	6	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5			1.5			V
		V _{CC} = 4.5 V	3.15			3.15			
		V _{CC} = 6 V	4.2			4.2			
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0			0			V
		V _{CC} = 4.5 V	0			1.35			
		V _{CC} = 6 V	0			1.8			
V _I	Input voltage		0			V _{CC}			V
V _O	Output voltage		0			V _{CC}			V
t _t	Input transition (rise and fall) time	V _{CC} = 2 V	0			0			ns
		V _{CC} = 4.5 V	0			500			
		V _{CC} = 6 V	0			400			
T _A	Operating free-air temperature		−55			125			°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	T _A = 25°C			SN54HC574		SN74HC574		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = –20 µA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I _{OH} = –6 mA	4.5 V	3.98	4.3		3.7		3.84		
		I _{OH} = –7.8 mA	6 V	5.48	5.8		5.2		5.34		
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 µA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I _{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
		I _{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I _I	V _I = V _{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I _{OZ}	V _O = V _{CC} or 0		6 V		±0.01	±0.5		±10		±5	µA
I _{CC}	V _I = V _{CC} or 0, I _O = 0		6 V			8		160		80	µA
C _i			2 V to 6 V		3	10		10		10	pF

SN54HC574, SN74HC574

OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS

WITH 3-STATE OUTPUTS

SCLS148B – DECEMBER 1982 – REVISED MAY 1997

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

	V _{CC}	T _A = 25°C		SN54HC574		SN74HC574		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock} Clock frequency	2 V	0	6	0	4	0	5	MHz
	4.5 V	0	30	0	20	0	24	
	6 V	0	38	0	24	0	28	
t _w Pulse duration, CLK high or low	2 V	80		120		100		ns
	4.5 V	16		24		20		
	6 V	14		20		17		
t _{su} Setup time, data before CLK↑	2 V	100		150		125		ns
	4.5 V	20		30		25		
	6 V	17		26		21		
t _h Hold time, data after CLK↑	2 V	5		5		5		ns
	4.5 V	5		5		5		
	6 V	5		5		5		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HC574		SN74HC574		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			2 V	6	11		4		5		MHz
			4.5 V	30	36		20		24		
			6 V	36	40		24		28		
t _{pd}	CLK	Any Q	2 V		90	180		270		225	ns
			4.5 V		28	36		54		45	
			6 V		24	31		46		38	
t _{en}	\overline{OE}	Any Q	2 V		77	150		225		190	ns
			4.5 V		26	30		45		38	
			6 V		23	26		38		32	
t _{dis}	\overline{OE}	Any Q	2 V		52	150		225		190	ns
			4.5 V		24	30		45		38	
			6 V		22	26		38		32	
t _t		Any Q	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54HC574, SN74HC574
OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH 3-STATE OUTPUTS

SCLS148B – DECEMBER 1982 – REVISED MAY 1997

switching characteristics over recommended operating free-air temperature range, $C_L = 150 \text{ pF}$
(unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HC574		SN74HC574		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			2 V	6					5		MHz
			4.5 V	30					24		
			6 V	36					28		
t _{pd}	CLK	Any Q	2 V	105 265			400		330		ns
			4.5 V	36 53			80		66		
			6 V	31 46			68		57		
t _{en}	\overline{OE}	Any Q	2 V	95 235			355		295		ns
			4.5 V	32 47			71		59		
			6 V	28 41			60		51		
t _t		Any Q	2 V	60 210			315		265		ns
			4.5 V	17 42			63		53		
			6 V	14 36			53		45		

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	No load	100	pF



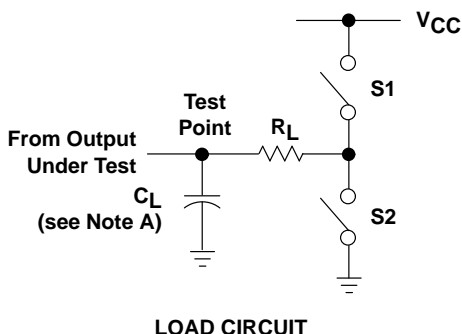
SN54HC574, SN74HC574

OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS

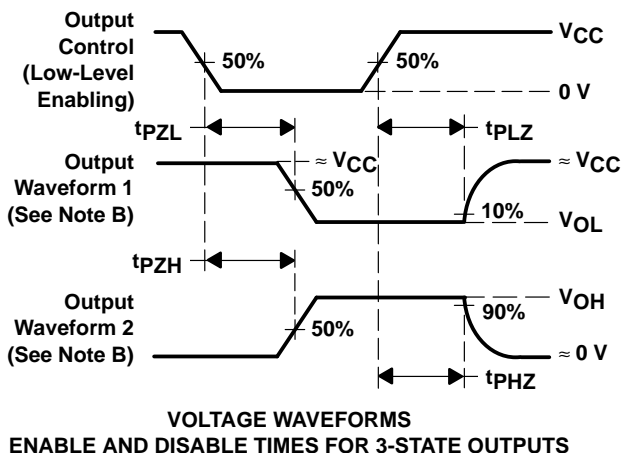
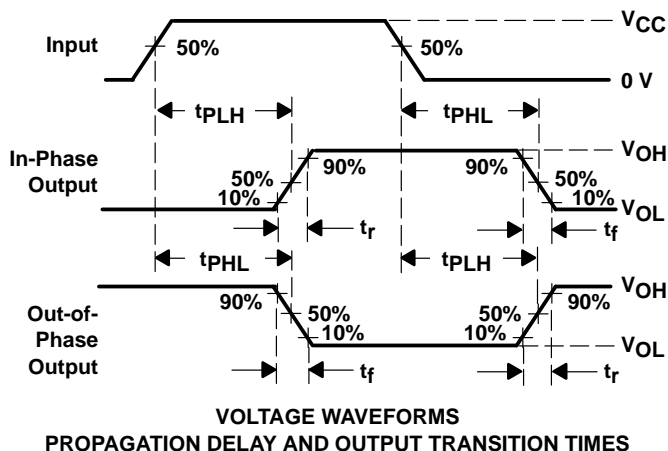
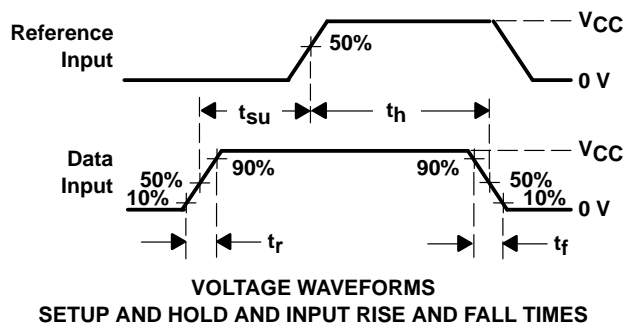
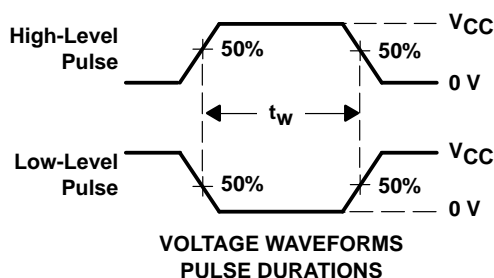
WITH 3-STATE OUTPUTS

SCLS148B – DECEMBER 1982 – REVISED MAY 1997

PARAMETER MEASUREMENT INFORMATION



PARAMETER	R_L	C_L	S1	S2
t_{en}	1 k Ω	50 pF or 150 pF	Open	Closed
			Closed	Open
t_{dis}	1 k Ω	50 pF	Open	Closed
			Closed	Open
t_{pd} or t_t	—	50 pF or 150 pF	Open	Open



- NOTES:
- C_L includes probe and test-fixture capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 - For clock inputs, f_{max} is measured when the input duty cycle is 50%.
 - The outputs are measured one at a time with one input transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.