

SN54HC112, SN74HC112 DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

SCLS099B – DECEMBER 1982 – REVISED MAY 1997

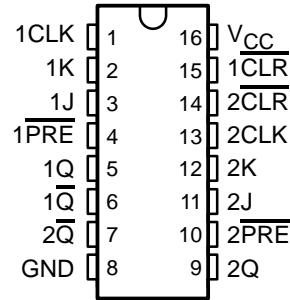
- Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

description

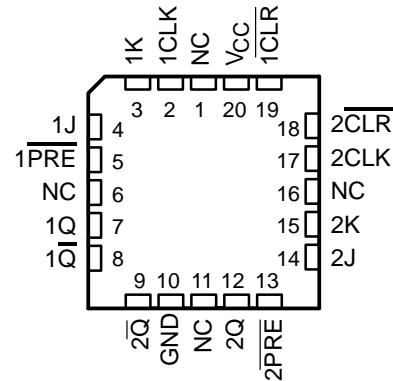
The 'HC112 contain two independent J-K negative-edge-triggered flip-flops. A low level at the preset (PRE) or clear (CLR) inputs sets or resets the outputs regardless of the levels of the other inputs. When PRE and CLR are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of CLK. Following the hold-time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops perform as toggle flip-flops by tying J and K high.

The SN54HC112 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74HC112 is characterized for operation from -40°C to 85°C .

SN54HC112 . . . J OR W PACKAGE
SN74HC112 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC112 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

| INPUTS | | | | | OUTPUTS | |
|--------|-----|-----|---|---|----------------|-----------------|
| PRE | CLR | CLK | J | K | Q | Q̄ |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H† | H† |
| H | H | ↓ | L | L | Q ₀ | Q̄ ₀ |
| H | H | ↓ | H | L | H | L |
| H | H | ↓ | L | H | L | H |
| H | H | ↓ | H | H | Toggle | |
| H | H | H | X | X | Q ₀ | Q̄ ₀ |

† This configuration is unstable; that is, it does not persist when either PRE or CLR returns to its inactive (high) level.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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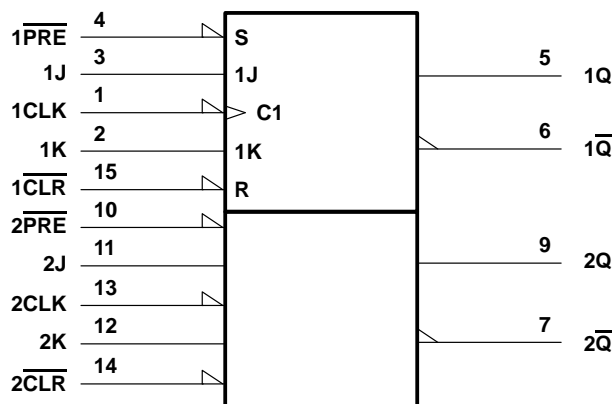
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DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS

WITH CLEAR AND PRESET

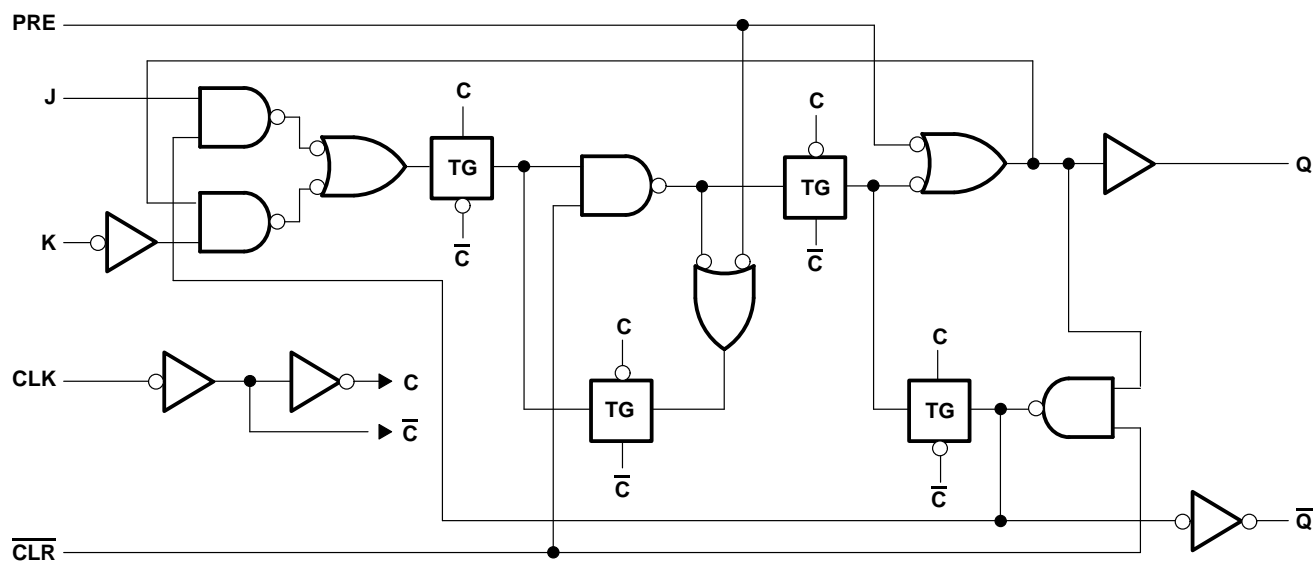
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram, each flip-flop (positive logic)



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absolute maximum ratings over operating free-air temperature†

| | |
|---|----------------|
| Supply voltage range, V_{CC} | –0.5 V to 7 V |
| Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) | ±20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) | ±20 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ±25 mA |
| Continuous current through V_{CC} or GND | ±50 mA |
| Package thermal impedance, θ_{JA} (see Note 2): D package | 113°C/W |
| N package | 78°C/W |
| Storage temperature range, T_{stg} | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JEDEC 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

| | | | SN54HC112 | | | SN74HC112 | | | UNIT |
|----------------|---------------------------------------|------------------|-----------|----------|-----|-----------|----------|-----|------|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | | 2 | 5 | 6 | 2 | 5 | 6 | V |
| V_{IH} | High-level input voltage | $V_{CC} = 2$ V | 1.5 | | | 1.5 | | | V |
| | | $V_{CC} = 4.5$ V | 3.15 | | | 3.15 | | | |
| | | $V_{CC} = 6$ V | 4.2 | | | 4.2 | | | |
| V_{IL} | Low-level input voltage | $V_{CC} = 2$ V | 0 | 0.5 | | 0 | 0.5 | | V |
| | | $V_{CC} = 4.5$ V | 0 | 1.35 | | 0 | 1.35 | | |
| | | $V_{CC} = 6$ V | 0 | 1.8 | | 0 | 1.8 | | |
| V_I | Input voltage | | 0 | V_{CC} | | 0 | V_{CC} | | V |
| V_O | Output voltage | | 0 | V_{CC} | | 0 | V_{CC} | | V |
| t_t^\ddagger | Input transition (rise and fall) time | $V_{CC} = 2$ V | 0 | 1000 | | 0 | 1000 | | ns |
| | | $V_{CC} = 4.5$ V | 0 | 500 | | 0 | 500 | | |
| | | $V_{CC} = 6$ V | 0 | 400 | | 0 | 400 | | |
| T_A | Operating free-air temperature | | –55 | 125 | | –40 | 85 | | °C |

‡ If this device is used in the threshold region (from $V_{ILmax} = 0.5$ V to $V_{IHmin} = 1.5$ V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at $t_t = 1000$ ns and $V_{CC} = 2$ V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | V _{CC} | T _A = 25°C | | | SN54HC112 | | SN74HC112 | | UNIT |
|-----------------|---|---------------------------|-----------------|-----------------------|-------|------|-----------|-------|-----------|-------|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| V _{OH} | V _I = V _{IH} or V _{IL} | I _{OH} = -20 µA | 2 V | 1.9 | 1.998 | | 1.9 | | 1.9 | | V |
| | | | 4.5 V | 4.4 | 4.499 | | 4.4 | | 4.4 | | |
| | | | 6 V | 5.9 | 5.999 | | 5.9 | | 5.9 | | |
| | | I _{OH} = -4 mA | 4.5 V | 3.98 | 4.3 | | 3.7 | | 3.84 | | |
| | | I _{OH} = -5.2 mA | 6 V | 5.48 | 5.8 | | 5.2 | | 5.34 | | |
| V _{OL} | V _I = V _{IH} or V _{IL} | I _{OL} = 20 µA | 2 V | | 0.002 | 0.1 | | 0.1 | | 0.1 | V |
| | | | 4.5 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | | | 6 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | | I _{OL} = 4 mA | 4.5 V | | 0.17 | 0.26 | | 0.4 | | 0.33 | |
| | | I _{OL} = 5.2 mA | 6 V | | 0.15 | 0.26 | | 0.4 | | 0.33 | |
| I _I | V _I = V _{CC} or 0 | | 6 V | | ±0.1 | ±100 | | ±1000 | | ±1000 | nA |
| I _{CC} | V _I = V _{CC} or 0, I _O = 0 | | 6 V | | | 4 | | 80 | | 40 | µA |
| C _i | | | 2 V to 6 V | | 3 | 10 | | 10 | | 10 | pF |

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

| | | V _{CC} | T _A = 25°C | | SN54HC112 | | SN74HC112 | | UNIT |
|--------------------|----------------------------|-----------------|-----------------------|-----|-----------|-----|-----------|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| f _{clock} | Clock frequency | 2 V | 0 | 5 | 0 | 3.4 | 0 | 4 | MHz |
| | | 4.5 V | 0 | 25 | 0 | 17 | 0 | 20 | |
| | | 6 V | 0 | 29 | 0 | 20 | 0 | 24 | |
| t _w | Pulse duration | PRE or CLR low | 2 V | 100 | | 150 | | 125 | ns |
| | | | 4.5 V | 20 | | 30 | | 25 | |
| | | | 6 V | 17 | | 25 | | 21 | |
| | CLK high or low | | 2 V | 100 | | 150 | | 125 | |
| | | | 4.5 V | 20 | | 30 | | 25 | |
| | | | 6 V | 17 | | 25 | | 21 | |
| t _{su} | Setup time before CLK↓ | Data (J, K) | 2 V | 100 | | 150 | | 125 | ns |
| | | | 4.5 V | 20 | | 30 | | 25 | |
| | | | 6 V | 17 | | 25 | | 21 | |
| | PRE or CLR inactive | | 2 V | 100 | | 150 | | 125 | |
| | | | 4.5 V | 20 | | 30 | | 25 | |
| | | | 6 V | 17 | | 25 | | 21 | |
| t _h | Hold time, data after CLK↓ | | 2 V | 0 | | 0 | | 0 | ns |
| | | | 4.5 V | 0 | | 0 | | 0 | |
| | | | 6 V | 0 | | 0 | | 0 | |



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switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V_{CC} | $T_A = 25^\circ\text{C}$ | | | SN54HC112 | | SN74HC112 | | UNIT |
|------------|--|---------------------|----------|--------------------------|-----|-----|-----------|-----|-----------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| f_{\max} | | | 2 V | 5 | 10 | | 3.4 | | 4 | | MHz |
| | | | 4.5 V | 25 | 50 | | 17 | | 20 | | |
| | | | 6 V | 29 | 60 | | 20 | | 24 | | |
| t_{pd} | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ | Q or \overline{Q} | 2 V | | 54 | 165 | | 245 | | 205 | ns |
| | | | 4.5 V | | 16 | 33 | | 49 | | 41 | |
| | | | 6 V | | 13 | 28 | | 42 | | 35 | |
| | CLK | Q or \overline{Q} | 2 V | | 56 | 125 | | 185 | | 155 | |
| | | | 4.5 V | | 16 | 25 | | 37 | | 31 | |
| | | | 6 V | | 13 | 21 | | 31 | | 26 | |
| t_t | | Q or \overline{Q} | 2 V | | 29 | 75 | | 110 | | 95 | ns |
| | | | 4.5 V | | 9 | 15 | | 22 | | 19 | |
| | | | 6 V | | 8 | 13 | | 19 | | 16 | |

operating characteristics, $T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|--|-----------------|-----|------|
| C_{pd} Power dissipation capacitance per flip-flop | No load | 35 | pF |

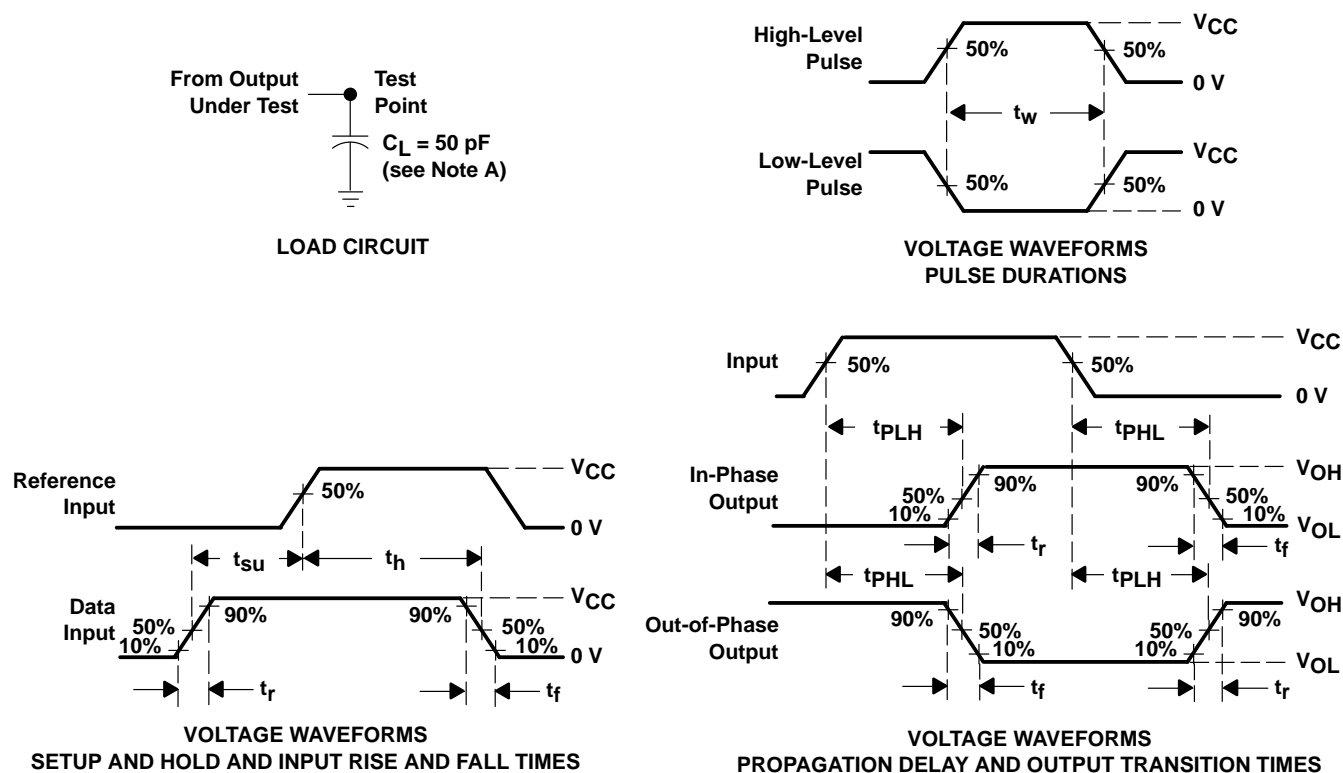
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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- C_L includes probe and test-fixture capacitance.
 - Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 6 \text{ ns}$, $t_f = 6 \text{ ns}$.
 - For clock inputs, f_{max} is measured when the input duty cycle is 50%.
 - The outputs are measured one at a time with one input transition per measurement.
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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