SN54HC7074, SN74HC7074
6-SECTION MULTIFUNCTION (NAND, INVERT, NOR, FLIP-FLOP) CIRCUITS

D2831, MARCH 1984—REVISED SEPTEMBER 1987

- **Contains D-type Flip-Flops with Preset and Clear, NAND, NOR, and Inverter Gates**
- **Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

The SN54HC7074 and SN74HC7074 are each comprised of the following sections:

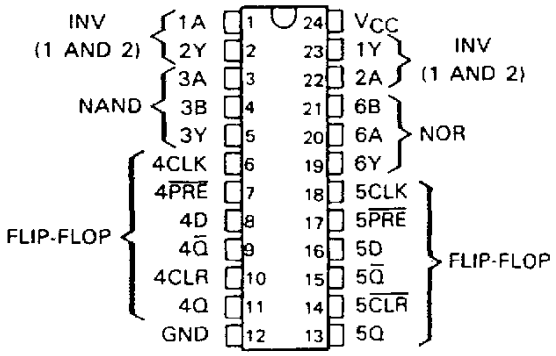
Two inverters
One 2-input NOR gate
One 2-input NAND gate
Two D-type flip-flops

They perform the Boolean functions shown under the respective function table.

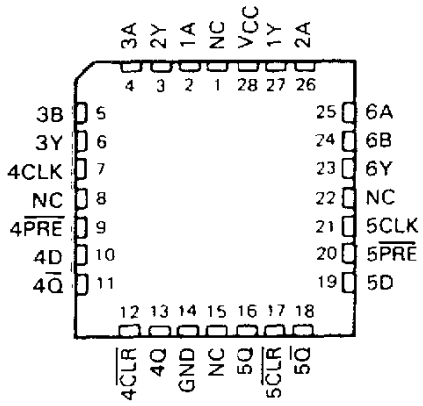
The D-type flip-flops are positive-edge-triggered and are functionally similar to the SN54HC74 and SN74HC74. A low level at the $\overline{PRE}$ or $\overline{CLR}$ inputs sets or resets the outputs regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

The SN54HC7074 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC7074 is characterized for operation from −40°C to 85°C.

SN54HC7074 . . . JT PACKAGE
SN74HC7074 . . . DW OR NT PACKAGE
(TOP VIEW)

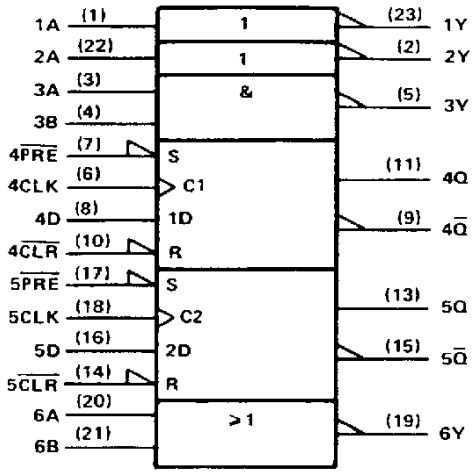


SN54HC7074 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

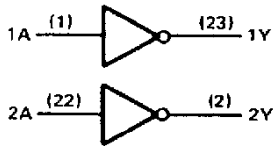
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

INVERTERS

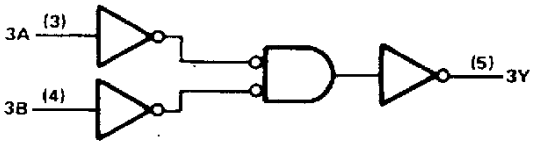


FUNCTION TABLE
(EACH INVERTER)

INPUT	OUTPUT
A	Y
H	L
L	H

positive logic: $Y = \overline{A}$

2-INPUT NAND GATE



FUNCTION TABLE

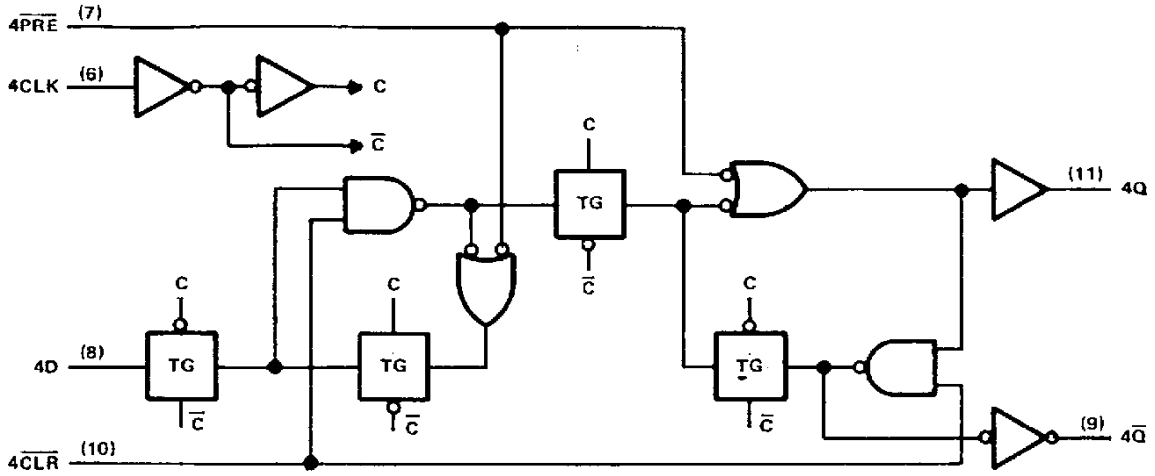
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

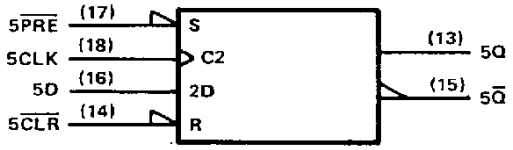
positive logic: $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$

Pin numbers shown are for DW, JT, and NT packages.

logic diagrams (positive logic)

D-TYPE FLIP-FLOPS





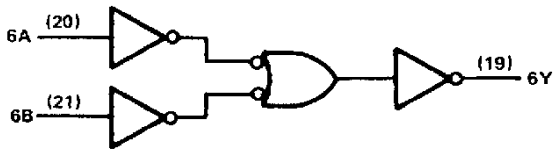
The detail above, and the composite logic symbol to the left, apply to both flip-flops.

FUNCTION TABLE
(EACH D FLIP-FLOP)

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

*This configuration is nonstable; i.e., it will not persist when either $\overline{PRE}$ or $\overline{CLR}$ returns to the inactive (high) level.

2-INPUT NOR GATE



FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

positive logic: $Y = \overline{A+B}$ or $Y = \overline{A} \cdot \overline{B}$

Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or JT package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or NT package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC7074			SN74HC7074			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		2	5	6	2	5	6	V
V_{IH} High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
	V_{CC} = 4.5 V	3.15			3.15			
	V_{CC} = 6 V	4.2			4.2			
V_{IL} Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	0		0.9	
	V_{CC} = 6 V	0		1.2	0		1.2	
V_I Input voltage		0		V_{CC}	0		V_{CC}	V
V_O Output voltage		0		V_{CC}	0		V_{CC}	V
t_t Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
	V_{CC} = 4.5 V	0		500	0		500	
	V_{CC} = 6 V	0		400	0		400	
T_A Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC7074		SN74HC7074		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	$V_I = V_{IH}$ or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	$V_I = V_{IH}$ or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	$V_I = V_{IH}$ or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	$V_I = V_{IH}$ or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	$V_I = V_{IH}$ or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0, I_O = 0	6 V			4		80		40	μA
C_i		2 to 6 V		3	10		10		10	pF

timing requirements for each D-type flip-flop over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC7074		SN74HC7074		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	5.5	0	3.7	0	4.5	MHz
			4.5 V	0	28	0	19	0	22	
			6 V	0	31	0	21	0	25	
t_w	Pulse duration	CLK high or CLR low	2 V	90		135		110		ns
			4.5 V	18		26		23		
			6 V	16		24		20		
		$\overline{PRE}$ low or $\overline{CLR}$ low	2 V	100		150		125		
			4.5 V	20		30		25		
			6 V	17		25		21		
t_{su}	Setup time before CLK↑	Data	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
		$\overline{PRE}$ high or $\overline{PRE}$ low	2 V	25		38		31		
			4.5 V	5		8		6		
			6 V	4		7		5		
t_h	Hold time, data after CLK↑		2 V	5		5		5		ns
			4.5 V	5		5		5		
			6 V	5		5		5		

switching characteristics for each D-type flip-flop over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC7074		SN74HC7074		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	5.5	10		3.7		4.5		MHz
			4.5 V	28	50		19		22		
			6 V	31	60		21		25		
t_{pd}	CLK	Q or $\overline{Q}$	2 V		45	175		263		219	ns
			4.5 V		15	35		53		44	
			6 V		13	30		45		38	
t_{pd}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	2 V		45	230		345		288	ns
			4.5 V		15	46		69		58	
			6 V		13	39		59		49	

C_{pd}	Power dissipation capacitance per flip-flop	No load, T_A = 25°C	40 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

switching characteristics for gates and inverters over recommended operating free-air temperature range (unless otherwise noted). C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC7074		SN74HC7074		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		24	90		135		115	ns
			4.5 V		9	18		27		23	
			6 V		7	15		23		20	
t_t		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per NAND or NOR gate	No load, T_A = 25°C	27 pF typ
	Power dissipation capacitance per inverter		20 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION DATA

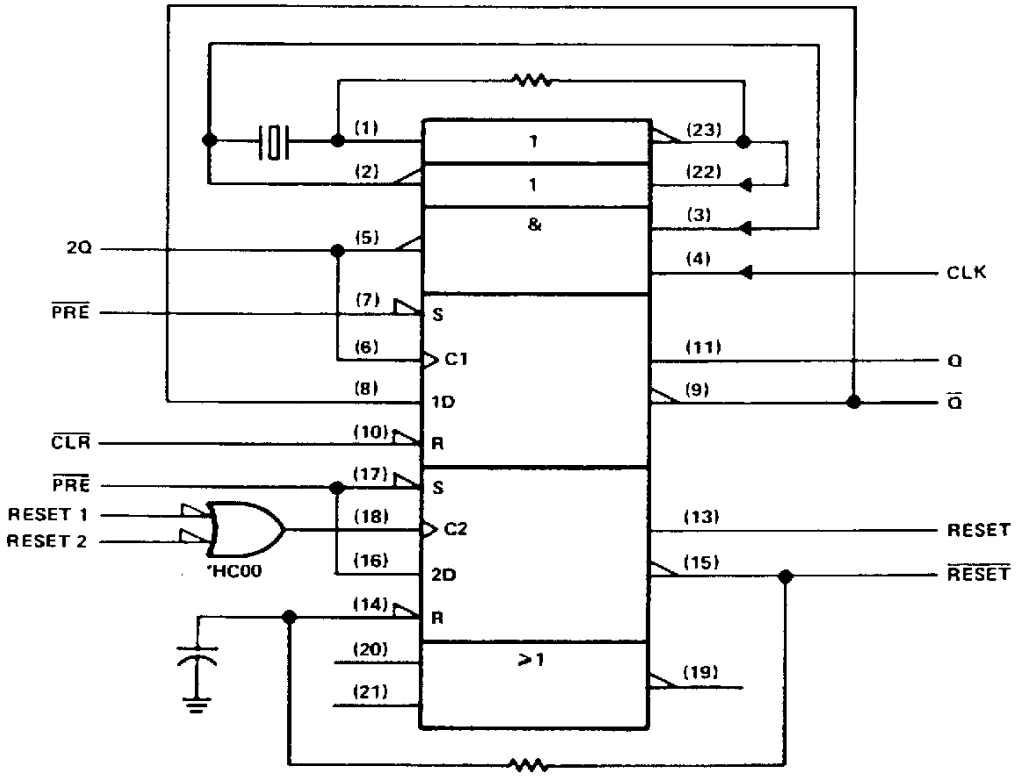


FIGURE 1. CLOCK AND RESET GENERATION FOR MICROPROCESSOR-BASED SYSTEM

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