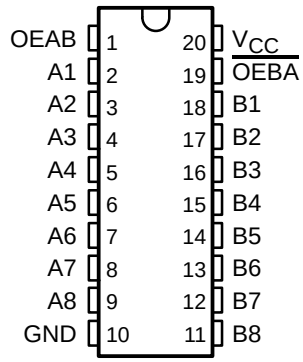
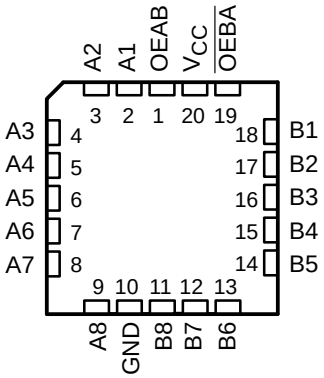
- **Inputs Are TTL-Voltage Compatible**
- **Lock Bus-Latch Capability**
- **True Logic**
- **High-Current 3-State Outputs Can Drive up to 15 LSTTL Loads**
- **Package Options Include Plastic Small-Outline (DW) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HCT623 . . . J OR W PACKAGE
SN74HCT623 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HCT623 . . . FK PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation allows for maximum flexibility in timing.

The ’HCT623 allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the output-enable (OEAB and $\overline{\text{OEBA}}$) inputs.

The output-enable inputs disable the device so that the buses are effectively isolated. The dual-enable configuration gives the transceivers the capability to store data by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. Each output reinforces its input in this transceiver configuration. When both OEAB and $\overline{\text{OEBA}}$ are enabled and all other data sources to the two sets of bus lines are in the high-impedance state, both sets of bus lines (16 total) remain at their last states. The 8-bit codes appearing on the two sets of buses are identical.

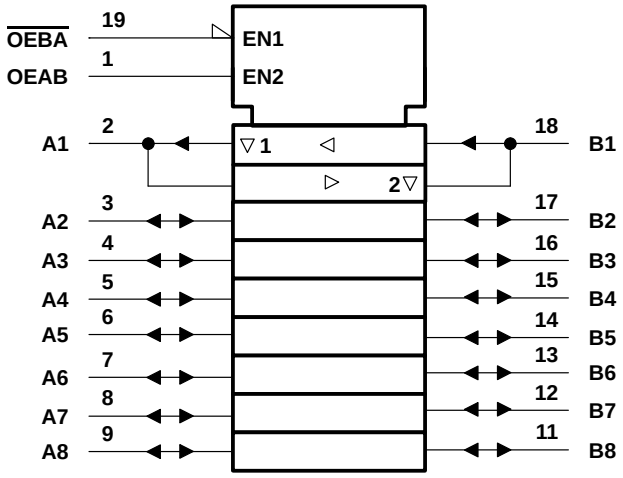
The SN54HCT623 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HCT623 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS		OPERATION
$\overline{\text{OEBA}}$	OEAB	
L	L	B data to A bus
H	H	A data to B bus
H	L	Isolation
L	H	B data to A bus, A data to B bus

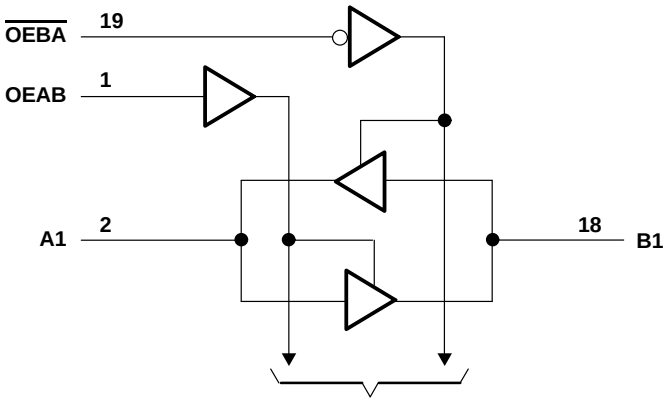
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range‡

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND . . . . . ±70 mA
Package thermal impedance, θ_{JA} (see Note 2): DW package . . . . . 97°C/W
N package . . . . . 67°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

			SN54HCT623			SN74HCT623			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time		0		500	0		500	ns
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HCT623		SN74HCT623		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		V_I = V_{IH} or V_{IL}	I_{OH} = –20 µA	4.5 V	4.4	4.499		4.4		4.4		V
			I_{OH} = –6 mA		3.98	4.3		3.7		3.84		
V_{OL}		V_I = V_{IH} or V_{IL}	I_{OL} = 20 µA	4.5 V		0.001	0.1		0.1		0.1	V
			I_{OL} = 6 mA			0.17	0.26		0.4		0.33	
I_I	$\overline{OEAB}$ or $\overline{OEBA}$	V_I = V_{CC} or 0		5.5 V			±0.1	±100		±1000		±1000	nA
I_{OZ}	A or B	V_O = V_{CC} or GND		5.5 V			±0.01	±0.5		±10		±5	µA
I_{CC}		V_I = V_{CC} or 0,	I_O = 0	5.5 V			8		160		80	µA
ΔI_{CC}†		One input at 0.5 V or 2.4 V, Other inputs at 0 or V_{CC}		5.5 V		1.4	2.4		3		2.9	mA
C_i	$\overline{OEAB}$ or $\overline{OEBA}$			4.5 V to 5.5 V		3	10		10		10	pF

† This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT623		SN74HCT623		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	4.5 V		15	22		33		28	ns
			5.5 V		13	20		30		25	
t_{en}	$\overline{OEBA}$	A	4.5 V		30	42		63		53	ns
			5.5 V		23	38		57		48	
t_{dis}	$\overline{OEBA}$	A	4.5 V		18	30		45		38	ns
			5.5 V		16	28		42		35	
t_{en}	OEAB	B	4.5 V		30	42		63		53	ns
			5.5 V		23	38		57		48	
t_{dis}	OEAB	B	4.5 V		18	30		45		38	ns
			5.5 V		16	28		42		35	
t_t		A or B	4.5 V		9	12		18		15	ns
			5.5 V		8	11		16		14	

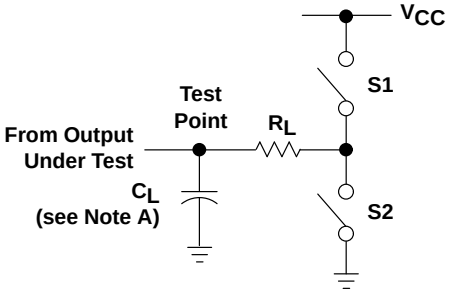
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT623		SN74HCT623		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	4.5 V		18	38		58		47	ns
			5.5 V		11	34		52		42	
t_{en}	$\overline{OEBA}$	A	4.5 V		36	59		89		74	ns
			5.5 V		30	53		80		67	
	OEAB	B	4.5 V		36	59		89		74	
			5.5 V		30	53		80		67	
t_t		A or B	4.5 V		17	42		63		53	ns
			5.5 V		14	38		57		48	

operating characteristics, T_A = 25°C

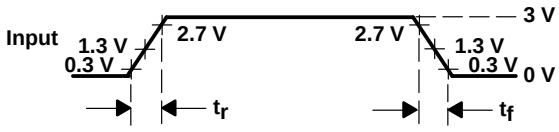
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	No load	40	pF

PARAMETER MEASUREMENT INFORMATION

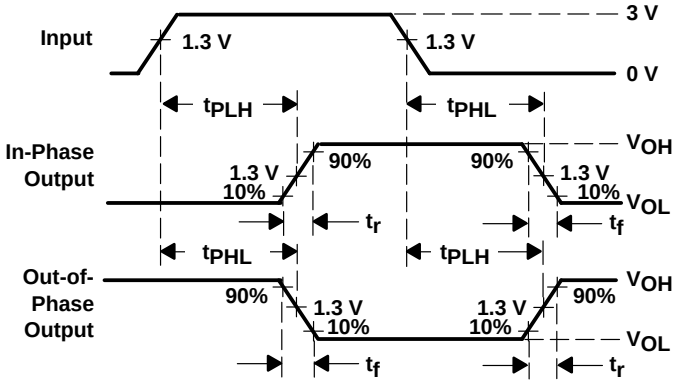


LOAD CIRCUIT

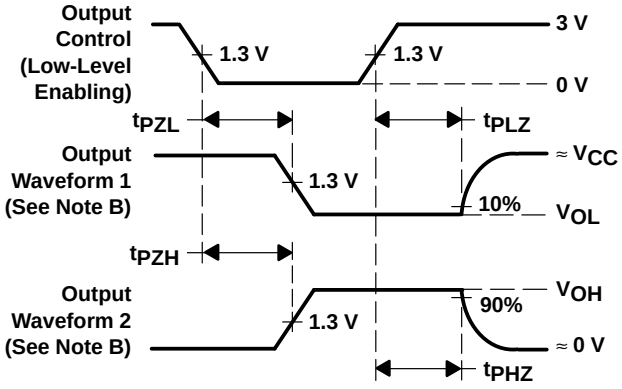
PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		––	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

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