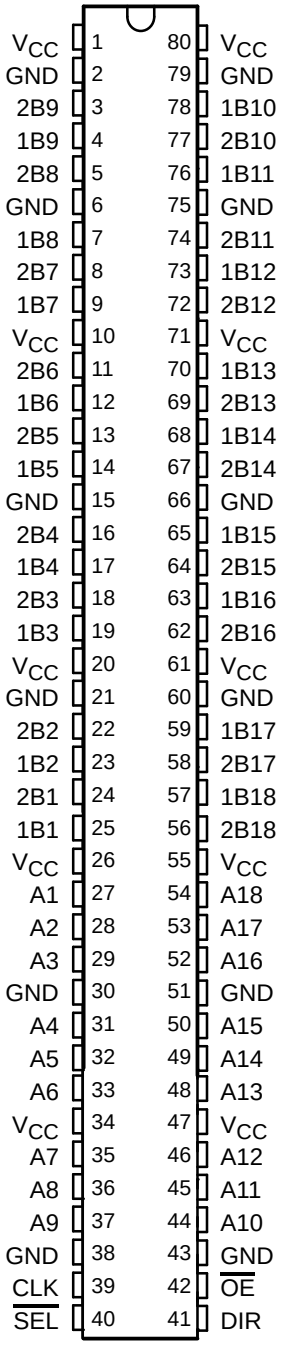
- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Sub-Micron Process**
- **A-Port Outputs Have Equivalent 50-Ω Series Resistors and B-Port Outputs Have Equivalent 20-Ω Series Resistors, So No External Resistors Are Required**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Packaged in Thin Shrink Small-Outline Package**

DBB PACKAGE
(TOP VIEW)



description

The SN74ALVCHG162282 is an 18-bit to 36-bit registered bus exchanger. This device is intended for use in applications where data must be transferred from a narrow high-speed bus to a wide lower-frequency bus. It is designed specifically for low-voltage (3.3 V) V_{CC} operation.

The device provides synchronous data exchange between the two ports. Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input. For data transfer in the B-to-A direction, the select ($\overline{SEL}$) input selects 1B or 2B data for the A outputs.

For data transfer in the A-to-B direction, a two-stage pipeline is provided in the 1B path, with a single storage register in the 2B path. Data flow is controlled by the active-low output-enable ($\overline{OE}$) and direction-control (DIR) input. DIR is registered to synchronize the bus direction changes with the clock.

description (continued)

The A-port N-channel output transistors are sized at 450 μm and the P-channel output transistors are sized at 700 μm. All A-port outputs have 50-Ω damping resistors. The B-port N-channel output transistors are sized at 225 μm, and the P-channel output transistors are sized at 560 μm. All B-port outputs have 20-Ω damping resistors.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The switching characteristics are based on a 25-pF (A port) and 80-pF (B port) load, but are tested with the standard 50-pF load.

The SN74ALVCHG162282 is characterized for operation from 0°C to 70°C.

Function Tables

A-TO-B STORAGE ($\overline{OE}$ = L, DIR = H)

INPUTS			OUTPUTS	
$\overline{SEL}$	CLK	A	1B	2B
H	X	X	$1B_0$†	$2B_0$†
L	↑	L	L‡	L
L	↑	H	H‡	H

† Output level before indicated steady-state input conditions were established

‡ Two CLK edges are needed to propagate the data.

B-TO-A STORAGE ($\overline{OE}$ = L, DIR = L)

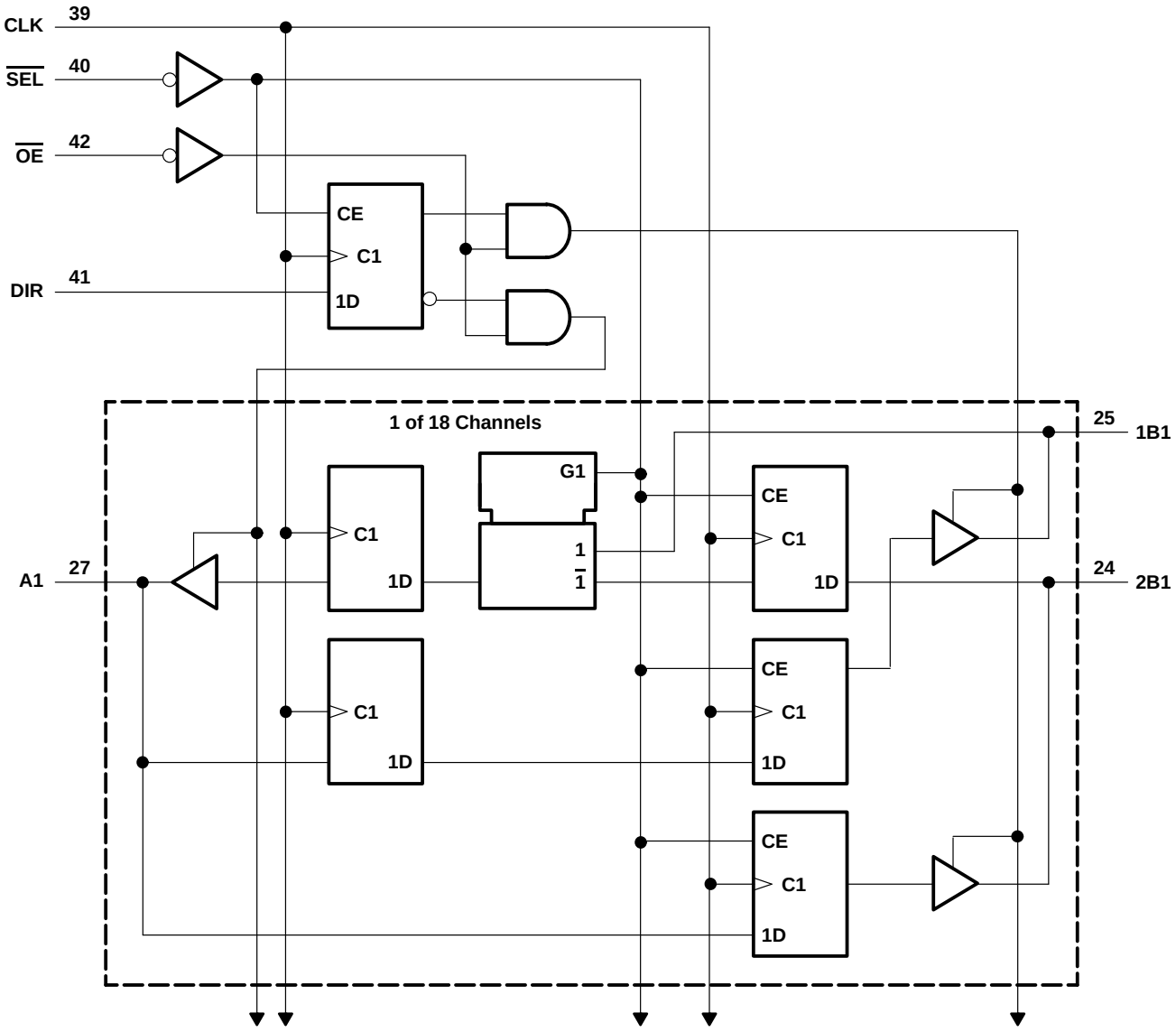
INPUTS				OUTPUT
CLK	$\overline{SEL}$	1B	2B	A
↑	H	X	L	L§
↑	H	X	H	H§
↑	L	L	X	L
↑	L	H	X	H

§ Two CLK edges are needed to propagate the data. The data is loaded in the first register when $\overline{SEL}$ is low and propagates to the second register when $\overline{SEL}$ is high.

OUTPUT ENABLE

INPUTS			OUTPUTS	
CLK	$\overline{OE}$	DIR	A	1B, 2B
↑	H	X	Z	Z
↑	L	H	Z	Active
↑	L	L	Active	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
I/O ports (see Notes 1 and 2) . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . –50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 3) . . . . . 106°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The input and output positive voltage ratings may be exceeded up to 4.6 V if the input and output clamp-current ratings are observed.
3. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

recommended operating conditions (see Note 4)

				MIN	MAX	UNIT
V_{CC}	Supply voltage			3	3.6	V
V_{IH}	High-level input voltage		V_{CC} = 3 V to 3.6 V	2		V
V_{IL}	Low-level input voltage		V_{CC} = 3 V to 3.6 V		0.8	V
V_I	Input voltage			0	V_{CC}	V
V_O	Output voltage			0	V_{CC}	V
I_{OH}	High-level output current	A to B	V_{CC} = 3 V		8	mA
		B to A	V_{CC} = 3 V		6	
I_{OL}	Low-level output current	A to B	V_{CC} = 3 V		8	mA
		B to A	V_{CC} = 3 V		6	
$\Delta t/\Delta v$	Input transition rise or fall rate			0	10	ns/V
T_A	Operating free-air temperature			0	70	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP†	MAX	UNIT
V_{OH}		I_{OH} = –100 μA	3 V to 3.6 V	V_{CC}–0.2			V
	A to B	I_{OH} = –8 mA	3 V	2			
	B to A	I_{OH} = –6 mA	3 V	2			
V_{OL}		I_{OL} = 100 μA	3 V to 3.6 V			0.2	V
	A to B	I_{OL} = 8 mA	3 V			0.8	
	B to A	I_{OL} = 6 mA	3 V			0.8	
I_I		V_I = V_{CC} or GND	3.6 V			±5	μA
$I_{I(hold}$		V_I = 0.8 V	3 V	75			μA
		V_I = 2 V	3 V	–75			
		V_I = 0 to 3.6 V‡	3.6 V			±500	
I_{OZ}§		V_O = V_{CC} or GND	3.6 V			±10	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	3.6 V			40	μA
ΔI_{CC}		One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V			750	μA
C_i	Control inputs	V_I = V_{CC} or GND	3.3 V		4		pF
C_{io}	A or B ports	V_O = V_{CC} or GND	3.3 V		8.5		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ This is the bus-hold maximum dynamic current required to switch the input from one state to another.
§ For I/O ports, the parameter I_{OZ} includes the input leakage current.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

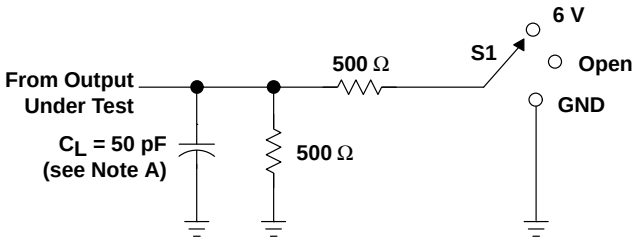
			V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	
f_{clock}	Clock frequency			160	MHz
t_w	Pulse duration, CLK high or low		2.3¶		ns
t_{su}	Setup time, high or low	A data before CLK↑	1.5		ns
		B data before CLK↑	2		
		DIR before CLK↑	2		
		$\overline{SEL}$ before CLK↑	2		
t_h	Hold time, high or low	A data after CLK↑	0.3		ns
		B data after CLK↑	0.3		
		DIR after CLK↑	0.3		
		$\overline{SEL}$ after CLK↑	0.3		

¶ The parameter is warranted but not production tested.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 25 pF (A port), 80 pF (B port) (unless otherwise noted) (see Figure 1)

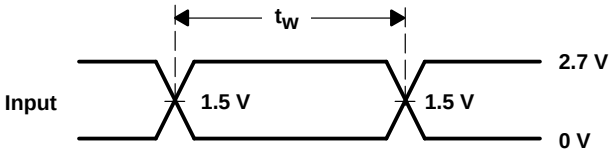
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	
f_{max}			160		MHz
t_{pd}	CLK	A	1.5	5	ns
		B	1.5	7.4	
t_{en}	CLK	A	1.5	6.3	ns
		B	1.5	9.4	
	$\overline{OE}$	A	1.5	6	
		B	1.5	9.5	
t_{dis}	CLK	A	1.5	6.4	ns
		B	1.5	7.8	
	$\overline{OE}$	A	1.5	5	
		B	1.5	7.6	

PARAMETER MEASUREMENT INFORMATION

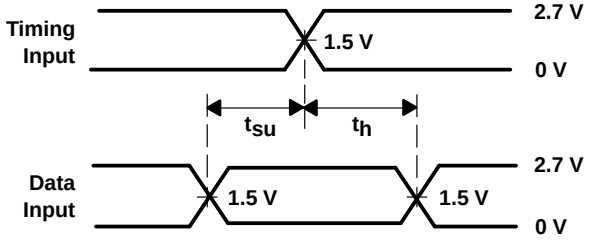


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

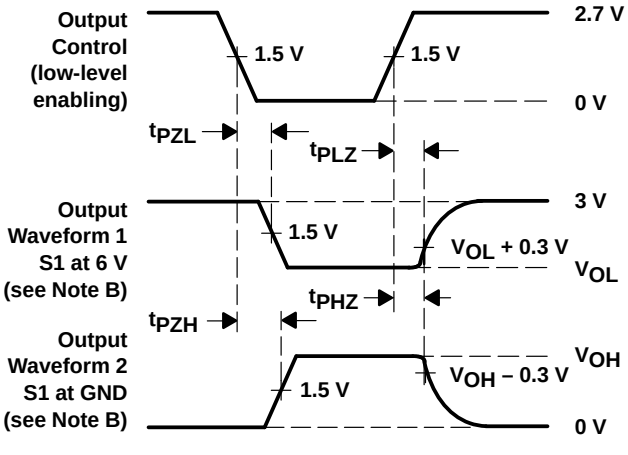
LOAD CIRCUIT



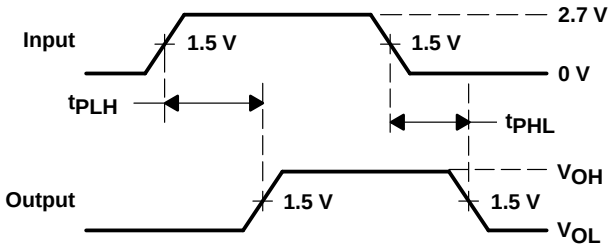
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.