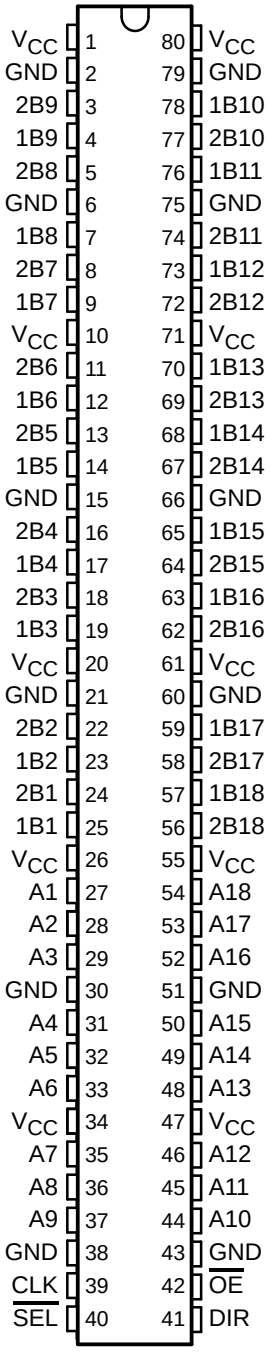
- **EPIC™ (Enhanced-Performance Implanted CMOS) Sub-Micron Process**
- **Output Ports Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required**
- **Member of the Texas Instruments Widebus™ Family**
- **Bus-Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Packaged in Thin Shrink Small-Outline Package**

**DBB PACKAGE**
**(TOP VIEW)**




## description

The SN74ALVCHR162282 is an 18-bit to 36-bit registered bus exchanger designed for 2.3-V to 3.6-V $V_{CC}$ operation. This part is intended for use in applications where data must be transferred from a narrow high-speed bus to a wide lower-frequency bus. It is designed specifically for low-voltage (3.3-V) $V_{CC}$ operation.

The device provides synchronous data exchange between the two ports. Data is stored in the internal registers on the low-to-high transition of the CLK input. For data transfer in the B-to-A direction, $\overline{SEL}$ selects 1B or 2B data for the A outputs.

For data transfer in the A-to-B direction, a two-stage pipeline is provided in the 1B path, with a single storage register in the 2B path. Data flow is controlled by the active-low output enable ($\overline{OE}$) and the DIR input. The DIR control pin is registered to synchronize the bus direction changes with the clock.

The outputs, which are designed to sink up to 12mA, include 26-Ω resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCHR162282 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

## FUNCTION TABLES

**A-TO-B STORAGE ($\overline{OE}$ = L, DIR = H)**

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| $\overline{SEL}$ | CLK | A | 1B | 2B |
| H | X | X | $1B_0$† | $2B_0$† |
| L | ↑ | L | L‡ | X |
| L | ↑ | H | H‡ | X |

† Output level before the indicated steady-state input conditions are established

‡ Two CLK edges are needed to propagate the data.

**B-TO-A STORAGE ($\overline{OE}$ = L, DIR = L)**

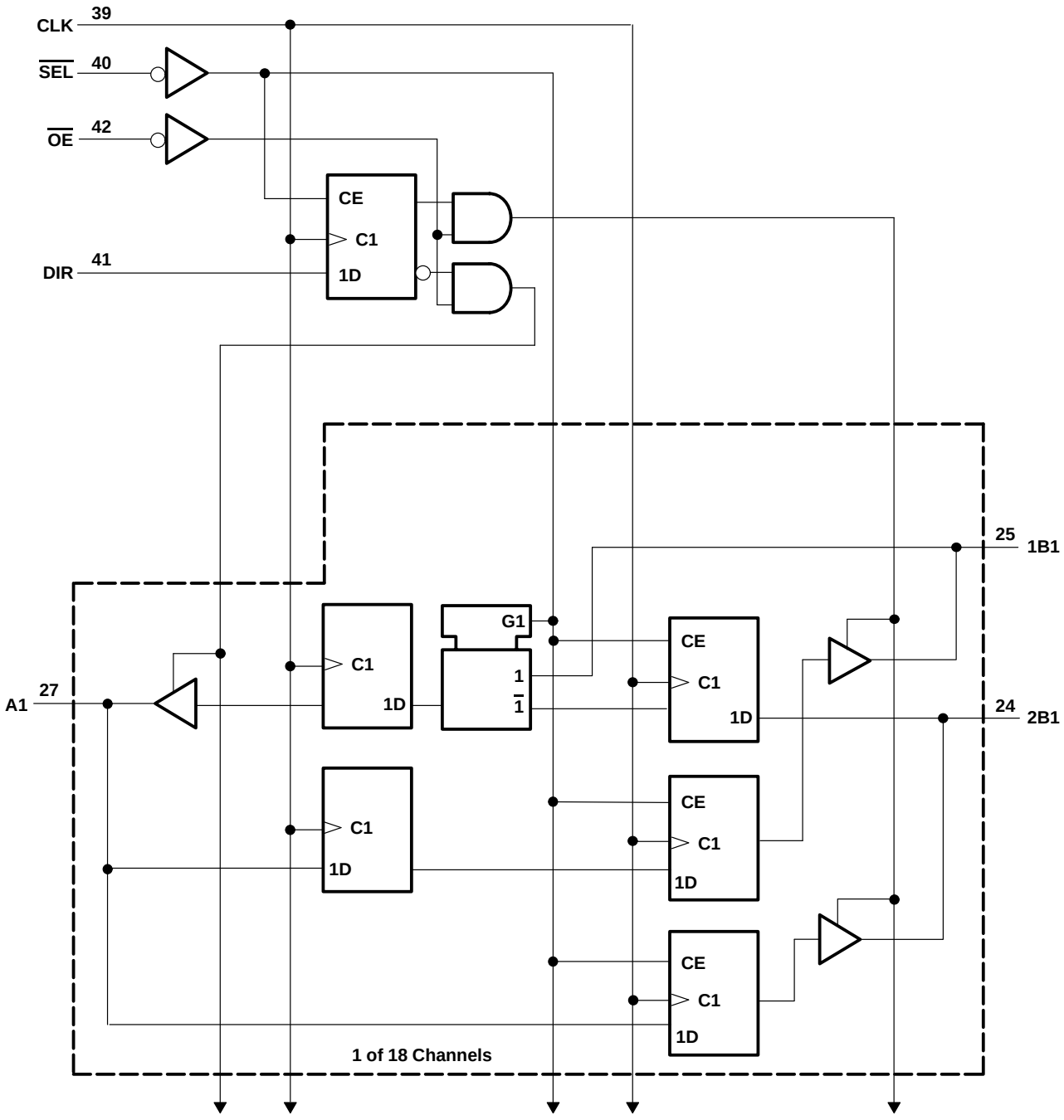
| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| CLK | $\overline{SEL}$ | 1B | 2B | A |
| ↑ | H | X | L | L§ |
| ↑ | H | X | H | H§ |
| ↑ | L | L | X | L |
| ↑ | L | H | X | H |

§ Two clock edges are needed to propagate the data. The data is loaded in the first register when $\overline{SEL}$ is low and propagates to the second register when $\overline{SEL}$ is high.

**OUTPUT ENABLE**

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| CLK | $\overline{OE}$ | DIR | A | 1B, 2B |
| ↑ | H | X | Z | Z |
| ↑ | L | L | Z | Active |
| ↑ | L | H | Active | Z |

**logic diagram (positive logic)**



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 4.6 V
Input voltage range, $V_I$: Except I/O ports (see Note 1) . . . . . –0.5 V to 4.6 V
I/O ports (see Notes 1 and 2) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Output voltage range, $V_O$ (see Notes 1 and 2) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . –50 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) . . . . . ±50 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ±50 mA
Continuous current through each $V_{CC}$ or GND . . . . . ±100 mA
Maximum power dissipation at $T_A$ = 55°C (in still air) (see Note 3) . . . . . 0.84 W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

PRODUCT PREVIEW

### recommended operating conditions (see Note 4)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2.3 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2.3 V to 2.7 V | | 0.7 | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | | 0.8 | |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2.3 V | | –6 | mA |
| | | $V_{CC}$ = 2.7 V | | –8 | |
| | | $V_{CC}$ = 3 V | | –12 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2.3 V | | 6 | mA |
| | | $V_{CC}$ = 2.7 V | | 8 | |
| | | $V_{CC}$ = 3 V | | 12 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 0 | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | | $I_{OH}$ = –100 μA | | 2.3 V to 3.6 V | $V_{CC}$–0.2 | | | V |
| | | $I_{OH}$ = –4 mA | $V_{IH}$ = 1.7 V | 2.3 V | 1.9 | | | |
| | | | $V_{IH}$ = 2 V | 2.7 V | 2.2 | | | |
| | | $I_{OH}$ = –6 mA | $V_{IH}$ = 1.7 V | 2.3 V | 1.7 | | | |
| | | | $V_{IH}$ = 2 V | 3 V | 2.4 | | | |
| | | $I_{OH}$ = –8 mA, | $V_{IH}$ = 2 V | 2.7 V | 2 | | | |
| | | $I_{OH}$ = –12 mA, | $V_{IH}$ = 2 V | 3 V | 2 | | | |
| $V_{OL}$ | | $I_{OH}$ = 100 μA | | 2.3 V to 3.6 V | | | 0.2 | V |
| | | $I_{OH}$ = 4 mA | $V_{IL}$ = 0.7 V | 2.3 V | | | 0.4 | |
| | | | $V_{IL}$ = 0.8 V | 2.7 V | | | 0.4 | |
| | | $I_{OH}$ = 6 mA | $V_{IL}$ = 0.7 V | 2.3 V | | | 0.55 | |
| | | | $V_{IL}$ = 0.8 V | 3 V | | | 0.55 | |
| | | $I_{OH}$ = 8 mA, | $V_{IL}$ = 0.8 V | 2.7 V | | | 0.6 | |
| | | $I_{OH}$ = 12 mA, | $V_{IL}$ = 0.8 V | 3 V | | | 0.8 | |
| $I_I$ | | $V_I$ = $V_{CC}$ or GND | | 3.6 V | | | ±5 | μA |
| $I_{I(hold)}$ | | $V_I$ = 0.7 V | | 2.3 V | 45 | | | μA |
| | | $V_I$ = 1.7 V | | | –45 | | | |
| | | $V_I$ = 0.8 V | | 3 V | 75 | | | |
| | | $V_I$ = 2 V | | | –75 | | | |
| | | $V_I$ = 0 to 3.6 V‡ | | 3.6 V | | | ±500 | |
| $I_{OZ}$§ | | $V_O$ = $V_{CC}$ or GND | | 3.6 V | | | ±10 | μA |
| $I_{CC}$ | | $V_I$ = $V_{CC}$ or GND, | $I_O$ = 0 | 3.6 V | | | 40 | μA |
| $\Delta I_{CC}$ | | One input at $V_{CC}$ – 0.6 V, | Other inputs at $V_{CC}$ or GND | 3 V to 3.6 V | | | 750 | μA |
| $C_i$ | Control inputs | $V_I$ = $V_{CC}$ or GND | | 3.3 V | | | | pF |
| $C_{io}$ | A or B ports | $V_O$ = $V_{CC}$ or GND | | 3.3 V | | | | pF |

† All typical values are measured at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
‡ This is the bus-hold maximum dynamic current required to switch the input from one state to another.
§ For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.

## timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

| | | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | | | | | | | MHz |
| $t_w$ | Pulse duration, CLK high or low | | | | | | | | ns |
| $t_{su}$ | Setup time | A data before CLK↑ | | | | | | | ns |
| | | B data before CLK↑ | | | | | | | |
| | | DIR before CLK↑ | | | | | | | |
| | | $\overline{SEL}$ before CLK↑ | | | | | | | |
| $t_h$ | Hold time | A data after CLK↑ | | | | | | | ns |
| | | B data after CLK↑ | | | | | | | |
| | | DIR after CLK↑ | | | | | | | |
| | | $\overline{SEL}$ after CLK↑ | | | | | | | |

PRODUCT PREVIEW

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature, (unless otherwise noted) (see Figures 1 and 2)**

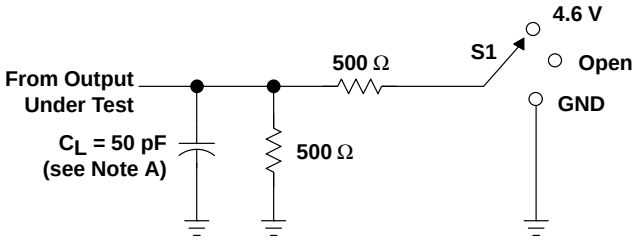
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | | | | | | | MHz |
| $t_{pd}$ | CLK | A | | | | | | | ns |
| | CLK | B | | | | | | | |
| $t_{en}$ | $\overline{OE}$ | A | | | | | | | ns |
| | $\overline{OE}$ | B | | | | | | | |
| $t_{dis}$ | $\overline{OE}$ | A | | | | | | | ns |
| | $\overline{OE}$ | B | | | | | | | |

**operating characteristics, $T_A$ = 25°C**

| PARAMETER | | | TEST CONDITIONS | $V_{CC}$ = 2.5 V ± 0.2 V | $V_{CC}$ = 3.3 V ± 0.3 V | UNIT |
|---|---|---|---|---|---|---|
| | | | | TYP | TYP | |
| $C_{pd}$ | Power dissipation capacitance | Outputs enabled | $C_L$ = 0, f = 10 MHz | | | pF |
| | | Outputs disabled | | | | |

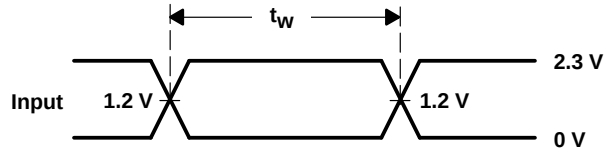
PRODUCT PREVIEW

## PARAMETER MEASUREMENT INFORMATION
## $V_{CC}$ = 2.5 V ± 0.2 V

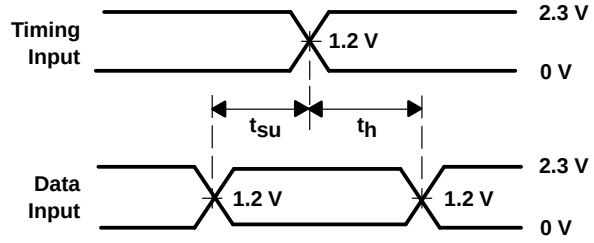



| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 4.6 V |
| $t_{PHZ}/t_{PZH}$ | GND |

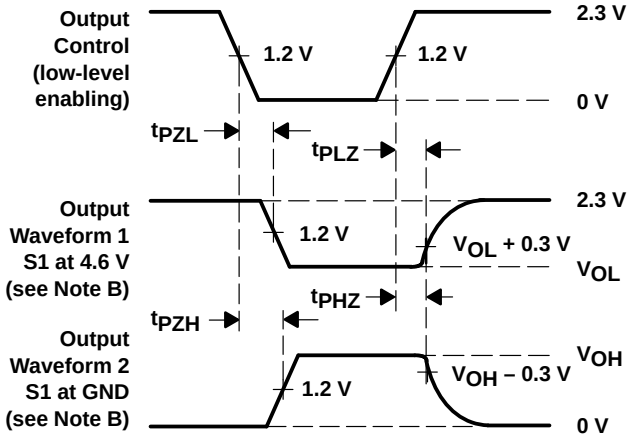
LOAD CIRCUIT



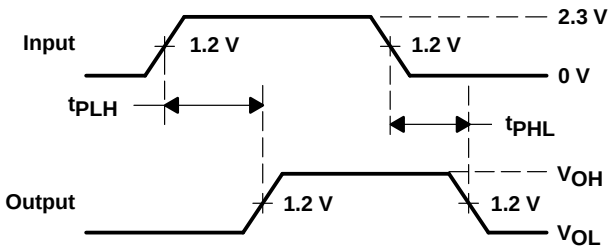

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

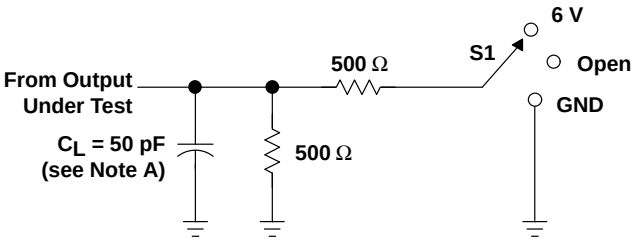



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

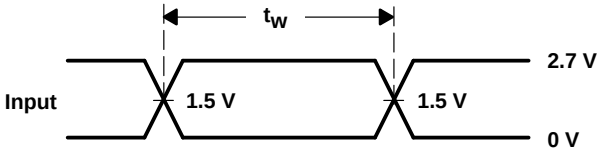
**Figure 1. Load Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION
## $V_{CC}$ = 2.7 V AND 3.3 V ± 0.3 V

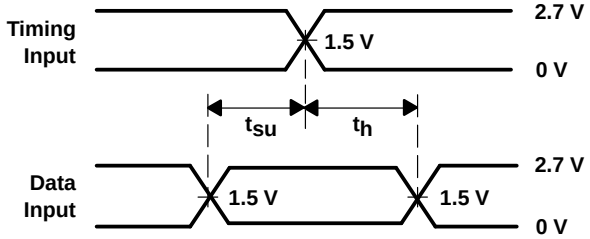



| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 6 V |
| $t_{PHZ}/t_{PZH}$ | GND |

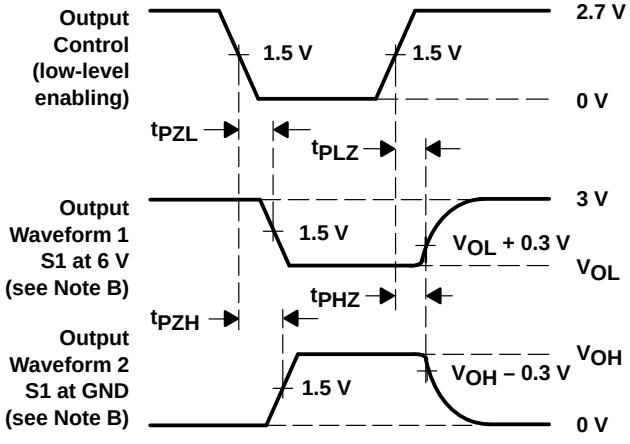
LOAD CIRCUIT



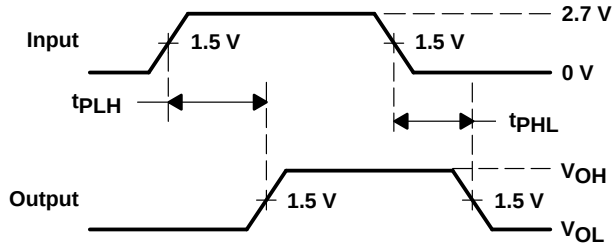

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

**Figure 2. Load Circuit and Voltage Waveforms**

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